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# Editorial

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This issue of *JETTA* contains eight papers and a Letter. The topics covered are scan test, verification, analog test, asynchronous circuits, and memory testing. The first paper is derived from the *IEEE European Test Symposium* (ETS) of 2009. Similarly, the second and sixth papers consist of detailed manuscripts of presentations made by the authors at ETS of 2010. We are thankful to Cecilia Metra for conducting the journal's peer review procedure for these papers.

In the first paper the authors, Inoue, Yoneda, Hasegawa and Fujiwara from Nara Institute of Science and Technology, Nara, Japan, propose a balanced secure scan design that prevents malicious use of the scan structure to access safety critical data. Their partial scan technique leads to a balanced circuit in which all paths between any pair of nodes have the same number of clock cycle delays. A balanced circuit though sequential is amenable to combinational test generation.

The second paper proposes the use of coding theory in the design of time compactors for scan out data emerging from multiple scan chains. The paper is authored by Gizdarski of Synopsys, Incorporated, Mountain View, California.

The third and the fourth articles discuss verification issues. Tadesse and Grodstein of Intel Corporation, Hudson, Massachusetts and Bahar of Brown University, Providence, Rhode Island describe the use of Boolean satisfiability (SAT) methods for generating vectors to test the critical path of a circuit. Another paper by G. Di Guglielmo, L. Di Guglielmo, Fummi and Pravadelli from University of Verona in Italy employs the concept of extended finite state machines to generate vectors for functional verification.

The fifth and sixth articles deal with analog and mixed-signal test. The paper by Jin of National Semiconductor Corporation, Santa Clara, California describes methods for linearity testing of analog to digital converters using a Kalman filter. The results show improved accuracy and reduced test time over conventional testing. The next paper is authored by Mozuelos, Lechuga, Martinez and Bracho from University of Cantabria in Spain. They propose the use of a built in sensor for quiescent and transient currents. The amplitude and duration of the transient current serve as fault signatures as demonstrated through actual hardware testing.

The seventh paper discusses testing of asynchronous circuits. It describes the implementation of a completely asynchronous scan test mode such that testing is supported by combinational automatic test pattern generation. The authors are Cheng and Li from National Taiwan University, Taipei, Taiwan.

The eighth paper discusses memory test. The authors, Nourivand and Al-Khalili of Concordia University, Montreal, Canada and Savaria of Ecole Polytechnique de Montreal, Montreal, Canada, report new fault modes for SRAMs that have a drowsy mode. A new type of *March* test is proposed.

The final article is a *JETTA* Letter authored by Maestro and Reviriego of Universidad Antonio de Nebrija, Madrid, Spain, Argyrides of Oxford Brookes University, Oxford, UK and Pradhan of University of Bristol, Bristol, UK. The authors present a soft error tolerant design of an encoder for use in an error correcting memory.

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