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Editorial

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This issue contains ten articles, including three *Letters*. The topics of these articles are hardware security, fault tolerance, test compression, reliability, signal integrity, mixed-signal testing, interconnect testing, test application, and approximate computing.

The first paper addresses hardware security. Wang, Guin and Singh from Auburn University, Auburn, Alabama, USA revisit generation of true random numbers from the power-up state of SRAM. Aging degrades the true random nature of these numbers. The authors show that periodic stressing of SRAM in the power-up state can preserve the true randomness.

The second paper examines the faults and reliability of a logic circuit realized as a switching lattice. Almost half a century ago, Sheldon B. Akers proposed this design style in a paper, "A Rectangular Logic Array" (*IEEE Transactions on Computers*, volume C-21, number 8, pages 848–857, August 1972). Present contributors are Anghel and Vatajelu from TIMA Laboratory of Grenoble-Alpes University in France, Bernasconi from University of Pisa in Italy, Ciriani and Trucco from University of Milan in Italy, and Frontini from INFN, Milan, Italy. They investigate effects of single stuck-at faults and the use of the available redundancy for fault tolerance. This paper was originally presented at the *Twentieth IEEE Latin-American Test Symposium* (LATS), held during March 11–13, 2019 in Santiago, Chile. *JETTA* Editor Leticia M. B. Poehls is responsible for the peer reviewing of the journal version.

The third paper provides a test compression methodology for the circular scan DFT (design for testability) architecture. The authors are Mitra from Tripura Institute of Technology, Agartala, India and Das from Assam University, Silchar, India. They achieve reductions in test data volume and test application time by exploiting computing algorithms such as ant colony optimization (ACO) and traveling salesman problem (TSP) solver.

In the fourth paper, Viterbi decoding circuits are designed with error detection schemes. Implementations in several logic gate technologies are analyzed for power, delay and area. Authors are Varada, Katpally and Thiruveedhi from CVR College of Engineering, Hyderabad, India.

In the fifth paper, Yu, Wang and Xu from Tianjin University, Tianjin, China address problems that occur during data transmission. These problems are associated with signal integrity (crosstalk, etc.) and power supply noise (voltage droop, etc.) Authors find that the pseudorandom bit sequence (PRBS) stimuli commonly used in simulation may not be the best for reliability assessment of data transmission. They suggest a modified PRBS that is influenced by the resonance frequency of the power distribution network (PDN).

Sixth paper proposes a method for reducing the measurement noise by using multiwavelet decomposition. Higher accuracy in measuring parameters of an analog-to-digital converter (ADC) is demonstrated. Authors are Ma, Huang, Yang and Tang from University of Electronic Science and Technology of China, Chengdu, China.

In the seventh paper, Bhowmik from National Institute of Technology Karnataka, Surathkal, India discusses testing of open faults of interconnects on a network-on-chips (NoC). Test efficiency is achieved by implementing distributed hardware for built-in self-test (BIST) and scheduling tests for multiple interconnects in parallel.

Next, there are three *JETTA* Letters.

Should we stop testing on the first failure, or continue through all tests to observe multiple failures? The question is addressed in the first letter by Yucesan and Ozkil from Atilim University, Ankara, Turkey. Investigation shows stopping at first failure reduces test time and running all tests gives useful information for test planning, which can save testing cost in the end. Authors recommend an interchangeable application of both techniques with more frequent use of stopping at first failure.

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Last two letters provide designs of approximate hardware for image processing applications. These designs offer reduced area, delay and power while preserving accuracy within acceptable range. The first letter gives the design of a memory. Authors are Jothin from Infant Jesus College of Engineering, Thoothukudi, India and Mohamed from Robert Bosch Engineering and Business Solutions, Coimbatore, India. In the second letter, Garg and Patel from Thapar Institute of Engineering and Technology, Patiala, India and Dutt from Indian Institute of Information Technology, Vadodara, India present an approximate multiplier circuit.