Journal of Electronic Testing (2020) 36:439–440
https://doi.org/10.1007/s10836-020-05900-6

Editorial

Vishwani D. Agrawal[1]

Received: 28 July 2020 / Accepted: 28 July 2020 / Published online: 3 August 2020

This issue contains ten articles, including two *Letters*. The topics of these articles are automatic test equipment (ATE), soft errors, mixed-signal circuit testing, MEMS testing, FPGA testability, memrister reliability, online test, and fault tolerance

In the first paper, Gurevich and Deshmukh of Intel Corporation, Chandler, Arizona, USA, address the issue of current carrying capacity (CCC) of the connection between the automatic test equipment (ATE) and the device under test (DUT). CCC is strongly dependent upon the types of ATE socket and DUT pin. Borrowing from four different industry standards, the authors define a set of CCC requirements for a present-day DUT and discuss the related simulation and measurement methods. They identify temperature and pin-force as additional parameters affecting the CCC.

The next two papers focus on single events, cross-talk and transients.

In the second paper, B. Liu from Air Force Engineering University, XinYang, HeNan, China, and Cai and X. Liu from Air Force Engineering University, Xi'An, ShannXi, China present an analytical model for crosstalk produced by single event transients (SET). Interconnects are modeled as distributed RLC circuits consisting of parasitic capacitance and inductance.

The third paper defines the reliability of a logic circuit in the presence of transient faults as the probability of correct output. This is a function of the input vector and accounts for the error masking effect of logic gates. It is evaluated through simulation. The resulting characterization then allows evaluation of the circuit reliability in the presence of soft errors. Contributors of this work are Cai, He, Wang, Yin and Yu from Changsha University of Science and Technology, Changsha, HN, China, Liu from Guangdong University of Technology, Guangzhou, GD, China, and Li from Chinese Academy of Sciences, Beijing, China.

The focus shifts to mixed-signal testing in the next two papers.

In the fourth paper, Deng, Chen and Zhang from Southwest Petroleum University, Chengdu, China address the problem of identifying incipient faults in nonlinear analog circuits. An incipient fault refers to the start of deviation in a component parameter such that the circuit performance begins to degrade. The proposed method uses a high order moment fractional transform (HMFT) and the authors demonstrate improved result compared to other known methods, such as fuzzy nonlinear programming (FNLP).

The fifth paper presents experimental results from radiation tests on key modules of a wireless-based monitoring system containing analog signal processing circuits, analog-to-digital converter (ADC) modules, microcontroller modules, and wireless transmission modules. Authors are Huang, Jiang and Deng from University of Western Ontario, London, Ontario, Canada.

Sixth paper addresses the sensitivity of a MEMS (micro-electro-mechanical system) pressure sensor. It consists of a piezoelectric device that converts the pressure change into resistance change, to be measured through a Wheatstone bridge configuration. Contributors are Jindal and De from Vellore Institute of Technology, Vellore, Tamil Nadu, India, Kumar from National Institute of Technology, Jamshedpur, Jharkhand, India, and Raghuwanshi from Indian Institute of Technology (Indian School of Mines), Dhanbad, Jharkhand, India.

In the seventh paper, by Palchaudhuri and Dhar from Indian Institute of Technology Kharagpur, West Bengal, India, we find a method of incorporating testability in a field programmable gate array (FPGA). Unused inputs of the look-up table (LUT) are employed to implement a variety of scan paths that help in testing and fault localization.

Ishizaka, Shintani and Inoue, from Nara Institute of Science and Technology (NAIST), Nara, Japan, are the authors of the eighth paper where the discussion is on resistive random-access memory (ReRAM). The authors point out that the basic component of ReRAM, memristor, has a lower write endurance and hence, an error-correcting code (ECC) circuit is

✉ Vishwani D. Agrawal
agrawvd@auburn.edu

[1] Auburn University, Auburn, AL 36849, USA

essential for reliability. They propose a hybrid CMOS-memristor ECC circuit to maintain a balance between the area overhead and reliability.

Next, there are two *JETTA* Letters.

The ninth article gives the design of an application specific integrated circuit (ASIC) to be used for fault detection and diagnosis of an electromechanical actuator. Contributors are Piccoli, Balen, and Henriques from Federal University of Rio Grande do Sul, Porto Alegre, RS, Brazil.

In the tenth and the last article, Mohammadi, Omidi and Lotfinejad, from University of Zanjan, Zanjan, Iran, propose a design for a fault-tolerant adder. They implement a Berger code checker using current mode multi-valued logic (CM-MVL) for area and power efficiency.