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Editorial

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I am pleased to announce the 2019 JETTA-TTTC Best Paper Award. We congratulate the winners, Breeta SenGupta, Dimitar Nikolov, Assmitra Dash and Erik Larsson. Their paper "Test Flow Selection for Stacked Integrated Circuits," appeared in *Journal of Electronic Testing: Theory and Applications,* Volume 35, Number 4, pp. 425–450, August 2019. See details following this editorial.

Following the tradition, the selection of the best paper was a two-phase process. In the first phase, the editorial board examined the six issues of 2019 (volume 35) to recommend papers that seemed to stand out. In the second phase, starting from the result of the first phase, an awards committee selected the winner. This year's committee, appointed by the IEEE Test Technology Technical Council (TTTC) of the IEEE Computer Society, consisted of Xiaoqing Wen (Chair), Jennifer Dworak, Jiun-Lang Huang and Nicola Nicolici. Yervant Zorian, TTTC President, announced the award at a plenary session of the International Test Conference in November 2020.

The first three papers of this issue were originally presented at *28th IEEE Asian Test Symposium* (ATS'19), held in Kolkata, India during December 10–13, 2019. We are thankful to program chairs of ATS'19, Rubin Parekhji of Texas Instruments, India, and James Chien-Mo Li of National Taiwan University, Taipei, Taiwan, for serving as editors.

The fourth paper in this issue is the sixth to come this year from the *Latin-American Test Symposium* (LATS). Over the years, we have developed a close cooperation with LATS, due mainly to efforts of Professor Leticia M. B. Poehls. We again thank her.

We encourage authors of papers in recent conferences to contribute to *JETTA*. All submitted papers are examined by a coordinating editor who conducts the peer review process. A paper can be published in one of two categories, regular papers (no page limit) or *JETTA Letters* (up to six pages). *JETTA* imposes no page charge but the article must include references of the conference or workshop proceedings, and a brief summary of previous accomplishments and enhancements beyond the journal version. Authors should consider expanding technical discussion, analysis and results, and using a different title.

This issue contains eight articles including a *Letter*. Topics addressed are nonlinear systems, on-line error detection, analog and mixed-signal testing, signal integrity, FPGA reliability, reversible logic, 3D-stacked device testing, and SEU protection.

In the first paper, Momtaz and Chatterjee from Georgia Institute of Technology, Atlanta, Georgia, USA, use machine learning for error diagnosis and fault recovery in nonlinear systems. They demonstrate their technique on a flying vehicle.

Next, Ozen and Orailoglu from University of California, San Diego, California, USA present their error detection system named Self-Check. It is a software system that detects hardware errors in a variety of applications.

The third paper presents a method for identifying a small set of internal test nodes to enhance the fault coverage in an analog circuit. The method derives efficiency from graph partitioning of transistor netlist and DC analysis. Authors are Sanyal, Patra and Dasgupta from Indian Institute of Technology Kharagpur, West Bengal, India, and Bhattacharya from Synopsys Inc., USA.

The fourth paper addresses the problem of signal integrity caused by coupling capacitance. The authors modify Dijkstra's shortest path algorithm to find pairs of input to output paths that are likely to be influenced by coupling. Authors are Meza-Ibarra, Gomez-Fuentes, Noriega and Vera-Marquina from Universidad de Sonora, Hermosillo, México, and Champac from National Institute for Astrophysics, Optics and Electronics, Puebla, México.

The fifth paper examines several adder and multiplier architectures for area, power, speed and soft error reliability when they are implemented on a field programmable gate array (FPGA). Authors are Gokalan and Tosun from Hacettepe University, Ankara, Turkey, and Dal from Ataturk University, Erzurum, Turkey.

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The sixth paper deals with reversible logic, which is an emerging technology. Authors are Kheirandish, Haghparast and Reshadi from Islamic Azad University, Tehran, Iran, and Hosseinzadeh from Iran University of Medical Sciences, Tehran, Iran. They provide designs of 3-input and 5-input majority voter circuits, which are used in reliability implementation by modular redundancy.

The seventh paper gives a method for diagnosis of multiple faults in through silicon vias (TSV) of a 3-dimensional stacked IC. A ring oscillator with TSV as load is implemented on the IC for testing and its frequency and duty cycle are analyzed for fault diagnosis. Authors are Shang, Tan, Li, Fan and Zeng from Guilin University of Electronic Technology, Guilin, China.

The final contributionis a *JETTA Letter* by Smith from Nelson Mandela University, Port Elizabeth, South Africa. The article documents experimental evaluation of the single event upset (SEU) suppression capability of an AND-OR-multiplexer filter.

Nearing the end of the year 2020, we cannot avoid noticing that testing, as ever, remains important. Also noticeable isa surge in remote and mobile electronics usage that is likely to continue.