Journal of Electronic Testing (2021) 37:285–286
https://doi.org/10.1007/s10836-021-05958-w

Editorial

Vishwani D. Agrawal[1]

Received: 29 June 2021 / Accepted: 29 June 2021 / Published online: 28 July 2021

This issue contains ten articles on topics of hardware security (3 articles), mixed-signal test (1), RF measurements (2), FinFET memory defects (2), and fault-tolerance (2).

Included among these are four papers from the IEEE 21st Latin-American Test Symposium (LATS), March 30 – April 2, 2020, Jatiúca (Maceió), Brazil. *JETTA* Editors Leticia M. B. Poehls and Serge Demidenko supervised the peer reviewing of the journal versions, appearing here as first, fourth, seventh and eighth papers.

First of the three hardware security papers examines the side channel analysis (SCA) attack vulnerability of a secret key decoding algorithm known as Montgomery ladder. The attack analyzes electromagnetic traces of the FPGA executing the algorithm. The vulnerability is found to increase as the execution frequency is raised. Reporting theoretical and experimental results are authors Kabin, Dyka, Klann, Aftowicz and Langendörfer from IHP – Leibniz Institut für innovative Mikroelektronik, Frankfurt (Oder), Germany.

Second paper addresses secret key generation from a physical unclonable function (PUF). Besides maintaining secrecy, the authors emphasize reducing the number of bits in the PUF hardware. Contributors are Bai and Yan from Lehigh University, Bethlehem, Philadelphia, USA.

Third paper analyzes circuit netlist for the presence of hardware Trojan (HT). Based upon controllability and transition probability, signals are classified as highly active (unlikely trigger for HT) or mostly inactive (possible triggers). The use of transition probability is shown to be beneficial in correctly predicting a signal to be a HT trigger. The authors are Mondal, Biswal, Mahalat, Roy and Sen from National Institute of Technology, Durgapur, India.

Fourth paper reports results of experiment and simulation for effects of radiation on an analog to digital converter (ADC). Linearity degradation, significant at low sampling rate, tends to decrease as sampling rate increases. The paper is authored by González, Costa, Machado, Kastensmidt and Balen from Federal University of Rio Grande do Sul, Porto Alegre, Brazil, Vaz and Gonçalez from Institute for Advance Studies, San Jose Campos, Brazil, Puchner from Cypress Semiconductor, Aerospace and Defense Department, San Jose, CA, USA, Medina from University of São Paulo, São Paulo, Brazil, and Bôas and Guazzelli from FEI University Center, São Bernardo do Campo, Brazil.

Next two papers are on RF measurements

Fifth paper examines the magnetic field radiated from an inductor, using measured data and finite element computation. Authors are Boukhari, Oumar, Capraro, Pietroy, Chatelon and Rousseau from National Institute of Sciences and Technologies of Abéché, Abéché, Chad, Polytechnic University of Mongo, Mongo, Chad, and University of Lyon, UJM-Saint-Etienne, CNRS, LabHC, UMR, Saint-Etienne, France.

Sixth paper gives an architecture for spectrum analyzer that measures the power spectral density (PSD) using a correlation filter. The main component of the system is a recursive second-order narrowband dynamic filter. Authors are Herasimov, Borysenko and Roshchupkin from Ivan Kozhedub Kharkiv National Air Force University, Kharkiv, Ukraine, and Hrabchak and Nastishin from Hetman Petro Sahaidachnyi National Army Academy, Lviv, Ukraine.

Next two papers are on finFET memory defects.

Seventh paper reports a study of open defects in a finFET-based SRAM cell. A short write time test is used to determine the effects on hold, read and write operations. Authors are Champac and Mesalles from National Institute for Astrophysics, Optics and Electronics—INAOE, Mexico, Villacorta from Polytechnic University of Aguascalientes, Mexico, and Vargas from Catholic University of Rio Grande do Sul—PUCRS, Brazil.

Continuing with the study of the finFET-based SRAM cell, the eighth paper provides results from modeling and simulation of single event upsets (SEU). Three cell types, high-density (HD), high performance (HP) and low voltage (LV), are examined and the HD cell is demonstrated to be most robust. Authors are Copetti, Medeiros, Taouil, Hamdioui, Bolzani Poehls and Balen, with affiliations into four organizations including Federal

✉ Vishwani D. Agrawal
agrawvd@auburn.edu

[1] Auburn University, Auburn, AL 36849, USA

University of Rio Grande do Sul, Porto Alegre, Brazil, RWTH Aachen University, Germany, Delft University of Technology, Delft, The Netherlands, and Pontifical Catholic University of Rio Grande do Sul, Porto Alegre, Brazil.

The last two papers are on fault-tolerance.

Ninth paper examines various crosstalk avoidance coding (CAC) schemes. An improved one-lambda coding (IOLC) is found to perform the best. The authors are Taali and Shirmohammadi from Shahid Rajaee Teacher Training University, Tehran, Iran.

Tenth paper proposes a fault-tolerance scheme for a graphics processing unit (GPU), which is often employed to find maximal eigenvalues of large sparce symmetric matrices of real numbers. To guard against inaccuracies caused by soft errors, the authors define an invariant property, for example, orthogonality among iteratively generated vectors in a specific computing algorithm. Authors are Loh, Saluja and Ramanathan from University of Wisconsin-Madison, Madison, Wisconsin, USA.