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Editorial

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Considering the rapid advances of the electronics technology it is not surprising that working engineers' knowledge, which centers around their expertise and experience, can easily get obsolete. Review, survey, and tutorial articles are excellent means to stay abreast. Besides, such articles are essential starting points for new researchers. The February issue of this year had a review on verification, "Pre-Silicon Verification Using Multi-FPGA Platforms: A Review," by Farooq and Mehrez (*JETTA*, volume 37, number 1, pages 7–24). Again, the first article in this issue is a review. We actively seek reviews, surveys, and tutorials on any topic within the scope of *JETTA*, especially those in emerging areas, so that we may continue to bring them to readers.

In this issue, we present ten articles, including one *JETTA Letter*. These are on memristive devices (a review), software reliability models, asynchronous circuit testing, hardware security, radiation effects, memory reliability, OPAMP aging, diagnosis by machine intelligence, and verification by theorem proving.

The first paper reviews defect handling in the manufacture of circuits implemented with memristor devices. Memristor is a resistive element whose resistance can be electrically set in low or high state. These devices offer an alternative to the CMOS technology due to manufacturing process similarity, high scalability and density, zero standby power, and capacity to implement high density memories as well as other digital functions. The article outlines a variety of manufacturing defects and equivalent fault models, pointing to similarities to and differences from CMOS. Authors presenting this work are Bolzani Poehls, Copetti and Gemmeke from RWTH Aachen University, Aachen, Germany, Fieback and Hamdioui from Delft University of Technology – TU Delft, Delft, The Netherlands, Hoffmann-Eifert and Menzel from Forschungszentrum Jülich Peter Grünberg Institute, Jülich, Germany, and Brum from Pontifical Catholic University of Rio Grande do Sul – PUCRS, Porto Alegre, Brazil.

Second paper outlines several software reliability models and presents a comparative study. Software testing is like hardware design verification where design errors, and not faults, are sought. The reliability of a program is assessed based on the rate of error exposition as the debugging progresses. In this work machine intelligence is used to recommend preferred reliability models. The paper is authored by Milovancevic and Vračar from University of Nis, Nis, Serbia, Dimov and Spasov from St. Kliment Ohridski University of Sofia, Sofia, Bulgaria, and Planić from Belgrade, Serbia.

Third paper proposes an asynchronous latch for scan test as well as for built-in self-test (BIST) of asynchronous circuits. These clock-less design for testability (DFT) approaches are shown to have lower area and power overheads in comparison to the conventional synchronous scan and BIST. The authors are Chen, Pai, Hsieh, Tseng, Chien-Mo, Liu and Chiu from National Taiwan University, Taipei, Taiwan.

Fourth paper addresses the problem of finding hardware Trojan (HT), i.e., locating the hardware maliciously placed on a chip without the knowledge of the designer or user. The authors present a new testability measure, named "sequential/combinational controllability and observability features for hardware Trojan detection (SC-COTD)," that when combined with a machine learning procedure, identifies the HT. Contributors of this research are Tebyanian, Mokhtarpour, and Shafieinejad from Tarbiat Modares University, Tehran, Iran.

Fifth paper discusses radiation hardening of electronic circuits to be used in aerospace applications. The authors first design a latch consisting of a self-recoverable cell, a 3-input C-element, and an inverter, which can tolerate a double node upset. A flip-flop, constructed with this latch has single and double node upset tolerances, but has reduced area, delay and power consumption compared to the available hardened designs. Contributors are Yan, Cao, Xu and Cui from Anhui University, Hefei, China, Ni from Anhui

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Polytechnic University, Wuhu, China, Girard from University of Montpellier/CNRS, Montpellier, France, and Wen from Kyushu Institute of Technology, Fukuoka, Japan.

Two papers that follow are about memories.

The sixth paper focuses on phase change memory (PCM), which is an emerging technology like the one discussed in the first article of this issue. The PCM exploits two states of material, amorphous (nonconducting) and crystalline (conducting), for representing 0 and 1 states of logic. The main idea put forward here is to initially use an error detection code and then selectively use the error correction code for a data word only after an error is detected. Significant reduction in hardware overhead is reported while degradation of reliability or repair rate is shown to be negligible. Authors are Lu and Li from National Taiwan University of Science and Technology, Taipei, Taiwan, Miyase from Kyushu Institute of Technology, Fukuoka, Japan, and Hsu and Sun from Industrial Technology Research Institute, Hsinchu, Taiwan.

Seventh paper gives a design for non-volatile static random-access memory (NVSRAM) cell using eight CMOS transistors and one oxygen-displacement RAM (OxRAM) element. This cell is about 35% larger and consumes 2.6% more power compared to a standard six transistor SRAM cell but retains its data when power is turned off. Authors of this article are Bazzi, Aziza and Moreau from Aix-Marseille University, Marseille, France, and Harb from International University of Beirut, Beirut, Lebanon.

Eighth paper examines the aging effect on an operational amplifier (OPAMP) caused by the bias temperature instability (BTI) phenomenon. BTI increases the threshold voltage of CMOS transistors. It is shown that for an OPAMP with open-loop configuration DC gain, cutoff frequency and slew rate significantly degrade with age. Also, the degradation rate becomes faster when operating temperature increases. For an OPAMP with negative feedback, DC gain remains almost unaffected while cutoff frequency shows degradation. The paper suggests a hardware monitor for performance degradation. Authors are Grossi and Omaña from University of Bologna, Bologna, Italy.

Ninth paper employs machine intelligence for run-time diagnosis of errors in the communication channels of a network on chip (NoC). A neural network (NN) hardware module is implemented on the NoC to receive on-line traffic data, and this NN is trained off-line using failure data. The paper concludes that a convolutional neural network (CNN) is highly effective in diagnosis and is better than a fully connected NN. The authors are Wang, Ouyang, Lu and Liang from Hefei University of Technology, China and Zhu from University of Texas at San Antonio, San Antonio, TX, USA.

Tenth paper, a *JETTA Letter*, describes a formal verification system for checking functional correctness of a digital system. A reader may need familiarity with concepts like formal specification, properties, assertions, model checking, and theorem proving for a full understanding of this work. However, simply said, the overall verification complexity becomes unmanageable as the design under verification (DUV) becomes large. The approach taken in the HVoC system is divide and conquer. The DUV is broken into modules to be verified independently before verifying the top-level interconnect. Authors are Minhas and Hasan from National University of Sciences and Technology (NUST), Islamabad, Pakistan, and Abed from Kuwait University.