Journal of Electronic Testing (2021) 37:569–570
https://doi.org/10.1007/s10836-021-05983-9

Editorial

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Received: 3 December 2021 / Accepted: 3 December 2021 / Published online: 9 December 2021

To begin this double issue of October and December 2021, I am pleased to announce the 2020 JETTA-TTTC Best Paper Award. The award selection committee was the same as last year and consisted of Xiaoqing Wen (Chair), Nicola Nicolici, Jennifer Dworak, Jiun-Lang Huang, and Erik Larsson. We congratulate the winning authors, Ankush Srivastava and Prokash Ghosh. Their paper, "A Novel Approach of Data Content Zeroization Under Memory Attacks," appeared in JETTA, Volume 36, Number 2, pages 147–167, April 2020. Yervant Zorian, TTTC President, announced the award at a plenary session during the International Test Conference (virtual meeting) on October 24. 2021. See the report in TTTC Newsletter in this issue.

This issue contains ten papers. The topics discussed are design for testability (DFT), hardware security, approximate circuits, hardware aging, soft errors, mixed-signal test, and interconnect test.

The first paper addresses the problem of reducing test data volume (TDV) and test application time (TAT) for circular scan (CS). In this type of testing, one orders test vectors to minimize bit conflicts between captured data and the next test vector. To achieve optimality in both TDV and TAT, the authors use a novel algorithm called modified shuffled shepherd optimization (MSSO) and demonstrate its benefits. The contributors of this research are Jayabalan from KPR Institute of Engineering and Technology, Coimbatore, India, Srinivas from Anurag University, Hyderabad, India, and Shajin and Rajesh from Anna University, India.

Continuing with the theme of DFT, the next paper proposes a new scan architecture. The commonly used serial-scan has low hardware overhead, but the area-inefficient random-access scan saves on power. The proposed joint scan combines the two into a configurable and multi-mode scan architecture to derive benefits from both. Authors are Tudu from Indian Institute of Technology (IIT) Tirupati, Ahlawat from Indian Institute of Technology (IIT) Jammu, and Shukla and Singh from Indian Institute of Technology (IIT) Bombay, India.

Third paper is on hardware security. Researchers model an in-vehicle communication network by an undirected weighted graph and use the well-known Dijkstra's shortest path algorithm to examine vulnerabilities of various modes of operation. Finally, a secure-by-design concept is proposed. The authors are Pethő and Khan from Budapest University of Technology and Economics, Budapest, Hungary, and Török from the Department of Automotive Technologies in Hungary.

Next, we have two papers on approximate circuits. There are two categories of such circuits. The first category consists of circuits that, despite faults, are suitable for certain functions. In the second category, hardware is intentionally trimmed such that the circuit remains usable for some intended functions. While the aim of the first category is to enhance yield, the second category has reduced area and power, and sometimes higher speed too.

In the fourth paper, authors Rao and Samundiswary from Pondicherry University, Puducherry, India, use a rounding-based approach to design an approximate multiplier. Their design demonstrates acceptable performance for image smoothing application with additional reduction in energy and delay over existing approximate designs.

Fifth paper discusses the first category of approximate circuits. Faults are rated for higher visibility at outputs. The first phase of testing is the usual one, after which only the failed circuits are retested in a second phase. This includes extra tests specifically aimed at the least visible faults to identify acceptable integrated circuits (AcICs) for certain error-tolerant applications. The authors make an interesting observation that about 30 to 40 percent faults in some circuits could be tolerable, suggesting future investigations on a possible over-testing situation. Contributors of this work are Jena and Deka from Indian Institute of Technology, Guwahati, India, and Biswas from Indian Institute of Technology, Bhilai, India.

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Sixth paper provides a method to monitor aging in sensors for activating security alarms. In general, aging is related to the NBTI (negative bias temperature instability) phenomenon that increases the threshold voltage of a PMOS device when it is conducting. However, measurement of age-related threshold voltage variation becomes unreliable due to factors like process variation and environmental effects. Researchers of this work develop differential calibration (DC) and use a machine learning approach for reliable estimation of aging. In DC the difference between two sensors, one heavily used and the other lightly used, as a function of time gives a reliable estimate of age. Contributors are Anik, Ebrahimabadi and Karimi from University of Maryland Baltimore County, Baltimore, MD, USA, and Danger and Guilley from Think Ahead Business Line of Secure-IC and Institut Polytechnique de Paris, France.

Seventh paper analyzes data transmission line for bit error rate (BER) in the presence of single event upset (SEU) pulses. A current source model is used to simulate the line. Results are verified by experiments in a cyclotron facility. Authors are Yoshikawa, Ishimaru and Iwata from Toyama Prefectural University, Toyama, Japan, and Mori and Kobayashi from Kyoto Institute of Technology, Kyoto, Japan.

Next come two papers on mixed-signal test. The eighth paper proposes mixed-signal circuit analysis in a somewhat digital mode. In a signal-flow model of the system, currents and voltages are represented by floating-point real numbers and analysis proceeds in an event-driven fashion. At least three hardware description languages (HDL) support this real number model (RNM). Basic advantage is the reduced computation time. Contributors of this work are Georgoulopoulos and Hatzopoulos from Aristotle University of Thessaloniki, Thessaloniki, Greece.

Ninth paper describes generation of diagnostic tests for a digital-to-analog converter (DAC) circuit using genetic algorithm (GA). Authors, X. Yang, C. Yang and H. Wang from University of Electronic Science and Technology of China, Chengdu, China, show how the tests are minimized for high fault detection and diagnostic coverages.

Tenth paper implements run-time built-in self-test (BIST) for bidirectional interconnects where crosstalk and electromigration may be relevant. BIST is activated periodically and hence monitors age or stress related effects as well. Authors are Sadeghi-Kohan and Hellebrand from University of Paderborn, Paderborn, Germany, and Wunderlich from University of Stuttgart, Stuttgart, Germany.

Let me end this final issue of 2021 with few closing remarks. As a result of the pandemic, we observed slowing down during the last two years. We saw reduction in the number of submissions and experienced increased processing time. We combined the last two issues of 2021 to stay on schedule. We used to hold the editorial board meeting annually at the International Test Conference. The conference went into virtual mode in 2020 and 2021, and the board did not meet for the first time since the inception of the journal in 1991. We hope to return to normal in 2022.