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Editorial

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In this issue, we have eight articles, including one *JETTA Letter*. These are on built-in self-test (BIST), approximate circuits, fault diagnosis, fault tolerance, analog circuits, and test equipment.

The first paper deals with test point insertion (TPI) for increasing fault coverage of logic built-in self-test (LBIST). In general, LBIST uses pseudorandom patterns that typically have low coverage of random pattern resistant (RPR) faults. TPI enhances the RPR fault coverage but is computationally expensive for large circuits. The authors use machine learning for TPI. Computing cost is kept low by using small artificial neural network (ANN) that only examines limited depth subcircuits around test points. These results are reported by Sun and Millican from Auburn University, Auburn, AL, USA.

Next, we have three papers on approximate circuits, typically arithmetic circuits used in error-resilient and real-time signal processing applications.

The second paper gives a survey of approximate multipliers and lists a number of future research directions. Authors are Anguraj and Krishnan from K. Ramakrishnan College of Technology, Trichy, Tamil Nadu, India, and Subramanian from S. Rangasamy College of Technology, Namakkal, Tamil Nadu, India.

Third paper continues the theme of approximate multiplier but takes a different approach. First, lower order input bits are trimmed and then the multiplier output is rounded off. Significant savings on area, delay, and energy are reported. Contributors are Raju from Vignan's Institute of Engineering for Women, Visakhapatnam, Andhra Pradesh, India, and Rao from Andhra University, Visakhapatnam, Andhra Pradesh, India.

Fourth paper observes that the sum and carry signals generated by an adder are strongly correlated. The two signals are mostly complementary and do not need to be independently generated. This reduces the amount of logic, though at the cost of making the result approximate. With these adders alternative multiplier designs are possible, showing reduced area, delay and power, and reasonable accuracy for signal processing. This paper is contributed by Chinthalgiri and Veeramachaneni from Gokaraju Rangaraju Institute of Engineering Technology, Hyderabad, India, Saranya from Dr. Mahalingam College of Engineering and Technology, Pollachi, Tamil Nadu, India, Jammu from GVP College of Engineering (A), Visakhapatnam, India, and Mahammad from Indian Institute of Information Technology, Design and Manufacturing (IIITDM), Kancheepuram, Chennai, India.

The fifth paper follows the satisfiability (SAT) approach for test generation. To overcome the high computational complexity, authors use machine learning (ML). A fully connected artificial neural network (ANN) named autoencoder is defined. Both unsupervised and supervised ML are employed, and the fault detection process continues through defect localization. Contributors of this research are Moness, Gaber and Ali from Minia University, Minia, Egypt, and Hussein from Effat University, Jeddah, Saudi Arabia.

The sixth paper is contributed by Dehbozorgi, Sabbaghi-Nadooshan and Kashaninia from the Central Tehran Branch, Islamic Azad University, Tehran, Iran. They address fault-tolerance of the processing-in-memory (PIM) architecture implemented with quantum-dot cellular automata (QCA). Focusing on the missing cell defect, they propose the use of ternary QCA, showing improved reliability of the PIM cell and logic gates.

Seventh paper provides a new op-amp model using a linear dopant drift TiO_2 memristor (LDDTM) emulator. Results of simulation and experiment demonstrate higher efficiency and improvements in performance parameters over conventional op-amp. Contributors of this work are Parlar and Almali from Van Yuzuncu Yil University, Van, Turkey.

Eighth paper, a *JETTA Letter*, examines a thermal sensor integrated circuit that is wirelessly powered and contains shielding and insulation for electromagnetic interference (EMI) and environmental conditions. The paper presents a

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low-cost, portable, configurable, and robust system to test this temperature sensing ASIC. Authors are Amin, Shahbaz, Jawed, Khan, Junaid, Kaleem, Siddiq, Warsi and Naveed from Karachi Institute of Economics and Technology, Karachi, Pakistan.