Depth-Optimized Reversible Circuit Synthesis

Mona Arabzadeh, Morteza Saheb Zamani, Mehdi Sedighi, Mehdi Saeedi

Abstract In this paper, simultaneous reduction of circuit depth and synthesis cost of reversible circuits in quantum technologies with limited interaction is addressed. We developed a cycle-based synthesis algorithm which uses negative controls and limited distance between gate lines. To improve circuit depth, a new parallel structure is introduced in which before synthesis a set of disjoint cycles are extracted from the input specification and distributed into some subsets. The cycles of each subset are synthesized independently on different sets of ancillae. Accordingly, each disjoint set can be synthesized by different synthesis methods. Our analysis shows that the best worst-case synthesis cost of reversible circuits in the linear nearest neighbor architecture is improved by the proposed approach. Our experimental results reveal the effectiveness of the proposed approach to reduce cost and circuit depth for several benchmarks.

Keywords Reversible logic · Synthesis · Linear nearest neighbor architecture · Circuit depth

1 Introduction

Boolean reversible circuits have attracted attention as components in several quantum algorithms including Shor's quantum factoring [1] and stabilizer circuits [2]. In the recent years, considerable efforts have been made to synthesize a Boolean reversible function by a set of quantum gates [3].

The proposed technologies for quantum computing suffer from practical limitations for implementation. For example, popular quantum technologies allow computation on a few qubits in a linear nearest neighbor (LNN) architecture where only adjacent qubits can interact [4]. Additionally, physical qubits are fragile and can hold their states only for a limited time, called *coherence time*, [5]. To reflect technological constraints in the synthesis stage, different technology-specific cost metrics have been introduced.

- Two-qubit cost is the number of two-qubit gates of any type and the number of one-qubit gates (reported separately) in a given circuit. The number of two-qubit gates for an n-qubit Toffoli gate (for $n \geq 3$) is estimated as 10n 25 [6]. Quantum cost (QC) is the number of NOT, CNOT, controlled-V and controlled-V[†] gates required to implement a given reversible function.
- Interaction cost is the distance between gate qubits for any two-qubit gate. Quantum circuit technologies with 1D, 2D and 3D interactions exist [4]. Interaction cost for a circuit is calculated by a summation over the interaction costs of its gates.
- Number of ancillae and garbage qubits reflect the limited number of qubits in the current quantum technologies.
- Depth is the largest number of elementary gates on any path from inputs to outputs in a circuit. Reducing circuit depth can increase coherence time.

Synthesis of reversible Boolean circuits has an exponential search space. Consequently, many heuristic algorithms have been proposed to consider the effects of quantum cost and two-qubit cost in the synthesis stage [7-10]. Additionally, several post-process optimization methods have been developed to improve

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quantum cost [8,11,6], interaction cost [12,13], and depth [14]. However, the number of algorithms which consider different parameters simultaneously — the focus of this work — is very limited.

Besides technological limitations, studying theoretical aspects of circuits with either limited interactions among qubits of gates or limited depth attracts interest in complexity theory. For example, NC^i is the class of decision problems solvable by a uniform family of Boolean circuits with polynomial size, depth of $O(\log^i n)$ and fan-in=2. QNC is the class of constant-depth quantum circuits without fanout gates [15].

In this paper, a synthesis algorithm for Boolean reversible circuits is proposed which uses a cycle-based strategy to synthesize circuits for the LNN architecture. The proposed technique leads to improved synthesis costs as compared to the best prior methods for several benchmarks. Moreover, a parallel structure for reversible Boolean circuits is presented which significantly reduces circuit depth with 2n ancillae. Overall, our circuits can be considered as depth-optimized reversible circuits for the LNN architecture.

This paper is organized as follows. Basic concepts are introduced in Section 2. Related synthesis and post-process optimization methods are reviewed in Section 3. The proposed cycle-based synthesis algorithm for the LNN architecture is described in Section 4. Section 5 presents a parallel structure to reduce circuit depth. Experimental results are reported in Section 6, and Section 7 concludes the paper.

2 Basic Concepts

In this section, preliminary concepts are briefly introduced. Further background can be found in [3].

Permutation Function. Let B be any set and define $f: B \to B$ as a one-to-one and onto transition function. The function f is a permutation function, as applying f to B leads to a set with the same elements of B and probably in a different order. If $B = \{1, 2, 3, ..., m\}$, there exist two elements b_i and b_j belonging to B such that $f(b_i) = b_j$. A k-cycle with length k is denoted as $(b_1, b_2, ..., b_k)$ which means that $f(b_1) = b_2, f(b_2) = b_3, ...,$ and $f(b_k) = b_1$. A given k-cycle $(b_1, b_2, ..., b_k)$ could be written in different ways, such as $(b_2, b_3, ..., b_k, b_1)$. Cycles c_1 and c_2 are called disjoint if they have no common members. Any permutation can be written uniquely, except for the order, as a product of disjoint cycles. If two cycles c_1 and c_2 are disjoint, they can commute, i.e., $c_1c_2 = c_2c_1$. A cycle with length two is called transposition. A cycle or a permutation is called even (odd) if it can be written as an even (odd) number of transpositions. When k-cycle is even (odd) then k is odd (even).

Reversible Function. An *n*-input, *n*-output, fully specified Boolean function $f: B \to B$ over variables $X = \{x_0, ..., x_{n-1}\}$ is called *reversible* if it maps each input pattern to a unique output pattern. Each reversible function can be considered as a permutation function. The added lines to a circuit are called *ancillae* and typically start out with a 0 or 1.

Reversible Gate. An n-input, n-output gate is reversible if it realizes a reversible function. A multiple-control Toffoli gate can be written as $C^m NOT(C; t)$, where $C = \{i_1, \ldots, i_m\}$ is the set of control lines, $t = \{j\}$ with $C \cap t = \emptyset$ is the target line and $0 \le i, j \le n-1$. A control line may be positive (negative) which means that if its value is one (zero), the value of the target is inverted. For m=0 and m=1, the gates are called NOT (N) and CNOT (C), respectively. For m=2, the gate is called $C^2 NOT$ or Toffoli (T). The SWAP(a,b) gate changes the value of two qubits a and b, and can be constructed by three CNOT gates C(a,b)C(b,a)C(a,b). The controlled-V (controlled-V[†]) gate changes the value of its target line using the transformation given by the matrix $V(V^{\dagger})$ if the control line has the value 1.

$$V = \frac{1+i}{2} \begin{bmatrix} 1 & -i \\ -i & 1 \end{bmatrix}, V^{\dagger} = \frac{1-i}{2} \begin{bmatrix} 1 & i \\ i & 1 \end{bmatrix}$$

3 Related Work

In this section, we review prior synthesis and optimization techniques that are used in this paper.

In [16], an NCT-based synthesis method is proposed which decomposes a given cycle into a set of transpositions. To implement an arbitrary transposition (a,b)(c,d) for distinct $a,b,c,d\neq 0$, 2^i , the authors introduced three subcircuits, namely π , κ_0 and π^{-1} (the inverse of π), where the κ_0 circuit, $C^{n-2}NOT(a_2,...,a_{n-1};a_0)$, implements a fixed transposition $(2^n-4,2^n-3)$ $(2^n-2,2^n-1)$. Accordingly, a synthesis algorithm was proposed to transform a,b,c and d to 2^n-4 , 2^n-3 , 2^n-2 and 2^n-1 , respectively. By cascading π , κ_0 and π^{-1} , an arbitrary transposition can be implemented with quantum cost 34n-64.

The NCT-based synthesis method in [16] was extensively improved in [10], k-cycle method hereafter. In the k-cycle method, a given cycle of length ≥ 6 is decomposed into a set of cycles of lengths < 6, called elementary cycles. Next, a set of synthesis algorithms was proposed to synthesize different elementary cycles,

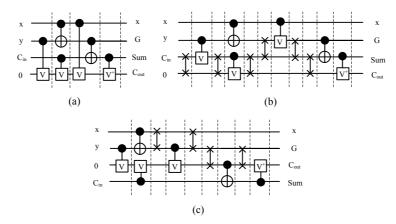


Fig. 1 (a) 3-input reversible full adder with optimal depth 4 [14], (b) the circuit in (a) after inserting SWAP gates and (c) reducing the number of SWAP gates by [12].

i.e., a pair of 2-cycles, a single 3-cycle, a pair of 3-cycles, a single 5-cycle, a pair of 5-cycles, a single 2-cycle (4-cycle) followed by a single 4-cycle (2-cycle) and a pair of 4-cycles. Similar to [16], 0 and 2^i terms are fixed before synthesis because their effect on their synthesis results is negligible [10]. NCT gates with positive controls are used in both [16] and [10]. The effect of decomposition on the result of [10] was considered in [17] where a cycle-assignment technique based on graph matching was proposed. The worst-case quantum cost for synthesizing an arbitrary reversible function on n lines is $8.5n2^n + o(2^n)$ in [10].

In [14], the authors introduced a post-process optimization algorithm to reduce the depth of a given quantum circuit. To achieve this, a set of circuit templates (circuit identities) was proposed to reduce quantum cost and circuit depth. The suggested templates are applied to change either gate locations or control/target positions in a subcircuit to parallelize more gates. The introduced templates were used by a greedy algorithm which starts from gate i and traverses the gates afterwards. At each step, the algorithm moves gates to left whenever possible and applies templates to check whether other gates can be moved to left or not. If no change is possible, it starts the same process from gate i + 1.

In [12], a synthesis flow was proposed to improve the interaction cost of a given quantum circuit. The authors studied the exact synthesis of some small gates for the LNN architecture. The proposed optimal circuits are used to simplify larger circuits. Besides, some circuit templates are introduced to reduce the number of SWAP gates. Finally, local and global reordering of input qubits are considered to reorder gate qubits for improving the interaction cost. The proposed techniques were consolidated in a unified design flow to implement a given circuit with arbitrary interactions for architectures with limited interactions.

Fig. 1-a shows a 3-input full adder with depth 4 [14] and six elementary gates. Actually, depth 4 is optimal since four qubits are involved in the fourth qubit [14]. Fig. 1-b shows the same circuit after inserting SWAP gates to make the gate qubits adjacent with QC=24 and depth=23. Fig. 1-c illustrates the same circuit after applying the method in [12] for reducing the number of SWAP gates where QC=18 and depth=17.

4 The Proposed Cycle-Based Synthesis Method for Interaction Cost

The main contribution of [10] is to propose a cycle-based synthesis approach with the primary focus on quantum cost as the sole metric considered. However, another important implementational constraint, namely interaction cost, is considered besides the quantum cost in our proposed cycle-based method in this section. To do that, we improve the k-cycle method by using negative controls and adapting the synthesis algorithms of elementary cycles to the LNN architecture. Particularly, two new elementary odd cycles, a 2-cycle and a 4-cycle, are included to improve quantum cost. These odd cycles are synthesized as a pair of 2-cycles and a pair of 4-cycles in [10] with one ancilla. Odd cycles need one ancilla in the NCT library for the implementation [16]. In our experiments, we used this ancilla for the decomposition of complex gates into elementary gates. Additionally, 0 and 2^i terms are not fixed before synthesis to be used in the proposed parallel structure as discussed in Section 5.

Negative controls can reduce the number of elementary gates in the κ_0 , π and π^{-1} circuits both with and without considering nearest neighbor restriction. Multiple-control Toffoli gates with at least one positive control can be simulated as efficiently as complex Toffoli gates with only positive controls [14]. By using

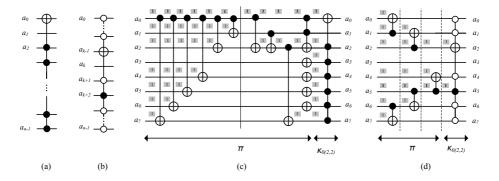


Fig. 2 (a) The $\kappa_{0(2,2)}$ circuit in [16,10]. (b) The proposed $\kappa_{0(2,2)}$ circuit. Each control at position $i, 0 \le i \le n-1, i \ne k+2$ is negative. (c) An example of π circuit in [10]. a_0 is used to control CNOTs in the first part. The second subcircuit is the circuit in [10, Theorem 3.1]. (d) An example of π circuit in the proposed method. Here, k=3. Refer to Table 1.

Algorithm 1: Gate selection in the π circuit

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Input:
  L n-bit input terms. Bit value at position i of the j-th input term is b_{(i,j)}.
  L n-bit \kappa_0 terms. Bit value at position i of the j-th \kappa_0 term is b_{(i,j)}^{\kappa_0}.
  Pivot is the boldfaced position in the intermediate terms in Table 1.
Output: The \pi circuit.
for i in 0 to L do
    if b_{(i,Pivot)} \neq 1 then
         Set b_{(i,Pivot)}=1 by either a CNOT or a Toffoli gate;
    for j in 0 to Pivot do
         if b_{(i,j)} \neq b_{(i,j)}^{\kappa_0} then
              Find a position p: b_{(i,p)} = 1, b_{(k,p)} \neq 1 \ (k < i), |p - j| is the minimum possible value, and p \leq Pivot;
              Apply CNOT(p;j);
         end
    end
          j in n-1 to Pivot+1 do
    for
         if b_{(i,j)} \neq b_{(i,j)}^{\kappa_0} then
              Find a position p: b_{(i,p)} = 1, b_{(k,p)} \neq 1 \ (k < i), |p-j| is the minimum possible value, and p \geq Pivot;
              Apply CNOT(p;j);
         end
    end
end
```

CNOT and Toffoli gates with negative controls, one may not fix 0 and 2^i terms before synthesis as compared with the methods in [16, 10].

Cycle Construction Length (CCL) is defined as the number of lines required to implement a given cycle of length L. In theory, the minimum CCL is $\log_2 L$. To implement the elementary cycles by NCT gates, at most two more lines are required in the proposed approach — one to avoid Toffoli gates without any positive control in the κ_0 circuit, and one to improve circuit cost in the π , π^{-1} circuits. Accordingly, we set $\mathrm{CCL}_{(2)}=2$, $\mathrm{CCL}_{(2,2)}=4$, $\mathrm{CCL}_{(3)}=3$, $\mathrm{CCL}_{(3,3)}=5$, $\mathrm{CCL}_{(4)}=4$, $\mathrm{CCL}_{(4,2)}=5$, $\mathrm{CCL}_{(4,4)}=5$, $\mathrm{CCL}_{(5)}=5$ and $\mathrm{CCL}_{(5,5)}=6$. For an n-line circuit, lines required to construct a given cycle, CCL in total, can be selected in $n\times(n-1)\times\ldots\times(n-\mathrm{CCL}-1)$ different ways. To improve interaction cost and depth we place the selected lines close to each other in the middle of the κ_0 circuit at positions $k, k\pm 1$ and $k\pm 2$ for $k=\lfloor n/2\rfloor$. Details are discussed later.

To synthesize a given elementary cycle, one needs to change input terms into the terms specified by the κ_0 circuit. This is done by converting the input terms into intermediate terms specified by the π circuit. Afterwards, the intermediate terms are transformed into κ_0 terms by a few specific gates, called static gates. In the proposed method, the control and target lines in the π circuit are selected such that interaction cost can be reduced. Since κ_0 cycles are constructed in the middle of the circuit and the intermediate terms are designed with at least one "1", as boldfaced in column Int. Terms in Table 1, it is possible to select control and target lines of each gate with length $\leq \lceil (n - \text{CCL})/2 + \text{CCL} \rceil$. Considering two SWAP gates with cost 6 leads to $\text{QC}_{LNN} \leq 3(n + \text{CCL})$ for each gate. To reduce circuit depth, the gates required to fix bit positions at the first half and the second half are applied in parallel. Algorithm 1 provides the details.

The $\kappa_{0(2,2)}$ circuits in [16,10] and the proposed $\kappa_{0(2,2)}$ circuit are shown in Fig. 2-a and Fig. 2-b, respectively. Fig. 2-c illustrates one example of the π circuit in [10]. The input term is "11110111" which should be changed to the second term in the $\kappa_{0(2,2)}$ circuit in [10], i.e., "11111101". This is done by a circuit with QC=16 and depth=11. In contrast, "11110111" should be changed to "00100100" in the proposed method. Fig. 2-d shows the π circuit with QC=5 and depth=3 based on Algorithm 1.

4.1 Building Blocks

In this section, direct synthesis of the suggested elementary cycles, i.e., (2), (2,2), (3), (3,3), (4,2), (4,4), (5), (5,5), is discussed. Fig. 3 illustrates the κ_0 circuits of all elementary cycles. We give a full description of the synthesis method for a pair of 2-cycles first.

(2,2)-synthesis: To change (a,b)(c,d) to $\kappa_{0(2,2)}$ terms:

- At most n NOT gates can be used to convert a to "0...1000...0". Other terms b, c, and d may be changed to new terms b', c' and d', respectively.
- At most one CNOT gate conditioned on either the *i*-th line $i\neq k+2$ (positive) or i=k+2 (negative) can be used to set the (k-1)-th bit of b'. Next, at most n-1 CNOT gates conditioned on the (k-1)-th bit can be applied to change the j-th bit of b' ($0 \le j \le n-1$, $j\neq k-1$) to "0...1001...0". c', and d' may be changed to new terms c'' and d''.
- At most one CNOT gate conditioned on either the *i-th* line $i\neq k+2$ (positive) or i=k+2 (negative) can be used to set the *k-th* bit of c''. Next, at most n-1 CNOT gates with positive control conditioned on the *k-th* bit can be applied to change the *j-th* bit of c'' ($0 \le j \le n-1, j \ne k$) to "0...1010...0". The last term d'' may be changed to a new term d'''.
- At most one CNOT gate conditioned on either the *i-th* line $i\neq k+2$ (positive) or i=k+2 (negative) can be used to set the (k+1)-th bit of d'''. Next, at most n-1 CNOT gates with positive control conditioned on the (k+1)-th bit can be applied to change the j-th bit of d''' ($0 \le j \le n-1, j\neq k+2$) to "0...1111...0".
- A Toffoli gate conditioned on the (k-1)-th and the k-th lines can be used to set the (k+1)-th line. Therefore, it changes "0...1111...0" to "0...1011...0".

Note that converting each term does not corrupt the previously fixed terms. The same number of gates are needed for the π^{-1} circuit. Accordingly, a total number of 8n+22 elementary gates are required for the π and π^{-1} circuits. The κ_0 circuit in Fig. 3-b implements $(2^{k+2}, 2^{k+2} + 2^{k-1})(2^{k+2} + 2^k, 2^{k+2} + 2^k + 2^{k-1})$ with cost 24n-88. Therefore, an arbitrary pair of 2-cycles (a,b)(c,d) can be implemented by at most 32n-66 elementary gates.

Following the above discussion for the (2,2)-synthesis method, details for the synthesis of other elementary cycles are given in Table 1. In this table, subscripts in column $Input\ Cycle(s)$ denote orders in considering each term. Intermediate terms are represented by binary expansions with LSB on the right and the underlined bit in the k-th position $(k=\lfloor\frac{n}{2}\rfloor)$. The boldfaced "1" is Pivot in Algorithm 1 for each term. The parenthesized pairs in column Max. Cost represent CNOT count with negative and positive controls, respectively. The numbers given in column Terms for the κ_0 circuit are bit positions with value "1" in binary representation. Table 2 reports the resulting quantum cost of each elementary cycle. As can be seen, the total number of elementary gates is improved by a linear factor in most cases. Considering the worst-case cost of 3(n+CCL) for each gate in the π and π^{-1} circuits in the LNN architecture and 6n-12 elementary gates (i.e., two chains of n-2 SWAP gates) for the κ_0 circuits leads to the results given in $Total\ Cost\ (LNN)$ column in Table 2.

4.2 Worst-Case Analysis

In this section, an upper bound on the number of gates in the proposed cycle-based method is calculated. To achieve this, let all terms of a truth table be involved in the input cycles to have a cycle with the maximum length 2^n for an n-input/n-output function. To convert a cycle with length>5 to a set of elementary cycles, we may have some repeated terms in non-disjoint cycles. As such, $2^n + a_r$ shows the maximum number of terms where a_r is the maximum number of repeated terms and can be estimated as $a_r = \frac{a_{r-1}+4}{5}$, $a_0 = \frac{2^n}{5}$ which results in $a_r = \frac{2^n}{5} + \sum_{i=2}^{\log_5(\frac{2^n-5}{4})} \frac{2^n+5^i-5}{5^i} = 2^{n-2} + \log_5(\frac{2^n-5}{4}) - \frac{9}{4}$. Theorem 1 discusses the maximum number of elementary gates in our approach.

Theorem 1 The maximum number of elementary gates for any permutation in the proposed approach is $9.4n2^n - 18.82^n + o(n^2)$ and $42.4n^22^n + o(n^3)$ without and with considering interaction cost, respectively.

Table 1 Direct synthesis of elementary cycles. Subscripts in the input cycles denote the orders in considering each term. The underlined bit in the k-th position $(k=\lfloor\frac{n}{2}\rfloor)$. The boldfaced "1" is Pivot in Algorithm 1. Numbers given for κ_0 terms are bit positions with "1" in the binary expansion.

I + C 1 ()		π or π^{-1} (reuit κ_0 Circuit						
Input Cycle(s)	Int. Terms	Max. Cost	Static Gates	Terms	Fig.				
/ 1)	(0100)	n N	-	(k+1)					
(a_1, b_2)	$(01\overline{1}0)$	n(1,n-1) C	_	(k-1)(k+1)	3-a				
(a_1, b_2)	(010000)	n N	-	(k+2)					
	(010010)	n(1,n-1) C	-	(k+2)(k-1)	0.1				
(c_3, d_4)	(010 1 00)	n(1,n-1) C	-	(k+2)(k)	3-b				
(3, 2,	(01 1 110)	n(1,n-1) C	T(k-1, k; k+1)	(k+2)(k)(k-1)					
	(00 <u>0</u> 10)	n N	-	(k-1)					
(a_1, b_2, c_3)	(0 1 010)	n(1,n-1) C	-	(k+1)(k-1)	3-с				
	(01 1 10)	n(1,n-1) C	-	(k+1)(k)(k-1)					
	(000 <u>0</u> 0 1 0)	n N	-	(k-2)					
	(0000110)	n(1,n-1) C	-	(k-1)(k-2)					
(a_1, b_2, c_3)	(000 1 110)	n(1,n-1) C	-	(k)(k-1)(k-2)	3-d				
(d_4, e_5, f_6)	(0 1 00010)	1 T, n-1 C	-	(k+2)(k-2)	5-u				
	(01 1 0110)	1 T, n-1 C	T(k-1, k+2; k+1)	(k+2)(k-1)(k-2)					
	(01 1 1110)	1 T, n-1 C	T(k, k+2; k+1)	(k+2)(k)(k-1)(k-2)					
	$(01\underline{0}000)$	n N	-	(k+2)					
(a_1, b_2, c_3, d_4)	(0100 1 0)	n(1,n-1) C	-	(k-1)(k+2)	3-е				
	(010100)	n(1,n-1) C	-	(k)(k+2)					
	(011110)	n(1,n-1) C	T(k-1,k;k+1)	(k-1)(k)(k+2)					
	(010 <u>0</u> 000)	n N	-	(k+2)					
(1 1)	(0100 1 00)	n(1,n-1) C	-	(k+2)(k-1)					
(a_1, b_2, c_3, d_4)	(0101000)	n(1,n-1) C	- (TD/L 1 L L 1 1)	(k+2)(k)	3-f				
(e_5, f_6)	(0111100)	n(1,n-1) C	T(k-1,k;k+1)	(k+2)(k)(k-1)					
	(01011 1 0) (01 1 0110)	n(1,n-1) C 1 T, $n-1$ C	T(k-2, k'; k+1)	(k+2)(k)(k-1)(k-2)					
	(010010)	<i>n</i> N	1(k-2,k',k+1)	(k+2)(k-1)(k-2) (k+2)					
	(010 <u>0</u> 000)	n(1,n-1) C		(k+2)(k-2)					
	(0100100)	$n(1,n-1) ext{ C}$ $n(1,n-1) ext{ C}$	_	(k+2)(k-2)					
(a_1, b_2, c_3, d_4)	(010 1 110)	$n(1,n-1) ext{ C}$ $n(1,n-1) ext{ C}$	_	(k+2)(k-1)(k-2)					
(e_5, f_6, g_7, h_8)	(0101000)	$n(1,n-1) ext{ C}$	T(k-2, k-1; k)	(k+2)(k-1)(k-2)	3-g				
(00, 70, 91, 100)	(01 1 1010)	1 T, n-1 C	T(k-2,k;k+1)	(k+2)(k)(k-2)					
	(01 1 1100)	1 T, n-1 C	T(k-1, k; k+1)	(k+2)(k)(k-1)					
	(01 1 11110)	n(1,n-1) C	T(k-2, k-1, k; k+1)	(k+2)(k)(k-1)(k-2)					
	(0100000)	n N	-	(k+2)					
	(01000 1 0)	n(1,n-1) C	-	(k+2)(k-2)					
$(a_1, b_4, c_2, d_3, e_5)$	(0100 1 00)	n(1,n-1) C	-	(k+2)(k-1)	3-h				
	(01 1 0110)	n(1,n-1) C	T(k-2, k-1; k+1)	(k+2)(k-1)(k-2)					
	(010 1 110)	n(1,n-1) C	-	(k+2)(k)(k-1)(k-2)					
	(0 1 0 <u>0</u> 0000)	n N	-	(k+2)					
	(010000 1 0)	n(1,n-1) C	-	(k+2)(k-3)					
	(01000 1 00)	n(1,n-1) C		(k+2)(k-2)					
,	(0100 1 110)	n(1,n-1) C	T(k-3, k-2; k-1)	(k+2)(k-2)(k-3)					
$(a_1, b_4, c_2, d_3, e_{10})$	(01010000)	n(1,n-1) C		(k+2)(k)	3-i				
$(f_5, g_8, h_6, i_7, j_9)$	(01110010)	1 T, n-1 C	T(k-3,k;k+1)	(k+2)(k)(k-3)					
	(01110100)	1 T, n-1 C	T(k-2,k;k+1)	(k+2)(k)(k-2)					
	(01110110)	n(1,n-1) C	T(k-2, k-1, k; k+1)	(k+2)(k)(k-2)(k-3)					
	(0101 1 110)	n(1,n-1) C	T(lo 1 lo/. lo + 1)	(k+2)(k)(k-1)(k-2)(k-3)					
	(01 1 01110)	1 T, n-1 C	T(k-1,k';k+1)	(k+2)(k-1)(k-2)(k-3)	I				

 ${\bf Table~2~Worst\text{-}case~costs~for~elementary~cycles}.$

			[10]					
EC	Length	κ_0	π , π^{-1}	Total Cost	Cost/Length	Total Cost (LNN)	Total Cost	Cost/Length
(2)	2	24n-64	2n+2	28n-60	14n-30	$145n^2$ -666 n +772	34n-30	17n-15
(2,2)	4	24n-88	4n+11	32n-66	8n-16.5	$147n^2$ -791 n +1100	34n-64	8.5n-16
(3)	3	24n-88	3n+4	30n-80	10n-26.7	$146n^2 - 804n + 1068$	32n-82	10.7n- 27.3
(3,3)	6	24n-112	6n + 26	36n-60	6n-10	$149n^2$ - $907n$ + 1474	38n-46	6.3n- 15.3
(4)	4	48n-152	4n+11	56n-130	14n-32.5	$291n^2$ - $1463n$ + 1868	50n-84	12.5n-21
(4,2)	6	36n-204	6n+14	48n-176	8n-29.4	$221n^2$ - $1615n$ + 2483	50n-122	8.3n- 20.3
(4,4)	8	36n-204	8n + 46	52n-112	6.5n-14	$223n^2$ - $1573n$ + 2678	56n-126	7n-15.7
(5)	5	48n-166	5n+13	58n-140	11.6n-28	$292n^2$ - $1537n$ + 2057	60n-130	12n-26
(5,5)	10	36n-204	10n + 57	56n-90	5.6n-9	$225n^2$ - $319n$ + 2790	64n-54	6.4n- 5.4

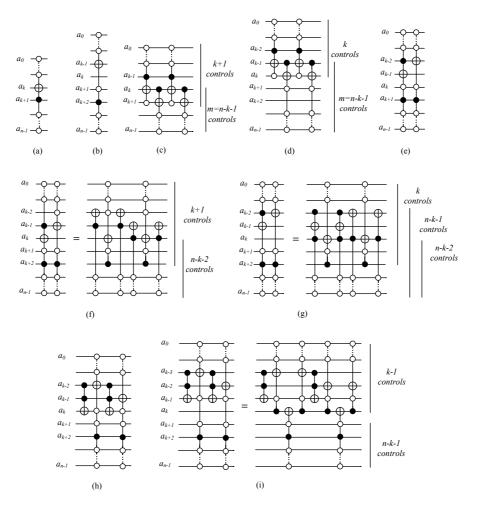


Fig. 3 The κ_0 circuit structures for different elementary cycles. The circuit structures for cycles (2,2), (3), (3,3), (4,2), (4,4), (5), and (5,5) are similar to those proposed in [10]. The new circuits for (2) and (4) besides the application of negative controls and the revised terms in the κ_0 circuits improve quantum cost and interaction cost.

Proof In Table 2, the column Cost/Length determines a cost needed for setting a term in each elementary cycle. To calculate the maximum cost, suppose at most one 3-cycle, one 4-cycle and one 5-cycle are included which can be synthesized by the related synthesis algorithms. All other terms are supposed to be synthesized as pairs of 2-cycles. Note that the number of elementary gates for fixing terms in a pair of 2-cycles is greater than any other pairs (See Table 2). The repeated terms in non-disjoint 5-cycles are synthesized by the (5,5)-cycle synthesis method.

Accordingly we will have, $3 \times Cost/Length_3 + 4 \times Cost/Length_4 + 5 \times Cost/Length_5 + (2^n - 12) \times Cost/Length_{2,2} + a_r \times Cost/Length_{5,5}$ which leads to $9.4n2^n - 18.8 \times 2^n + 2.8n^2 + 43.5n - 152.1$ elementary gates in the worst-case with arbitrary interaction and $42.4n^22^n + 11.3n^3 + 288.2n^2$ with limited interaction.

The worst-case quantum cost of [10] is $51n^22^n$ for architectures with limited interaction.

5 Synthesis with Parallel Structure

In this section, a parallel circuit structure is introduced for reversible logic that can be used to considerably reduce circuit depth of reversible circuits in most cases. The general idea is to copy input lines into k sets of zero-initialized ancillae, divide the input specification into k sets of disjoint cycles and then synthesize each set independently by using the prepared ancillae. The final results can be recovered by several CNOTs. It should be mentioned that adding ancillae has been previously used for quantum cost reduction in the synthesis and optimization methods [9,6]. In the proposed method, ancillae are used for the propose of depth reduction without considerable overhead on quantum cost, thanks to the specific form of input representation, i.e., cycle. Note that each cycle can be synthesized by a different synthesis method.

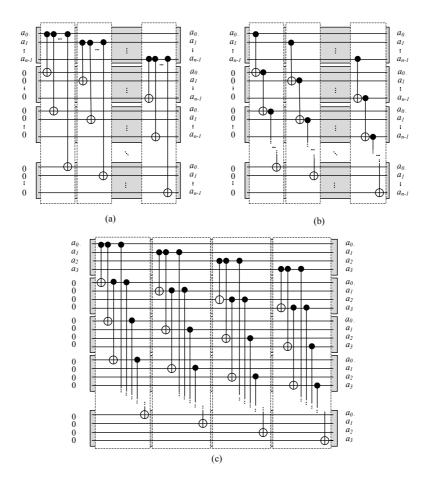


Fig. 4 (a) The input storing block with linear depth. (b) An alternative circuit structure with improved interaction cost and linear depth. (c) A logarithmic-depth circuit structure.

Input Storing Block. Copying an arbitrary quantum state is not possible in general but a Boolean value can be copied into a zero-initialized ancilla by a CNOT gate conditioned on the main line and targeted on the ancilla. For m n-line zero-initialized ancillae, the input storing block includes mn CNOT gates with constant depth m. Fig. 4-a shows the input storing block for a circuit with n main lines and m n-line ancillae. The interaction cost can be calculated as n(n-1)(1+2+...+m-1)=(1/2)nm(n-1)(m-1). Fig. 4-b illustrates another circuit structure with improved interaction cost, mn(n-1). Circuit depth in Fig. 4-a can be improved from linear factor to logarithmic factor $O(\log m)$ [15] as shown in Fig. 4-c. Thus, interaction cost can be calculated as $n(n-1)\sum_{i=0}^{\log_2 m-1} 2^{2i} = (1/2)n(n-1)(m^2-2)$.

Output Restoring Block. Since each subcircuit implements a set of disjoint cycles, for a given input combination, only one circuit (active) produces the results and the outputs of other subcircuits (inactive) are the same as the inputs. The number of inactive subcircuits is equal to the number of n-line ancillae registers, which is even. As such, XORing (by CNOT) the outputs of all subcircuits on the main lines cancels inputs and restores correct outputs at the main lines. Overall, for m n-line ancillae and m+1 sets of disjoint cycles, mn CNOTs with depth m are sufficient. Fig. 5-a illustrates the output restoring block for m n-line ancillae with interaction cost nm(n-1)(m-1). CNOT-circuit with common target can be implemented with logarithmic depth [15] as illustrated in Fig. 5-b for n=4 and m=4. In this case, interaction cost is $n(n-1)\sum_{i=0}^{\log_2 m-1} 2^i - 1/2^{i+1} = (1/2)nm(n-1)(2m+\log_2 m+2)$.

Theorem 2 Consider a given specification F on n lines written as a set of disjoint cycles $C_1C_2...C_m$ for an odd m. Assume that subcircuit L_i implements C_i . The specification F can be implemented with depth $O(\operatorname{depth}_{max}(L_i))$ in the presence of m n-line ancillae.

Proof Copying the input lines to m-1 n-line zero-initialized ancillae replicates inputs at the ancillae. Disjoint cycles commute. Hence, each subcircuit can be implemented on one register independently. The input storing/output restoring blocks have constant depth m. Therefore, circuit depth is dominated by the maximum depth of all subcircuits.

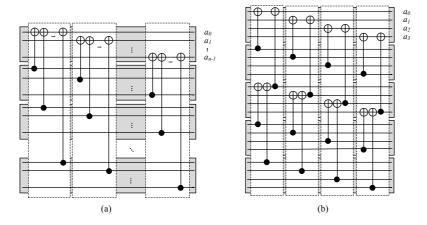


Fig. 5 (a) The output restoring block with linear depth. (b) The output restoring block with logarithmic depth for four main lines and four 4-line ancillae.

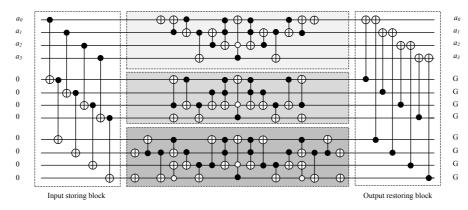


Fig. 6 An example of the proposed parallel cycle-based structure for a 4-line function.

A given specification may contain a set of disjoint cycles with exponential lengths, i.e., $O(2^n)$. In such cases, circuit depth cannot be further improved by Theorem 2. However, as will be shown in Section 6, circuit depth can be reduced considerably even with a small number of n-line ancillae. To efficiently employ the result of Theorem 2, one needs to determine disjoint cycle sets.

Example 1 Assume that the input cycles (1,3) (7,10) (0,4) (6,15) (2,8) (5,13) are given for a circuit with 4 lines. All cycles are elementary and no decomposition is required. Let 2 4-line ancillae be available and each pair of 2-cycles be assigned to one set, i.e., (1,3) (7,10) to set #1, (0,4) (6,15) to set #2 and (2,8) (5,13) to set #3. Applying the input storing block provides the input data on the added zero-initialized ancillae. Now, the proposed method in Section 4 can be applied for each cycle pair which leads to three subcircuits. To combine the results, one needs to add the output restoring block. Accordingly, total depth is equal to the maximum depth of the synthesized subcircuits (i.e., 33) plus 4 (2 for each input storing/output restoring block). Fig. 6 illustrates the result.

Cycle Distribution. Consider n elementary cycles and m register sets, including the input register. The problem is to assign disjoint cycles into different registers such that the total depth of the circuit in each register is minimized and the depths of the registers are almost equal. To achieve this goal, we modeled the cycle distribution problem as the bin packing problem with a few exceptions. In our modeling, registers are bins and cycles are objects. Each cycle is decomposed into a set of elementary cycles and cost values in Table 2 are used as the weights of elementary cycles. If the input permutation is odd, the permutation in one bin should be odd. Many heuristic algorithms have been developed to solve different variants of the bin packing problem. Examples include first fit and best fit algorithms.

¹ Bin packing problem is a combinatorial NP-hard problem in computational complexity theory in which objects of different weights must be packed into a finite number of bins of capacity W such that the number of used bins are minimized. Given a bin of size W and a list $w_1, ..., w_n$ of sizes of the items, one should find an integer B and a B-partition $S_1 \cup ... \cup S_B$ of $\{1, ..., n\}$ such that $\sum_{i \in S_k} w_i \leq W$ for all k = 1, ..., B. A solution is optimal if it has minimal B.

Benchmark	# of Cycles Before DCM After DCM After I								1 & DIST Depth				
Function	EC	nEC	(2)	(3)	(4)	(5)	set1	set2	set3	circ1	circ2	circ3	total
hwb8	48	16	36	-	28	16	26	28	26	1923	1995	1953	1999
hwb9	54	38	-	54	-	76	43	43	44	4344	4347	3988	4351
hwb10	228	26	152	-	-	154	101	103	102	9929	10058	9898	10062
hwb11	-	186	-	186	-	372	186	186	186	23862	23826	23827	23866
nth_prime7	-	5	1	3	1	28	19	6	8	1519	390	734	1523
nth_prime8	-	1	-	1	-	62	63	-	-	5852	-	-	5852
nth_prime9	1	3	2	-	1	125	122	4	2	13783	393	346	13787
nth_prime10	1	3	1	2	-	253	96	85	75	12115	10947	9329	12119
nth_prime11	-	6	2	-	1	507	315	36	159	46888	5470	23765	46892

Table 3 Benchmark specifications before and after decomposition.

To solve the problem, a best fit algorithm is developed which sorts c elementary cycles according to their maximum synthesis costs and proceeds one cycle at a time. To distribute cycles, the first cycle is selected and temporarily assigned to bin i for $1 \le i \le m$. Then, the total cost is calculated among all the bins and the cycle is permanently assigned to the bin which results in the lowest total cost. In the case of a tie, the bins are selected in sequence. The algorithm continues until all the cycles are assigned. Therefore, the total time complexity is $O(c \log c) + O(cm^2)$. At the end, the algorithm checks the permutation of each bin to make sure that at most one bin has an odd permutation. Odd permutations need one ancilla in the NCT library [16]. If more than one bin is found with an odd permutation (called odd bin), the algorithm moves the smallest odd cycle of the odd bin with maximum depth to the odd bin with the minimum depth. This can take O(m) time. After the changes, the involved bins should have even permutations. This process is continued until at most one bin with an odd permutation exists — this occurs when the input permutation is odd and at least m even permutations exist to fill all the bins. Altogether, the whole process has a time complexity of $O(c \log c) + O(cm^2)$.

6 Experimental Results

The proposed cycle-based synthesis method for the LNN architecture and the suggested parallel structure for reversible logic synthesis were implemented in C++ and all of the experiments were performed on an Intel Pentium IV 2.5GHz computer with 4GB memory. To evaluate the proposed synthesis method, some of the reversible benchmark functions from [18] were synthesized. The selection criteria for these benchmarks will be discussed later in this section and their specifications are given in Table 3 before and after decomposition. The decomposition approach of [10] is used in our method to decompose the input cycles into the proposed elementary cycles. The number of elementary cycles (EC) and non-elementary cycles (nEC) of each benchmark is reported is this table. After decomposition, all cycles are elementary with length<6. Note that [10] proposes the best prior synthesis algorithm for medium-size hwbN and N-th prime functions if no ancilla is available [18]. While hwbN functions can be implemented with a polynomial cost $O(n \log^2 n)$ if a logarithmic number of garbage bits $\lceil \log n \rceil + 1$ is available [18], the proposed approach is more general and can be applied to many reversible functions.

To evaluate the proposed parallel structure, the cycle-based algorithm of Section 4 was used for synthesizing each subset. Since the number of signals is limited in the current quantum technologies, the minimum number of ancillae (2 n-line registers) was used. Therefore, the number of input cycles should be >3 to have at least one cycle in each subset. In our experiments, the results of [14] were used for decomposing multiple-control Toffoli gates and calculating quantum cost for the gates with negative controls. Besides, the two-qubit cost model of [6] is used for evaluating the results. A naive SWAP insertion method and the method of [12] were used to evaluate the results for the LNN architecture. For the naive method, move and delete rules were applied on the synthesized circuits to remove redundant gates. To estimate circuit depth, the greedy level compaction algorithm of [14] was implemented without applying the templates. Table 4 and Table 5 report the quantum cost (QC), the two-qubit cost (2-qubit) and the depth (Depth) for the synthesized circuits without and with limited interaction. Since [10] does not target the limited interaction in the LNN architecture, we used the method of [12] on the results of [10] and ours to insert SWAP gates. Runtime of [10] and our method is less than one minute for the selected benchmarks. In the proposed method, this time includes the time required for applying the distribution procedure in the parallel structure and the time required for synthesis and applying the move and delete rules. In the parallel structure, due to the qubit reordering in [12], at most 3n(3n-1) SWAP gates are used between the input storing block, the subsets and the output restoring block to order lines.

Table 4 Comparison of the proposed approach and prior best results. #A is the number of ancillae. R and P are used for regular and parallel structures, respectively. The resulted circuits are available at http://ceit.aut.ac.ir/~arabzadeh/results/, and may be viewed with RCViewer+ [19].

Benchmark	m		The	Proposed	d Method			[10]		Improvement (%)		
Function	n	R/P	# A	QC	2-qubit	Depth	QC	2-qubit	Depth	QC	2-qubit	Depth
hwb8	8	R	-	6686	4468	5622	6940	5348	5442	3.6	16.4	-3.3
IIWDO	0	P	16	6964	4730	1999	0940			-0.3	11.5	63.2
hwb9	9	R	-	14474	10382	12054	16173	12479	12472	10.5	16.8	3.3
IIW D3	J	Р	18	15262	10764	4351	10175	12413	12412	5.6	13.7	65.1
hwb10	10	R	-	35298	23584	29751	35618	25453	27812	0.8	7.3	-6.9
IIW DIO	10	Р	20	35890	23874	10062	00010		2,012	-0.7	6.2	63.8
hwb11	11	R	-	86864	65260	71418	90745	71175	69763	4.2	8.3	-2.3
1111011		Р	22	87234	65442	23866	00.10	,11,0	00.00	3.8	8.0	65.7
nth_prime7	7	R	-	2888	2296	2473	3172	2841	2514	8.9	19.1	1.6
nen - primer		P	14	3100	2398	1523				2.2	15.5	39.4
nth_prime8	8	R	-	7016	5624	5852	7618	6622	5793	7.9	15.0	-1.0
p		P	-	-	-	-				-	-	-
nth_prime9	9	R	-	16820	11907	14285	17975 14	14076	13941	6.4	15.4	-2.4
- F		P	18	17507	12053	13787				2.6	14.3	1.1
nth_prime10	10	R	-	38843	27743	31924	40301	31841	31254	3.6	12.8	-2.1
		P	20	39317	27933	12119				2.4	12.2	61.2
nth_prime11	11	R	-	92863	67401	75668	95433	75474	72934	2.6	10.6	-3.7
		Р	22	93389	67677	46892				2.1	10.3	35.7
Average	Average								5.4	13.6	-1.9	
Tiverage										2.2	11.5	49.4

Table 5 Comparison of the proposed approach and the one in [10] with the nearest neighbor limitation. The improvement column compares the results after applying [12] on both methods. The resulted circuits are available at http://ceit.aut.ac.ir/~arabzadeh/results/, and may be viewed with RCViewer+ [19].

Benchmark	n				posed Met aive	hod +[19]	[10]-	+[12]	Improvement (%)		
Function	10	R/P	# A	QC	Depth	QC '	Depth	QC	Depth	QC	Depth	
hwb8	8	R P	- 16	36684 46788	32313 14758	31553 36045	20940 9248	36732	22720	14.0 1.8	7.8 59.2	
hwb9	9	R	-	87310	74676	77860	46958	91805	51181	15.1	8.2	
IIW 03	9	P	18	100228	31810	87389	19597	31000	01101	4.8	61.7	
hwb10	10	R P	20	$279496 \\ 291014$	248524 89021	202903 212616	112623 41479	228240	117893	11.1 6.8	4.4 64.8	
hwb11	11	R P	- 22	682182 685944	605294 205472	562817 569876	297986 104372	611843	307114	8.0 6.8	2.9 66.0	
nth_prime7	7	R P	- 14	12264 15106	10649 7734	10922 15897	9799 6930	15356	10130	28.8 -3.5	3.2 31.5	
nth_prime8	8	R P	-	35976	29975	30796	26920	42059	24574	26.7	-9.5 -	
nth_prime9	9	R P	- 18	91984 98686	76910 76020	90511 95362	54457 54850	99003	55737	8.5 3.6	2.2 1.5	
nth_prime10	10	R P	20	241538 250526	199996 79165	222865 228777	124122 49613	248901	137091	10.4 8.0	9.4 63.8	
nth_prime11	11	R P	- 22	654910 665132	577721 361756	576047 585165	308413 195500	625320	324005	7.8 6.4	4.8 39.6	
Average										14.6 4.4	3.8 48.6	

As can be seen in Table 5, the effect of the post-process method is more significant for [10] but altogether the results of the proposed LNN-based method are better than those of [10] after applying [12] on both methods. Notice that using negative controls does not allow to increase the quantum cost. For odd permutations, one more ancilla should be added. The two-qubit costs are compared in Table 4 and the results show 13.6% and 11.5% improvement on average for the regular and parallel structures, respectively. In the parallel structure, the average depth improvement of the N-th prime benchmarks is less than that of hwbN functions since the input cycles of those functions are unstructured with different cycle lengths which result in unbalanced subsets after distribution. Input cycle distributions after decomposition (DCM) and distribution (DIST) are reported in Table 3. For hwbN functions, applying the distribution method leads to 3 sets with almost the same numbers of elementary cycles. We report the circuit depth for each set along with the total depth after considering the effect of input storing and output restoring blocks in this table. As

reported in Table 3, function *nth_prime8* has one disjoint input cycle. Accordingly, the resulting elementary cycles should be assigned to one set by the proposed method.

In choosing the benchmark functions that were considered in this paper, the general guidelines presented in [10] and [3] were considered. These guidelines stipulate that one of the scenarios in which the cycle-based methods render significantly superior results is when the input function contains permutations without regular patterns such as hwbN, N-th prime [10] functions. For this reason, only the results of these functions are reported in this paper. As for other functions in [18], some are reported in [10] along with a discussion on their suitability for the cycle-based approach (like Permanent). To avoid being repetitive, we did not include this set in this paper. There are yet other benchmarks that include important arithmetic functions like adders, multipliers and group arithmetic (e.g., in Galois Fields). Since the proposed cycle-based synthesis method is a general synthesis approach, it may not produce interesting results compared to other approaches specifically developed for those benchmark functions.

7 Conclusion

In this paper, a synthesis approach is proposed in order to reduce logical depth for architectures with limited interactions which applies a cycle-based approach to synthesize a given specification. The proposed method focuses on the interaction cost and depth besides the traditional quantum cost metric as a multi-objective view in the large picture. To achieve this, we redesigned the elementary cycles in [10] with negative controls and limited interaction between gate lines. Moreover, a new parallel circuit structure was proposed for reversible logic in the presence of several ancillae registers. Altogether, the mentioned structure, which can be used with other synthesis methods, filling with the proposed cycle-based synthesis method for interaction cost leads to our whole flow for depth-optimized reversible circuit synthesis.

A given permutation is written as a set of disjoint cycles to be used in the proposed parallel circuit structure. Then, the resulting cycles are distributed among the available n-line registers based on the bin packing problem. The cycles are then synthesized on the assigned registers independently. Our experiments and analysis show the effectiveness of the proposed approach with and without the interaction cost limitations for the attempted benchmarks and in the worst-case.

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