Designing A One-Bit Coplanar QCA ALU Using A Novel Robust Area-Efficient Three-Input Majority Gate Design

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Designing A One-Bit Coplanar QCA ALU Using A Novel Robust Area-Efficient Three-Input Majority Gate Design

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Abstract

Quantum-dot Cellular Automata (QCA) which is a suitable alternative to conventional CMOS technology is susceptible to some defects in chemical synthesis and deposition phases of circuit fabrication. Besides, the majority gate is one of the most important primary gates for designing digital circuits in this emerging technology. Designing a fault-tolerant majority gate is one of the hot topics in QCA technology. Most previous works tried to improve the majority gate reliability by increasing the number of QCA cells which resulted in occupying more area. In this paper we propose a novel area-efficient three-input majority gate which can tolerate the single-cell omission and extra-cell deposition defects by 86% and 75%, respectively. The proposed majority gate consists of 11 simple QCA cells with 0.006 μm^2 and 1.62 e-002 MeV area and energy consumption, respectively. A complete fault tolerance analysis for our proposed majority gate against cell omission, extra-cell deposition, and cell displacement and misalignment defects is also provided. We design a fault-tolerant coplanar fulladder/fullsubtractor and a two-to-one multiplexer using the proposed majority gate and compare it with the same previous works. Simulation results from QCADesigner 2.0.3 and QCADesigner-E show that in all cases our proposed robust circuits can reduce the area consumption. Finally, we implement a fault tolerant coplanar one-bit ALU using the proposed circuits that can perform four logical and mathematical operations.

Keywords: Quantum-dot Cellular Automata, Majority gate, ALU, Reliability

1 Introduction

There has been a lot of research on finding a proper alternative to CMOS technology in the last decade. Although CMOS technology makes it possible to design more depth circuits by decreasing the size of transistor width, it has reached the physical restriction which results in some disorders like short-channel effects, design variation, and heat. Considering the high levels of performance, speed, and component density and the very low level of power consumption of quantum-dot cellular automata (QCA) technology, it has become a suitable alternative for CMOS technology [1–4].

QCA technology stores and transfers the information in cells containing quantum dots. Two free electrons sit in four quantum dots which are located in four corners of each cell. The free electrons are placed at diagonally opposite positions due to electrostatic Coulombic interactions between them. The two possible resulting polarizations define the logical state of the cell [5]. The process of storing and transferring data in QCA cells is based on the relative formation of the cell charges instead of electric flow which results in a field coupled technology (FCN) [6]. Metal-Island, Semiconductor, Magnetic, and Molecular are the four different types of QCA cell implementations [7].

QCA technology has some serious problems which are not already fixed completely due to its novelty. There are some defects in the chemical synthesis and deposition phases of QCA circuit design which decrease the reliability of these circuits [8, 9]. Cell misalignment, cellular displacement, cell omission, and deposition of extra cells are the four most probable defects that would occur in the deposition phase resulting in a drastic reduction in circuit efficiency. As a result, fault-tolerant logical QCA circuit design has become so momentous that researchers have done a bunch of studies about this since the last decade.

Three-input majority gate and inverter are the two fundamental logic gates in designing logical and computational circuits in QCA technology [7]. The efficiency of these two gates will result in the efficiency of the whole logical system. In this work, we design a novel robust area-efficient three-input majority gate with 11 simple QCA cells. Then we design a one-bit fulladder/fullsubtractor, a 2:1 multiplexer, and finally a one-bit ALU using the proposed three-input majority gate.

The remainder of this work is structured as follows. First, we review the QCA fundamentals as well as the different types of defects in QCA design in Section 2. In Section 3 we propose our fault-tolerant area-efficient three-input majority gate, verify its fault tolerance against common defects and compare it with already proposed designs. The computational circuits including a one-bit fulladder/fullsubtractor, a 2:1 multiplexer, and a one-bit ALU using our proposed structure are introduced and compared with the previous works in Section 4. Finally, we conclude the paper in Section 5.

2 Preliminaries

In this section, we first review the QCA fundamentals including QCA basic logic gates and clocking system. Then, we explain different types of QCA wire crossing. Finally, common QCA defects are discussed.

2.1 QCA fundamentals

Square-shaped QCA cells are the basic element of QCA circuits which interact via local field with each other and realize logical behavior [7]. Each QCA cell consists of four quantum dots which are located at the vertices of the square and able to confine electric charge [10]. Furthermore, the QCA cells contain a free and mobile pair of electrons which can tunnel between the adjacent dots [11]. Considering the Coulombic interaction between electrons in each cell, they only can place themselves at opposite corners of the cell which leads to two possible stable cell polarizations. Figure 1 shows P = -1 and P = +1 polarizations which define the logic '0' and logic '1', respectively [11].

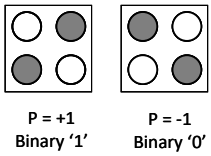


Fig. 1: QCA cell two polariziations.

To construct a binary wire, a chain of QCA cells should be placed next to each other to propagate the input to the output by Coulombic energy transaction between the electrons of the cells [12]. Figure 2 illustrates two types of QCA wires which are based on 45-degree (rotated) and 90-degree (simple) cells [13]. The rotated-based QCA wires (Figure 2.b) are usually employed to implement an inverter chain or for wire-crossing purposes [14].

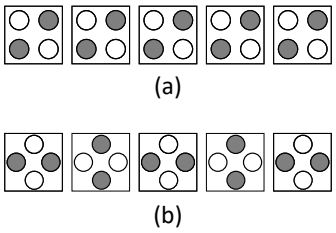


Fig. 2: Wires based on simple (a), and rotated (b) QCA cells.

The majority gate and inverter are the two basic gates of QCA technology that are employed to implement almost all the logical circuits [15]. Figure 3.a and 3.b show a basic three-input majority gate and an inverter, respectively. As it is shown in Figure 3.a a three-input majority gate consists of three input cells, one voter cell, and an output cell. A three-input majority gate functionality is given by Eq.1. The output value of the three-input majority gate becomes logic '1' only when two or more input values equal '1' [13].

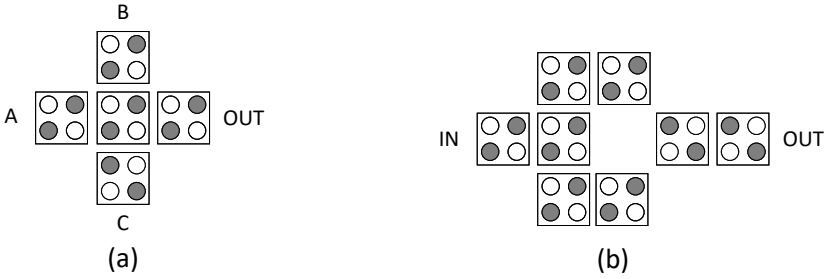


Fig. 3: Basic majority gate (a) and inverter (b) designed based on QCA technology.

$$OUT = AB + AC + BC \tag{1}$$

The QCA technology uses the clocking system in order to control the timing of the circuits and the information flow for creating pipelines and forcing logical circuits to stay in the quantum mechanics ground state [7]. A QCA clocking zone is a group of QCA cells which are controlled by the same clock. Four clocking zones are available in QCA and each of them has four phases. Figure 4 illustrates the QCA clock phases named Switch, Hold, Release and Relax [16]. In the Switch phase, the potential barrier among quantum dots is gone up and cells begin to polarize according to their input. In the Hold phase, the barrier is kept high. In the Release and Relax phases the barrier is lowered and remains lowered, respectively and cells become and remain unpolarized. The phase of a clock zone in a QCA design is 90 degrees different from the phase of the next and previous clock zones. For example, as it is shown in Figure 5, when clock 1 is in the switch case, clocks 2, 3 and 4 are in the relax, release and hold phases, respectively.

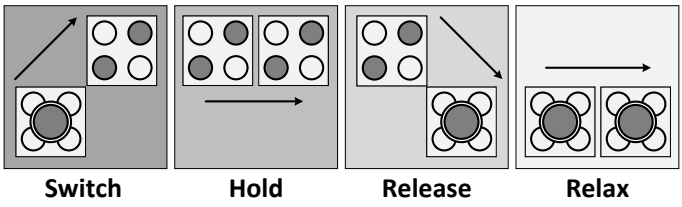


Fig. 4: Clock phases in QCA cells.

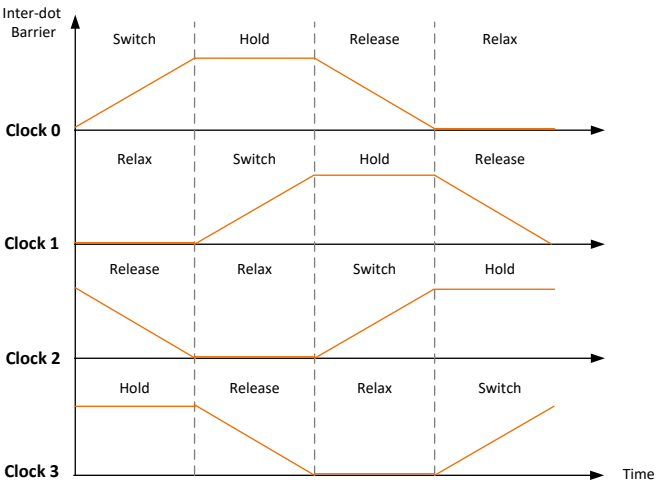


Fig. 5: Clock phases in neighbouring QCA cells.

2.2 Cross wire approaches

There are three different methods for crossing over QCA wires including multilayer, coplanar and logical coplanar [7]. Figure 6 shows these crossing methods. In the multilayer wire crossing (Figure 6.a), the crossing of two same type wires will be done in different layers [17]. The drawback of this type of wire crossing is that its implementation needs multiple active QCA layers on top of each other which have not been demonstrated before [7]. In the single-layer or coplanar wire crossing (Figure 6.b) which employs rotated QCA cells, two orthogonal wires cross each other without any effect on their operations [18]. The main drawback of this method is that because of employing two types of simple and rotated QCA cells, the implementation can easily be affected by fabrication and cross coupling defects [17]. Finally, the logical coplanar wire crossing (Figure 6.c) employs two groups of QCA cell arrays which have different clock phases. QCA cells in relax and release phases do not affect on their neighboring cells since they are unpolarized in these phases [19]. Therefore, those cells which are in the hold and relax phases can cross over cells which are in switch and release phases with no polarization effect [20]. This type of wire crossing, which is named logical coplanar wire crossing, is more reliable than simple coplanar wire crossing since it only employs simple QCA cells. It is also more area and energy efficient compared to multilayer wire crossing since it is implemented in one layer.

2.3 QCA defects

There are two types of defects in QCA design. One of them may occur during manufacturing QCA cells referred to as the synthesis step. Another may occur during placing the cells in the substrate which is referred to as the deposition

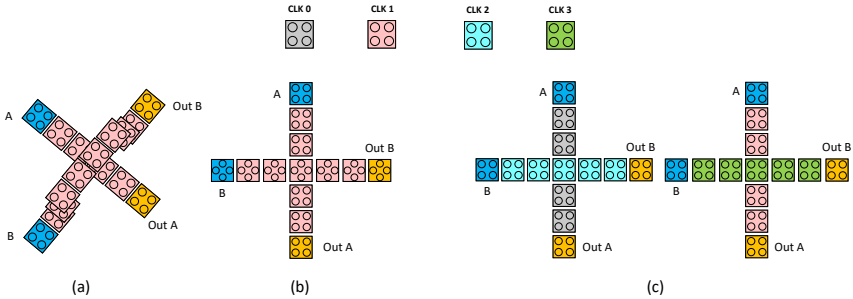


Fig. 6: QCA crossing wires types: multilayer (a), coplanar (b), and logical coplanar (c).

step [21]. Since QCA cell sizes are very small and need high accuracy in arranging, defects in the deposition step are more likely to occur [22, 23]. Common defects in the QCA deposition step are categorized into four groups as follows:

- *Cell omission*: This type of fault occurs when a cell is missing compared to the original fault-free design (Figure 7.a).
- *Cell displacement*: This type of fault occurs when a cell is misplaced within its original direction and the distance between the cell and other cells is reduced or increased (Figure 7.b).
- *Cell misalignment*: This type of fault occurs when a cell is not aligned correctly to its neighboring cells (Figure 7.c).
- *Extra cell*: This type of fault occurs when an additional cell is placed in the substrate (Figure 7.d).

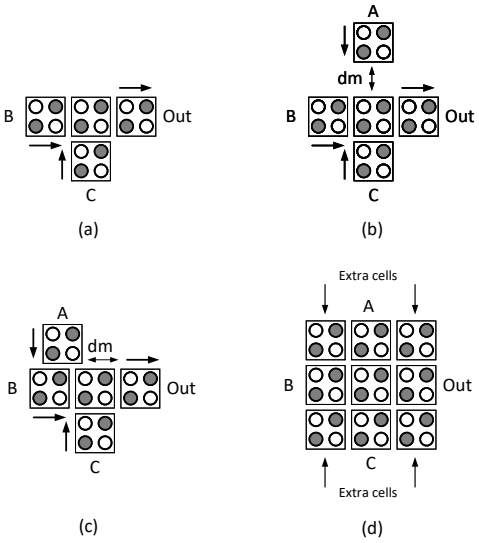


Fig. 7: QCA defects: Cell Omission (a), Cell Displacement (b), Cell Misalignment (c), and Extra Cell (d).

3 The proposed fault-tolerant three-input majority gate

Majority gates are one of the most important basic gates which are employed in QCA circuit designs. These gates always have an odd number of inputs and their only output is the majority vote of the inputs. Designing a fault-tolerant majority gate with optimized area consumption will result in area-efficient QCA circuits. In this section, we first propose a novel robust area-efficient three-input majority gate using simple QCA cells and verify its functionality with QCADesigner 2.0.3 simulator [24]. Then the simulation results including cell count, area, and number of clock cycles are provided using QCADesigner 2.0.3 simulator and the energy consumption is also reported using QCADesigner-E simulator [25]. After that, we study the fault tolerance of the proposed gate against different QCA defects such as cell omission, cell displacement, cell misalignment, and extra cell deposition. Finally, we compare the proposed design with those previous works which employ simple QCA cells in terms of area, cell count, energy consumption, number of clock cycles, and the amount of fault tolerance against single cell omission defect.

Figure 8 shows the layout of the proposed three-input majority gate. The output is calculated based on Eq.1. As it is shown the proposed gate consists of 11 simple QCA cells and the output is valid after one clock phase. The simulation results of the proposed structure which is performed by QCADesigner 2.0.3 is shown in Figure 9. The area and the energy consumption of our proposed three-input majority gate are 0.006 μm^2 and 1.62 e-002 MeV, respectively.

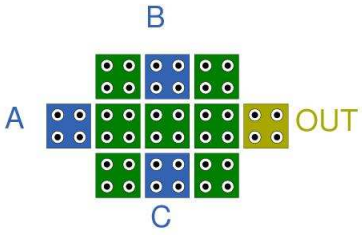


Fig. 8: The proposed three-input majority gate layout.

Two-input AND and OR gates can be implemented by fixing the polarization of one of the proposed three-input majority gate inputs to '0' and '1', respectively. Figure 10.a and Figure 10.b illustrate the proposed fault tolerant two-inputs AND and OR gates, respectively. The output of these three gates is verified by QCADesigner 2.0.3 which is shown in Figure 11.

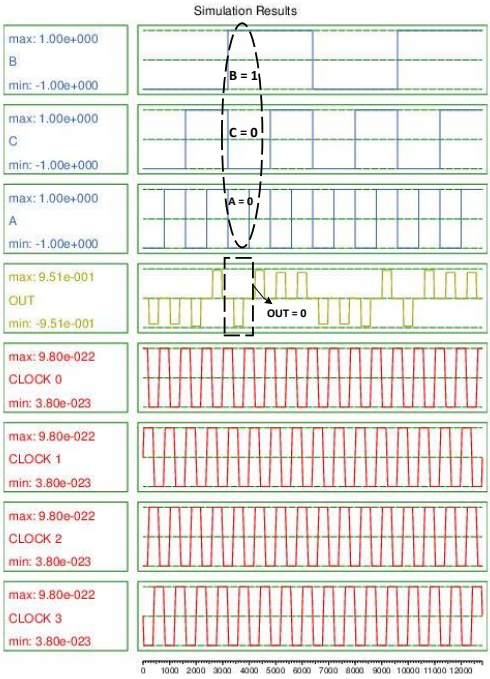


Fig. 9: The proposed three-input majority gate simulation results.

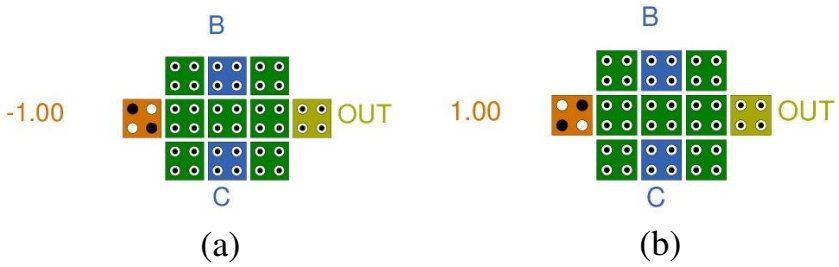


Fig. 10: The proposed and, or gate circuit layout.

3.1 The fault tolerance of the proposed majority gate against QCA defects

In this subsection, we study the fault tolerance of the proposed three-input majority gate against different QCA defects including single-cell omission, double-cell omission, cell displacement, and finally extra cell deposition.

To calculate the fault tolerance against cell omission defect which is one of the most important QCA defects, we consider all possible cases in which a single or double QCA cells of the proposed majority gate (excluding input/output cells) are omitted. Table 1 and Table 2 show the output results in each case of single and double cell omission, respectively. As Table 1 and Table 2 show,

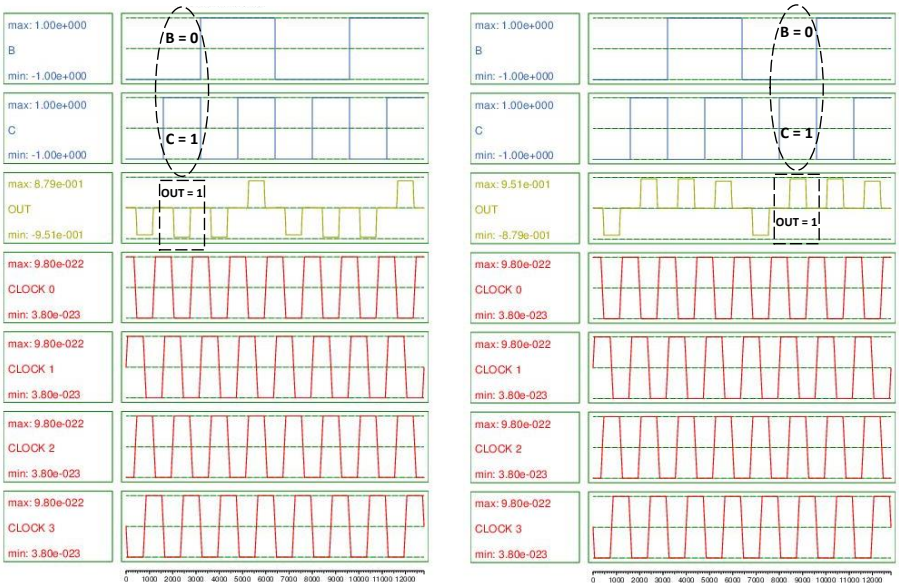


Fig. 11: The proposed and (a) , or (b) gate simulation results.

the majority gate output remains correct in many cases. In fact, the output in 86% and 43% of cases of single and double cell omission defects is correct, respectively.

Table 1: Single-cell omission analysis of the proposed majority gate based on cell numbers in Figure 12.

Omitted Cell	Output	Omitted Cell	Output
1	Correct	5	Incorrect
2	Correct	6	Correct
3	Correct	7	Correct
4	Correct		
Correct Rate = 86%			

Extra cell deposition is another important QCA defect that we consider it in fault tolerance calculations. To measure the fault tolerance of the proposed three-input majority gate against this defect, we consider all possible cases where an extra simple QCA cell is located around the proposed gate. Figure 12 shows all these extra cells which are labeled as E1 to E8. The output result

Table 2: Double-cell omission analysis of the proposed majority gate based on cell numbers in Figure 12.

Omitted Cells	Output	Omitted Cells	Output
1,2	Correct	3,4	Correct
1,3	Incorrect	3,5	Incorrect
1,4	Correct	3,6	Incorrect
1,5	Incorrect	3,7	Incorrect
1,6	Correct	4,5	Incorrect
1,7	Correct	4,6	Correct
2,3	Incorrect	4,7	Incorrect
2,4	Incorrect	5,6	Incorrect
2,5	Incorrect	5,7	Incorrect
2,6	Correct	6,7	Correct
2,7	Correct		
Correct Rate = 43%			

after depositing each extra cell is provided in Table 3. As it is shown the proposed gate output is correct in 75% of cases.

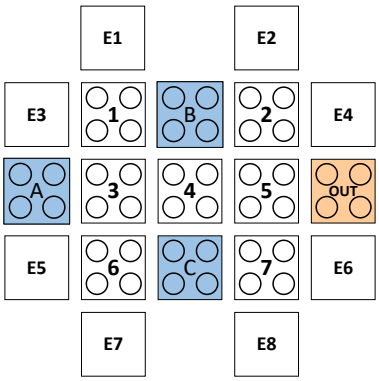


Fig. 12: Extra cells around the proposed majority gate.

For calculating the fault tolerance of the proposed gate against misalignment and displacement defects, the permitted range of displacement of all QCA cells in which the output remains correct is measured for four main sides (e.i. north, east, south, and west). Table 4 shows the mentioned permitted range. As it is shown, the proposed majority gate is highly tolerant against misalignment and displacement defects.

Table 3: Extra cell deposition analysis of the proposed majority gate based on cell labels in Figure 12.

Position	Output
E1	Correct
E2	Correct
E3	Correct
E4	Incorrect
E5	Correct
E6	Incorrect
E7	Correct
E8	Correct
Correct Rate = 75%	

Table 4: Displacement defect analysis of the proposed majority gate based on cell numbers in Figure 12.

Cell	North	South	West	East
A	≤ 7	≤ 7	≤ 36	-
B	≤ 3	-	-	-
C	-	≤ 3	-	-
OUT	≤ 4	≤ 4	-	≤ 6
1	∞	-	∞	-
2	∞	-	-	∞
6	-	∞	∞	-
7	-	∞	-	∞

3.2 Comparing the proposed three-input majority gate with previous works

The majority gate is one of the basic logic gates in QCA circuit design. Although there has been a lot of research in proposing an area/energy efficient majority gate with a high level of tolerance against QCA defects, it is still an open topic. We have proposed an area-efficient three-input majority gate using simple QCA cells. Since as mentioned before, those designs which employ both simple and rotated QCA cells can be affected by cross-coupling defects, in this subsection we will only compare our work to other area/energy efficient and robust three-input majority gates which are based on simple QCA cells.

Table 5 shows the comparison between the proposed majority gate and previous works in terms of the number of QCA cells, area consumption (μm^2), latency (number of clocks), energy consumption (MeV), and the gate tolerance against single-cell omission defect. As it is shown, our proposed robust majority gate is the most area-efficient design which employs the least number of QCA cells comparing to all the previous works.

Table 5: Three-input majority gates comparison.

	#Cell	Area (μm^2)	Latency (#Clocks)	Total Energy (MeV)	Cell Omission Defect Tolerance (%)
[26]	25	0.009	0.25	1.57 × e-002	80
[27]	37	0.032	0.25	9.32 × e-003	82
[28]	36	0.042	0.25	2.31 × e-002	93.8
[29]	20	0.014	0.5	1.96 × e-002	87
[30]	27	0.015	0.25	1.66 × e-002	100
[31]-1	13	0.006	0.25	1.76 × e-002	88
[31]-2	18	0.009	0.25	1.52 × e-002	91
[21]	13	0.009	0.25	3.82 × e-003	71
proposed	11	0.006	0.25	1.62 × e-002	86

4 Digital circuits based on the proposed three-input majority gate

In this section, we first design a fault-tolerant fulladder/fullsubtractor and a robust 2:1 multiplexer based on the proposed majority gate and compare them with same designs utilizing the best three area-efficient fault-tolerant majority gates which already have been proposed ([31]-1, [31]-2, [21]). Finally, we design a one-bit ALU based on our proposed basic circuits and compare it with previous ALU designs.

4.1 The proposed fulladder/fullsubtractor

Fulladder/fullsubtractor (FA/FS) is one of the most important building block in designing computational digital circuits like arithmetic multipliers, dividers and ALU [32–34]. In this subsection we design four different FA/FSs based on the three-input majority gates designed in [31]-1, [31]-2, [21], and our proposed one. Then we compare them in terms of the number of cells, area and energy consumptions.

The fulladder outputs named Sum and C_{out} are calculated based on equations Eq.2 and Eq.3, respectively. The equations for calculating fullsubtractor outputs named Sub and B_{out} are also provided in Eq.4 and Eq.5, respectively. In all these four equations A, B, and C are considered as inputs.

$$Sum = A \oplus B \oplus C \tag{2}$$

$$C_{out} = AB + AC + BC \tag{3}$$

$$Sub = A \oplus B \oplus C \tag{4}$$

$$B_{out} = A'B + A'C + BC \tag{5}$$

For designing an area-efficient fault-tolerant fulladder/fullsubtractor employing the proposed fault-tolerant three-input majority gate, we use the FA/FS combined circuit design which is introduced in [32]. The circuit outputs (i.e. Sum, Sub, C_{out} and B_{out}) can be computed using the equations Eq.6-8.

$$Sum/Sub = MV(MV'(A, B, C), A, MV(A', B, C)) \tag{6}$$

$$C_{out} = MV(A, B, C) \tag{7}$$

$$B_{out} = MV(A', B, C) \tag{8}$$

The fault-tolerant FA/FS circuit diagram employing our proposed three-input majority gate and its corresponding layout is illustrated in Figure 13.a and Figure 13.b, respectively, and the simulation output of the proposed circuit is also provided in Figure 14. As it is shown in Figure 13.b, the proposed layout consists of 99 simple QCA cells, and the outputs are ready after one clock cycle. The area and total energy consumption of this proposed circuit are also 0.09 μm^2 and 5.96 e-002 MeV, respectively. We calculate the reliability of the proposed FA/FS against single-cell omission defect. The results show that the Sum/Sub, C_{out} and B_{out} are 35%, 88% and 72% tolerant, respectively.

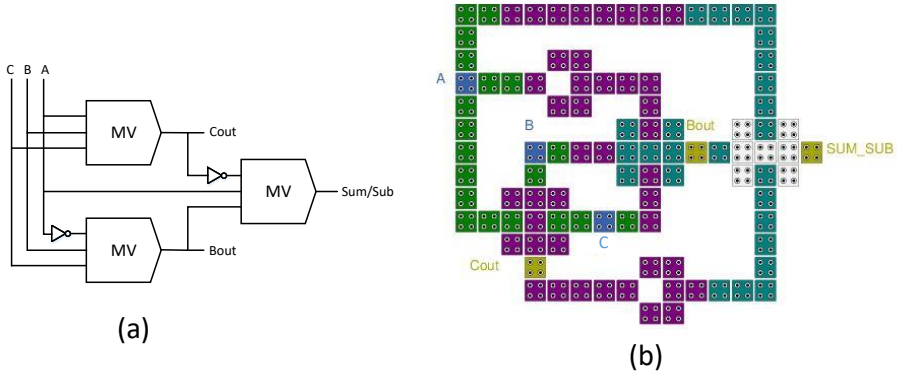


Fig. 13: Fulladder/fullsubtractor circuit diagram (a) and layout (b).

We compare our proposed fault-tolerant FA/FS with other three works which are designed using the three-input majority gates designed in [31]-1, [31]-2 and [21]. All the FA/FSs are designed based on [32] work which provides one of the best architectures for coplanar FA/FS. The comparison is made in terms of cell count, area, and energy consumption which is available in Table 6. As it is shown, the fault-tolerant FA/FS employing our proposed majority gate occupies less area in comparison to other designs.

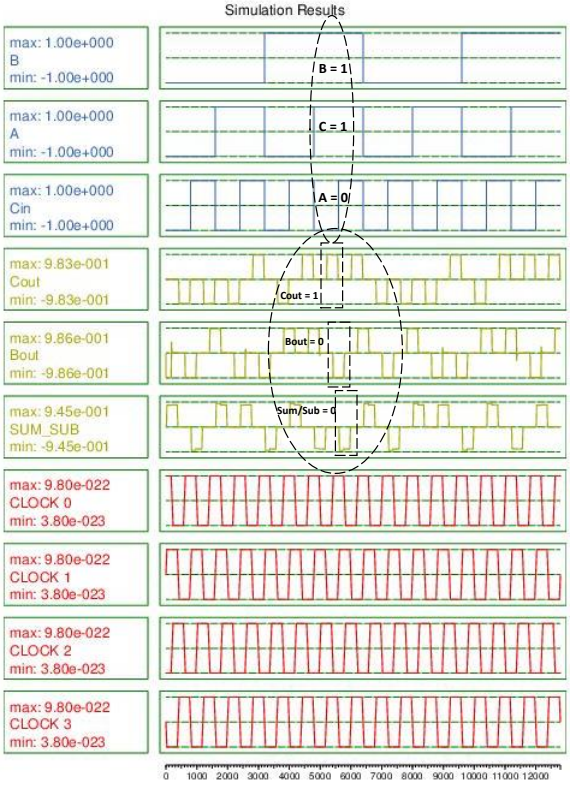


Fig. 14: The proposed fulladder/fullsubtractor simulation results.

Table 6: Fulladder/Fullsubtractors comparison.

Design	#Cells	Area (μm^2)	Energy (MeV)
[31]-1	127	0.13	5.65 e-002
[31]-2	146	0.16	7.24 e-002
[21]	116	0.12	3.98 e-002
Proposed	99	0.09	5.96 e-002

4.2 The proposed 2:1 multiplexer

Multiplexers are important digital circuits which are widely used in implementing different digital designs such as memory systems and FPGAs. In this subsection we design and compare four different 2:1 multiplexers employing three-input majority gates designed in [31]-1, [31]-2, [21] and our proposed one.

A 2:1 multiplexer can connect one of its two inputs to the only output by a single-bit selection bit. Figure 15.a shows a 2:1 multiplexer diagram where A and B are the inputs that can be transferred to the output (i.e. Out) based on the selection bit named S. The multiplexer output becomes A when the value

of S is Zero (i.e. S = '0'), and it becomes B when the value of S is One (i.e. S = '1'). The multiplexer output (i.e. Out) can be calculated using the equation Eq.9. Based on this equation three three-input majority gate and a not gate are needed for implementing a 2:1 multiplexer.

$$Out = (A.S') + (B.S) = MV(MV(A, S', 0), MV(B, S, 0), 1) \tag{9}$$

Figure 15.b illustrates the proposed fault-tolerant 2:1 multiplexer. The simulation output of the proposed circuit is also provided in Figure 16. As it is shown in Figure 15.b, the proposed design consists of 51 simple QCA cells and the circuit output is ready after a 0.75 clock cycle. Based on the simulation results of the QCADesigner 2.0.3 tool, our proposed multiplexer consumes 0.04 μm^2 area. The total energy consumption of our design is also 3.87 e-002 meV according to QCADesigner-E tool simulation results. The proposed design is also 43% tolerant against single-cell omission defects.

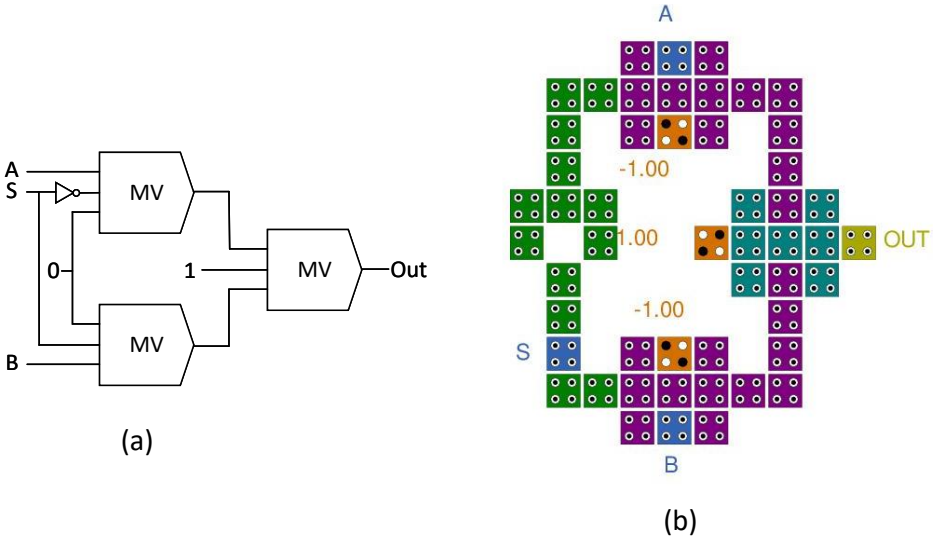


Fig. 15: Two-to-one multiplexer circuit diagram (a) and layout (b).

We compare our 2:1 multiplexer to three other works which are based on the three best majority gates that were mentioned above. Table 7. shows the comparison of these designs in terms of cell count, area and energy consumptions. As the simulation results show, the 2:1 multiplexer based on our proposed three-input majority gate is area-efficient in comparison to other three works.

4.3 The proposed one-bit ALU

The *Arithmetic Logic Unit* (ALU) which is one of the most important parts of the CPU, performs the basic arithmetic and logical operations. We design a new coplanar fault-tolerant ALU based on our proposed three-input majority

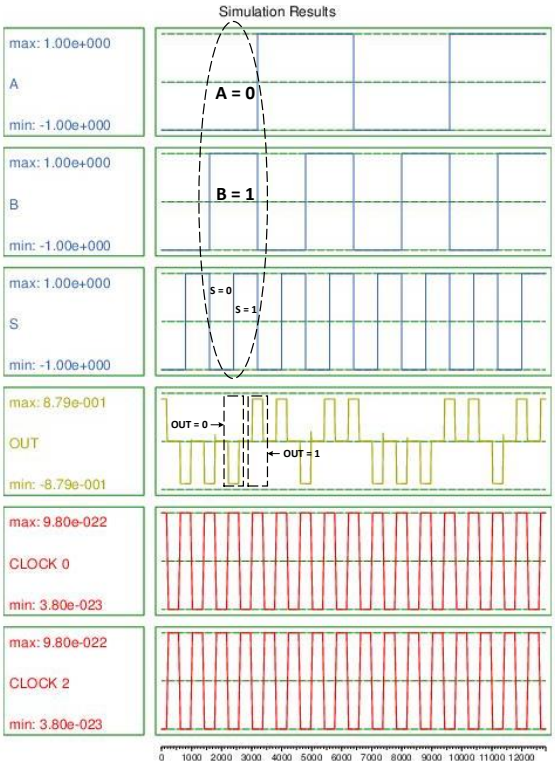


Fig. 16: The proposed two-to-one multiplexer simulation results.

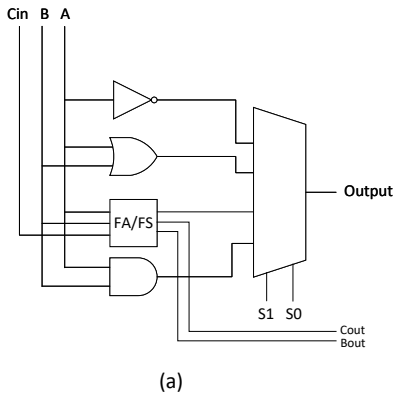
Table 7: Multiplexers comparison.

Design	#Cells	Area (μm^2)	Energy (MeV)
[31]-1	65	0.06	3.88 e-002
[31]-2	86	0.09	4.64 e-002
[21]	63	0.07	1.73 e-002
Proposed	51	0.04	3.87 e-002

gate and compare it with the previous designs. Figure17.a and Figure17.b shows the circuit diagram and truth table of the proposed ALU, respectively. As it is shown, the proposed ALU can perform four different functions. The QCA layout of the proposed fault-tolerant design is also provided in Figure 18.

Based on the proposed circuit layout in Figure 18, our coplanar ALU consists of 591 simple QCA cells employing logical wire crossing. The QCADesigner 2.0.3 simulation results show that the ALU consumes 1.25 μm^2 and the output is provided after 3.75 clock cycles.

We compare our design with previous works in Table8. As there is no unique structure for these ALUs, we compare them in terms of the number



S1	S0	Output	Function
0	0	A’	Not
0	1	A˅B	Or
1	0	A⊕B⊕Cin	Add/Subtract
1	1	A^B	And

(b)

Fig. 17: The proposed ALU circuit diagram (a) and truth table (b).

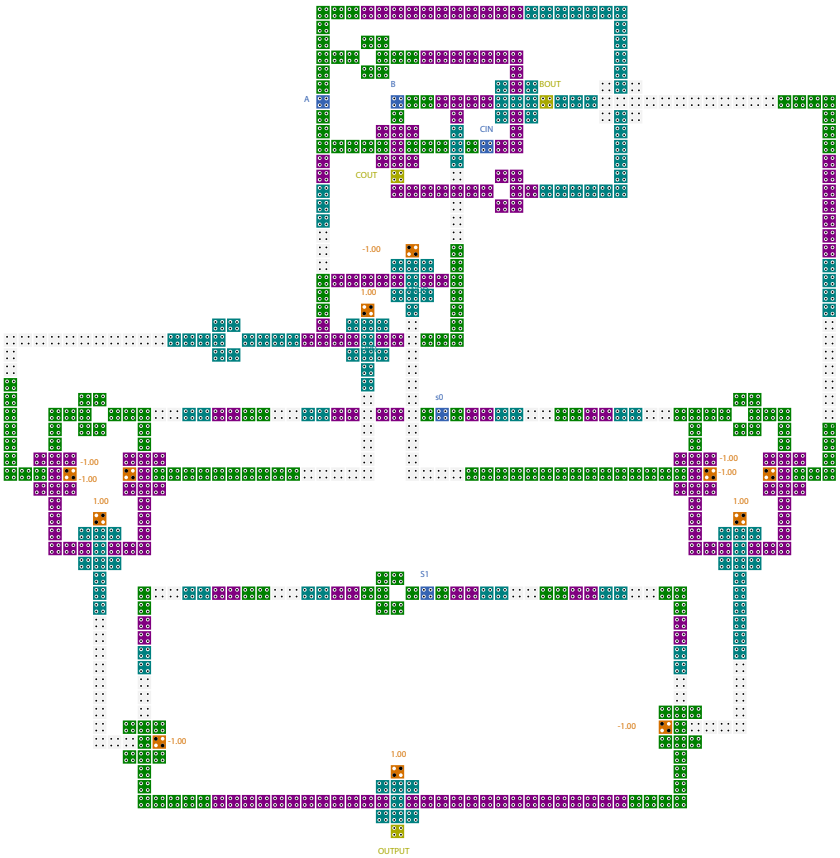


Fig. 18: The proposed ALU circuit QCA layout.

Table 8: ALUs comparison

Designs	Building Blocks	Layout	#Cells	Area (μm^2)	Latency (#Clocks)	Fault Tolerant	Cell Type
[35]	And, Or, Fulladder, Mux	Single Layer	900	-	-	No	Simple
[4]	And, Or, Xor, Fulladder, Mux	Multi Layers	-	0.78	3	Yes	Rotated
[5]	And, Or, Xor, Fulladder, Mux	Multi Layers	324	0.245	2.25	No	Simple
[34]	And, Or, Fulladder, Mux	Single Layer	625	1.34	3.75	Yes	Rotated
proposed	And, Or, Fulladder, Mux	Single Layer	591	1.25	3.75	Yes	Simple

of implemented building blocks, the number of cells, area consumption, the number of clock cycles that the output needs to be generated, the circuit layout structure, and the type of cells which are employed in design. As it is shown, compared to other designs, our proposed fault tolerant coplanar ALU is superior in terms of QCA cell count, and occupied area.

5 Conclusion and future works

One of the most important issues in QCA technology is the circuit reliability against defects in chemical synthesis and deposition phases of circuit fabrication. We have proposed a novel area-efficient fault tolerant three-input majority gate which has 11 simple QCA cells and occupies 0.006 μm^2 area with 1.62 e-002 MeV energy consumption. The proposed majority gate is highly tolerance against QCA defects and the most area-efficient design comparing to the previous works. A coplanar area-efficient fault tolerant fulladder/fullsubtractor and 2:1 multiplexer are also designed based on the proposed majority gate which in most cases could decrease the area consumption while improving the circuit fault tolerance in comparison to other similar designs. Using the proposed circuits, we designed a one-bit ALU which can perform AND, OR, NOT, and ADD/SUBTRACT operations. Simulation results show that our proposed ALU is also superior to other works. More area-efficient and robust complex circuits can be designed in future works by employing the proposed three-input majority gate.

Declarations

- Funding: No funds, grants, or other support was received.
- Conflict of interests: The authors have no relevant financial or non-financial interests to disclose.
- Ethics approval : Not applicable.
- Consent to participate : Not applicable.
- Consent for publication : Not applicable.
- Availability of data and materials : The simulation files including the proposed three-input majority gate, the proposed fulladder/fullsubtractor, the proposed 2:1 multiplexer, and the proposed ALU which are generated and/or analysed during the current study are available in the Google Drive repository.

- Code availability : Not applicable.
- Authors' contributions : Samira Riki and Fatemeh Serajeh Hassani contributed to the design and implementation of the research, to the analysis of the results and to the writing of the manuscript.

References

[1] Sherizadeh, R., Navimipour, N.J.: Designing a 2-to-4 decoder on nanoscale based on quantum-dot cellular automata for energy dissipation improving. Optik **158**, 477–489 (2018)

[2] Seyedi, S., Navimipour, N.J.: An optimized design of full adder based on nanoscale quantum-dot cellular automata. Optik **158**, 243–256 (2018)

[3] Seyedi, S., Navimipour, N.J.: Design and evaluation of a new structure for fault-tolerance full-adder based on quantum-dot cellular automata. Nano communication networks **16**, 1–9 (2018)

[4] Rahimpour Gadim, M., Jafari Navimipour, N.: A new three-level fault tolerance arithmetic and logic unit based on quantum dot cellular automata. Microsystem technologies **24**(2), 1295–1305 (2018)

[5] Babaie, S., Sadoghifar, A., Bahar, A.N.: Design of an efficient multilayer arithmetic logic unit in quantum-dot cellular automata (qca). IEEE Transactions on Circuits and Systems II: Express Briefs **66**(6), 963–967 (2018)

[6] Anderson, N.G., Bhanja, S.: Field-coupled nanocomputing. Lecture Notes in Computer Science (LNCS) **8280** (2014)

[7] Danehdaran, F., Khosroshahy, M.B., Navi, K., Bagherzadeh, N.: Design and power analysis of new coplanar one-bit full-adder cell in quantum-dot cellular automata. Journal of Low Power Electronics **14**(1), 38–48 (2018)

[8] Tahoori, M.B., Momenzadeh, M., Huang, J., Lombardi, F.: Defects and faults in quantum cellular automata at nano scale. In: 22nd IEEE VLSI Test Symposium, 2004. Proceedings., pp. 291–296 (2004). IEEE

[9] Gupta, N., Shrivastava, S., Patidar, N., Katiyal, S., Choudhary, K.: Design of one bit arithmetic logic unit (alu) in qca. Int. J. Comput. Appl. Eng. Sci **2**(3), 281–5 (2012)

[10] Tougaw, P.D., Lent, C.S.: Logical devices implemented using quantum cellular automata. Journal of Applied physics **75**(3), 1818–1825 (1994)

[11] Lent, C.S., Tougaw, P.D.: A device architecture for computing with quantum dots. Proceedings of the IEEE **85**(4), 541–557 (1997)

[12] Dysart, T.J.: Modeling of electrostatic qca wires. IEEE transactions on nanotechnology **12**(4), 553–560 (2013)

[13] Huang, J., Lombardi, F.: Design and Test of Digital Circuits by Quantum-dot Cellular Automata. Artech, London (2007)

[14] Safoev, N., Jeon, J.-C.: Low area complexity demultiplexer based on multilayer quantum-dot cellular automata. International Journal of Control and Automation **9**(12), 165–178 (2016)

[15] Safoev, N., Jeon, J.-C.: A novel controllable inverter and adder/subtractor in quantum-dot cellular automata using cell interaction based xor gate. Microelectronic Engineering **222**, 111197 (2020)

[16] Asfestani, M.N., Heikalabad, S.R.: A unique structure for the multiplexer in quantum-dot cellular automata to create a revolution in design of nanostructures. Physica B: Condensed Matter **512**, 91–99 (2017)

[17] Angizi, S., Alkaldy, E., Bagherzadeh, N., Navi, K.: Novel robust single layer wire crossing approach for exclusive or sum of products logic design with quantum-dot cellular automata. Journal of Low Power Electronics **10**(2), 259–271 (2014)

[18] Shin, S.-H., Jeon, J.-C., Yoo, K.-Y.: Wire-crossing technique on quantum-dot cellular automata. In: NGCIT2013, the 2nd International Conference on Next Generation Computer and Information Technology, pp. 52–57 (2013)

[19] Kim, K., Wu, K., Karri, R.: Quantum-dot cellular automata design guideline. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences **89**(6), 1607–1614 (2006)

[20] Shin, S.-H., Jeon, J.-C., Yoo, K.-Y.: Design of wire-crossing technique based on difference of cell state in quantum-dot cellular automata. International journal of Control and Automation **7**(4), 153–164 (2014)

[21] Huang, J., Momenzadeh, M., Lombardi, F.: On the tolerance to manufacturing defects in molecular qca tiles for processing-by-wire. Journal of Electronic Testing **23**(2), 163–174 (2007)

[22] Roohi, A., DeMara, R.F., Khoshavi, N.: Design and evaluation of an ultra-area-efficient fault-tolerant qca full adder. Microelectronics Journal **46**(6), 531–542 (2015)

[23] Momenzadeh, M., Huang, J., Tahoori, M.B., Lombardi, F.: Characterization, test, and logic synthesis of and-or-inverter (aoi) gate design for qca implementation. IEEE Transactions on Computer-Aided Design of

Integrated Circuits and Systems **24**(12), 1881–1893 (2005)

[24] Walus, K., Dysart, T.J., Jullien, G.A., Budiman, R.A.: Qcadesigner: A rapid design and simulation tool for quantum-dot cellular automata. IEEE transactions on nanotechnology **3**(1), 26–31 (2004)

[25] Torres, F.S., Wille, R., Niemann, P., Drechsler, R.: An energy-aware model for the logic synthesis of quantum-dot cellular automata. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems **37**(12), 3031–3041 (2018)

[26] Sun, M., Lv, H., Zhang, Y., Xie, G.: The fundamental primitives with fault-tolerance in quantum-dot cellular automata. Journal of Electronic Testing **34**(2), 109–122 (2018)

[27] Foroutan, S.A.H., Sabbaghi-Nadooshan, R., Mohammadi, M., Tavakoli, M.B.: Investigating multiple defects on a new fault-tolerant three-input qca majority gate. The Journal of Supercomputing **77**(8), 8305–8325 (2021)

[28] Wang, X., Xie, G., Deng, F., Quan, Y., Lü, H.: Design and comparison of new fault-tolerant majority gate based on quantum-dot cellular automata. Journal of Semiconductors **39**(8), 085001 (2018)

[29] Kumar, D., Mitra, D.: Design of a practical fault-tolerant adder in qca. Microelectronics Journal **53**, 90–104 (2016)

[30] Ahmadpour, S.-S., Mosleh, M.: A novel fault-tolerant multiplexer in quantum-dot cellular automata technology. The Journal of Supercomputing **74**(9), 4696–4716 (2018)

[31] Ahmadpour, S.-S., Mosleh, M.: New designs of fault-tolerant adders in quantum-dot cellular automata. Nano Communication Networks **19**, 10–25 (2019)

[32] Sadeghi, M., Navi, K., Dolatshahi, M.: Novel efficient full adder and full subtractor designs in quantum cellular automata. The Journal of Supercomputing **76**(3), 2191–2205 (2020)

[33] Oskouei, S.M., Ghaffari, A.: Designing a new reversible alu by qca for reducing occupation area. The Journal of Supercomputing **75**(8), 5118–5144 (2019)

[34] Ahmadpour, S.-S., Mosleh, M., Rasouli Heikalabad, S.: The design and implementation of a robust single-layer qca alu using a novel fault-tolerant three-input majority gate. The Journal of Supercomputing **76**(12), 10155–10185 (2020)

[35] Mustafa, M., Beigh, M.: A novel bit-slice design of quantum-dot cellular automata based arithmetic logic unit. Communications in Information Science and Management Engineering **3**(9), 455 (2013)