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EDITORIAL

Guest Editorial: Special Issue on SoC for Multimedia Networking (SiPS 2007)

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This special issue focuses on "SoC for Multimedia Networking," the theme of the 2007 IEEE Workshop on Signal Processing Systems (SiPS 2007) held in Shanghai, China in October 2007. This issue consists of highest quality papers selected from SiPS 2007 presentations with three major emphases centered on multimedia, networking, and architecture/SoC. For SiPS 2007, we were very pleased to receive a record number of 299 paper submissions from 36 countries. After a rigorous review and selection process, the final technical program consisted of 130 papers (43.48% acceptance rate) representing 25 different countries. These papers were arranged into nine lecture and 10 poster sessions (one special session), and the three-day technical program also included a student paper contest. The highlights of the workshop were the three keynote presentations by Magdy Bayoumi, Liang-Gee Chen, and Lajos Hanzo, each of them addressing state-of-the-art and future direction in these emerging areas.

To select high quality papers for publication in this special issue, authors of the papers that received high review scores were invited to submit expanded version of their papers to include more in-depth research work. Each of the papers was again carefully reviewed by at least three reviewers and the final decision for each was reached after careful discussion among the four guest editors. Finally, only seven papers passed through this rigorous process and were eventually accepted. They address some contemporary design and implementation issues in "SoC for Multimedia Networking" applications.

In multimedia communication, it is always challenging to achieve high received video quality under coding and communication constraints. Guo *et al.* presents a fast multi-hypothesis motion compensated filter for video denoising. The authors utilize a number of hypotheses (temporal predictions) to estimate the current pixel which is corrupted with noise. Song *et al.* proposes an adaptive pixel interpolation technique for spatial error concealment in block-based coding system, where a missing pixel in a corrupted block can be derived from four neighborhoods of the block through interpolation using a multiple prediction strategy. The design works effectively in consecutive block loss situation which is common in real-time video. Pantoja *et al.* addresses the use of super-resolution algorithm based on irregular sampling for video transcoding with resolution conversion. This is because in transcoding, quantization and other techniques could result in lower video output quality. The proposed method was applied to VC-1 to H.264 transcoding to show video quality improvement. The paper also includes a hardware feasibility study.

In system-on-chip designs, recent research have migrated from fairly simple single processor and memory designs to relatively complicated systems with multiple processors, on-chip memories, standard peripherals, and other functional blocks. Communication between these blocks becomes the dominant critical system path and performance bottleneck of system-on-chip designs. Network-on-chip architectures emerged as solutions for future system-on-chip communication architecture designs. Wang *et al.* presents a novel network-on-chip architecture, pipelining multi-channel central caching, to address the cost and communication latency/throughput of existing architectures. By embedding a central cache into every switch of the network, blocked head packets can be removed from the input buffers and stored in the caches temporally, thus alleviating the effect of head-of-line and

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deadlock problems and achieving higher network throughput and lower communication latency without higher area cost.

In DSP architecture design, reducing accelerator run-time overhead and memory bandwidth are two important components for research. Fine-grained accelerators are important for embedded signal processing and Boutellier *et al.* develops a methodology for applying flow-shop scheduling techniques to make effective, low-overhead use of fine-grained DSP accelerators; they demonstrate the methodology by applying it to MPEG-4 video decoding. Fischaber *et al.* explores how dataflow graph changes can be used to drive both on-chip and off-chip memory organizations and how these memory architectures can be mapped to a hardware implementation. By exploiting the data reuse inherent in many image processing algorithms and by creating memory hierarchies, off-chip memory bandwidth is reduced significantly from the original dataflow graph level specification of a motion estimation algorithm with a minimal increase in memory size. Analyses show a significant reduction in the delay between the memories and processing elements. Chuang *et al.* discusses architecture of fine grain scalability (FGS) encoder with low external memory bandwidth and low hardware cost. Significant bandwidth reduction can be attained by their proposed scan bucket algorithm, early context modeling with context reduction, and first scan pre-encoding. The hardware architecture is implemented by layer-wise hardware reuse. The authors also applied the techniques to real-time encode HDTV video with FGS enhancement layers.

We would like to sincerely thank the reviewers for their valuable comments that ensure the high quality of this special issue. We would like to especially thank the Editor-in-Chief Professor Sun-Yuan Kung for his guidance, and to the editorial staff of Springer, for their kind help and support. Thanks also go to all the authors for their high quality contributions. Finally, we thank the two IEEE technical committees (TCs), the Design and Implementation of Signal Processing Systems TC and the VLSI Systems and Applications TC, for their support and advice. We hope you enjoy the articles in this special issue as much as we do.

Xiaokang Yang received the B. S. degree from Xiamen University, Xiamen, China, in 1994, the M. S. degree from Chinese Academy of Sciences, Shanghai, China, in 1997, and the Ph.D. degree from Shanghai Jiao Tong University, Shanghai China, in 2000. He is currently a Professor and the Deputy Director of the Institute of Image Communication and Information Processing, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China. From August 2007 to July 2008, he visited the Institute for Computer Science, University of Freiburg, Germany, as an Alexander von Humboldt Research Fellow. From September 2000 to March 2002, he worked as a Research Fellow at the Centre for Signal Processing, Nanyang Technological University, Singapore. From April 2002 to October 2004, he was a Research Scientist in the Institute for Infocomm Research (I2R), Singapore. He has published over 130 refereed papers, and has filed 14 patents. His current research interests include visual processing and communication, media analysis and retrieval, and pattern recognition. He actively participates in the International Standards of MPEG and JVT. He received the Microsoft Young Professorship Award 2006, the Best Young Investigator Paper Award at IS&T/SPIE International Conference on Video Communication and Image Processing (VCIP2003) and awards from A-STAR and Tan Kah Kee foundations. He is currently a senior member of IEEE, a member of Design and Implementation of Signal Processing Systems (DISPS) Technical Committee of the IEEE Signal Processing Society and a member of Visual Signal Processing and Communications (VSPC) Technical Committee of the IEEE Circuits and Systems Society. He was the special session chair for Perceptual Visual Processing of IEEE ICME2006. He was the local co-chair of ChinaCom2007 and the technical program co-chair of IEEE SiPS2007.

Nam Ling received the B.Eng. degree in Electrical Engineering from the National University of Singapore, and the M.S. and Ph.D. degrees, both in Computer Engineering, from the University of Louisiana, Lafayette. He is currently a Full Professor of Computer Engineering and the Associate Dean for Research and Faculty Development for the School of Engineering, Santa Clara University (SCU), Santa Clara, California. He has served as Visiting Professor/Consultant/Scientist/Scholar to many institutions and as Collaborator/Consultant to several companies. He has more than 140 publications in the fields of video coding and systolic arrays. He is the primary author of the book Specification and Verification of Systolic Arrays. He and his team's fast motion estimation and Lagrange methods were both adopted into the H.264/MPEG-4 AVC video coding international standard and reference software. Prof. Ling is a recipient of the Arthur Vining Davis Junior Faculty Fellowship in 1991, the SCU Outstanding Achievement Award in 1992, the SCU Engineering Researcher of the Year Award in 1999, the SCU Award for Recent Achievement in Scholarship in 2002, the SCU President's Recognition Award in 2005, and the SCU Award for Sustained Excellence in Scholarship in 2007. He was named IEEE Distinguished Lecturer for 2002–2003 and 2007–2008. He also received the 2003 IEEE ICCE Best Paper Award

(First Place Winner) for the work on MPEG-4 face animation. He is an IEEE Fellow due to his contributions to video coding algorithms and architectures. He served as Keynote Speaker for IEEE APCCAS 2008 and VCVP 2008, and as major speaker and panelist for several other conferences and seminars. He will serve as Distinguished Invited Lecturer for IEEE ICIEA in 2010. Prof. Ling has served as the Chair of the IEEE Computer Society Technical Committee (TC) on Microprocessors and Microcomputers in 1993–1995 and the Chair of the IEEE Circuits and Systems Society Circuits and Systems for Communications TC in 2006–2008. He is also member of two other IEEE TCs (VSPC and DISPS). He served as an Associate Editor for the IEEE Transactions on Circuits and Systems I in 2002 and 2003 and was a Guest Editor for the Journal of VLSI Signal Processing Systems special issue in 2006. Prof. Ling was the General Chair for the IEEE Hot Chips Symposium in 1995, the General Co-Chair for VCVP in 2008, and the Technical Program Co-Chair for IEEE ISCAS in 2007, IEEE SiPS in 2000 and 2007, and IEEE DCV in 2002. He is currently a Technical Program Co-Chair for APSIPA ASC 2010. Prof. Ling was Track Co-Chair for IEEE ISCAS 2004–2006. He also served in the editorial boards of several technical journals, and served in program committees, organizing committees, and as session chair for many IEEE conferences. He has delivered more than 100 invited/distinguished/keynote colloquia in nine different countries.

Wenjun Zhang was born in Qingdao, China, in 1963. He received the B.S., M.S. and Ph.D. degrees in Electronic Engineering from Shanghai Jiao Tong University, Shanghai, China, in 1984, 1987 and 1989, respectively. From 1990 to 1993, he worked as a Postdoctoral Fellow at Philips Kommunikation Industrie AG in Nuremberg, Germany, where he was actively involved in developing HD-MAC (former European HDTV) system. He joined the Faculty of Shanghai Jiao Tong University in 1993 and became a full Professor at the Department of Electronic Engineering in 1995. As a team leader, he was successfully in charge of developing the first Chinese HDTV prototype system in 1998. By solving the technical bottleneck of highspeedmobile reception of digital television signals, he was one of the main contributors to the Chinese Digital Television Terrestrial Broadcasting Standard issued in 2006. He has more than 37 patents granted and more than 80 referred papers published in international journals and conferences. Prof. Zhang's current research interests include digital video coding and transmission, multimedia semantic processing and intelligent video surveillance. He is a Changjiang Scholarship Professor and was awarded by National Science Fund for Distinguished Scholars in the field of communications and information systems. He is a member of the IEEE.

Chang Wen Chen has been a Professor of Computer Science and Engineering at the University at Buffalo, State University of New York, since 2008. Previously, he was Allen S. Henry Endowed Chair Professor at the Department of Electrical and Computer Engineering, Florida Institute of Technology, from 2003 to 2007. He was on the faculty of Electrical and Computer Engineering at the University of Missouri - Columbia from 1996 to 2003 and at the University of Rochester, Rochester, NY, from 1992 to 1996. From 2000 to 2002, he served as the Head of the Interactive Media Group at the David Sarnoff Research Laboratories, Princeton, NJ. He has also consulted with Kodak Research Labs, Microsoft Research, Mitsubishi Electric Research Labs, Intel Corporation, NASA Goddard Space Flight Center, and Air Force Rome Laboratories. Prof. Chen has been the Editor-in-Chief for the IEEE Transactions on Circuits and Systems for Video Technology (CSVT) since January 2006. He has served as an Editor for Proceedings of IEEE, IEEE Transactions on Multimedia, IEEE Journal of Selected Areas in Communications, IEEE Multimedia Magazine, Journal of Wireless Communication and Mobile Computing, EUROSIP Journal of Signal Processing: Image Communications, and Journal of Visual Communication and Image Representation. He has also chaired and served in numerous technical program committees for IEEE and other international conferences. His current research interests include: reliable and secure multimedia streaming over P2P, wireless and ad hoc networks, mobile multimedia systems – processing, and analysis for mobile systems and devices, medical image analysis and biomedical information processing, distributed source coding for distributed systems and DSP for communications, collaborative signal processing and data aggregation for sensor networks. He received his B.S. degree from University of Science and Technology of China in 1983, MSEE from University of Southern California in 1986, and Ph.D. from University of Illinois at Urbana-Champaign in 1992. He was elected an IEEE Fellow for his contributions in digital image and video processing, analysis, and communications and an SPIE Fellow for his contributions in electronic imaging and visual communications.