# A Stable Low Power Dissipating 9T SRAM For Implementation of 4x4 Memory Array with High Frequency Analysis

**ancy joy** ( ancyjoy32@gmail.com )
Mar Athanasius College of Engineering
**Jinsa Kuruvilla**
Mar Athanasius College of Engineering

**Research Article**

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**Posted Date:** August 30th, 2022

**DOI:** https://doi.org/10.21203/rs.3.rs-436605/v1

# A Stable Low Power Dissipating 9T SRAM For Implementation of 4x4 Memory Array with High Frequency Analysis

**Ancy Joy[1], Jinsa Kuruvilla[2]**

[1] *Electronics and Communication Engineering, Mar Athanasius College of Engineering, Kerala Technological University, (Kerala), INDIA*

[2] *Electronics and Communication Engineering, Mar Athanasius College of Engineering, Kerala Technological University, (Kerala), INDIA*

*E-mail address: ancyjoy32@gmail.com, jinsak123@gmail.com*

*Received ## Mon.20##, Revised ## Mon. 20##, Accepted ## Mon. 20##, Published ## Mon. 20##*

**Abstract:** Today's high speed data processing and memory storage operations demand immediate data write and retrieval to meet up to benchmark. To act as a volatile or nonvolatile data storage for electronic devices such as mobile phones, laptops the Static Random-Access Memory (SRAM) has been perfect choice for industrialists. So memory usage is significant and more than 65% of electronic devices uses memory as its heart. Nevertheless, memory turns out to be a leading factor affecting speed, power and data retention in a handheld system. The urge for optimization in power is all time relevant. The proposed system is designed to optimize a single bit memory cell of conventional static random access memory and hence developed a stable system with low power consumption and obtained significantly low Power-Delay-Product (PDP) by varying operating frequencies in MHz range. Also, a comparative analysis of a 4x4 SRAM array is carried out between 6T SRAM cell and 9T SRAM cell. Here62.83% power reduction is obtained in the proposed system as compared with the existing system at an operating frequency of 2GHz. In this paper, a power reduction of 62.273% is obtained for the array structure. The power dissipation and Power Delay Product [PDP] of the single bit 9T SRAM cell is also lower than the conventional 6T SRAM. Thus, the paper implements the proposed scheme of SRAM into an array along with all connecting peripherals.

**Keywords:** Forced Sleep SVR, Frequency Analysis, PDP, Propagation Delay, SRAM.

## 1. INTRODUCTION

Our day-to-day life has taken a massive turn in evolving exponentially with the help of newly developed technology. In large storage devices data processing speed should increase to process massive data. It provides an interface with easy access, fast operation, better performance and output signal processing. Fast processing and operating speed parameters are achieved by the proper storing and retrieval of data to and from the memory locations.

Rapid processing of huge quantity of records implies quick access of these data at anytime and anywhere essential. Memory modules take part an imperative position of data storage and data retrieval of

records whenever it required. For Graphical Processing Unit (GPU), Microprocessors which are high-speed processors, one among the main choices for system designers are Static Random-Access Memory (SRAM) as cache memory. The critical program files, repeatedly used commands and stored data, all are in cache memory. Since data retrieval rate in cache is greater than in SRAM. It is possible to select RAM for RISC systems PC etc based on certain tradeoffs in design. As compared to DRAM's, SRAM's are much favorable in process, if the major feature for selection is not cost, owing to its advantage in volatility, density, rapidity and further custom performance attributes.

The configuration of SRAM is normally a latching circuitry and it is bistable i.e., two inverters connected back-to-back to form a cross coupled structure and in one side of inverter same information and other side its complemented form. Six Transistor (6T) structure is used in conventional SRAM. It requires a bit refreshment in every few seconds, SRAM has a feature of self-refreshing to avoid extra circuitry.

The optimization in RAM cell is focused on the other perspectives such as energy depletion, stability and dissipation of power. SRAMs are the primary contributors of power even though it has a stable structure and alignment. Static power dissipation and dynamic power dissipation are the major classification in dissipation in CMOS style. These two classifications definitely affect the power dissipation capacitance, output rise time, output loading effects, input voltage level, etc.. are a few parameters. So identifying the net leakage in power is significant in circuit design since scaling of the circuit, current requirements, heating effects are there by can redesign. It is also mandatory to consider in circuit design.

Here the 6T and 9T SRAM array have been implemented and is compared in terms of power[1]. By using dynamic power reduction methods power of 9T SRAM cell is reduced as compared to conventional 6T SRAM and thus by reducing total power in single cell, the power dissipation in a whole array can be factorized. Each SRAM cell holds a single bit, practically a word or blocks of data are stored into an array of cells that can be accessed randomly for both read and write operation by the use of addresses. These operations are carried out in an array using the peripheral circuitry that ensures the proper implementation of the read or write operation in the SRAM array. Periphery circuits like Write Driver Circuit (WDC), Pre-charge Circuit (PCH), Sense Amplifier (SA), and Row Decoder (RD) are also implemented. Here a frequency analysis is conducted in the proposed design and compared with existing. It is the modification of conventional six transistor SRAM cell. Tanner-Tool v16.01 for a 250nm technology node is used for the analysis. Also the delay(speed), power dissipation and Power-Delay-Product (PDP) as performance parameter is evaluated and then compared. It gives an idea of system stability also cell structure performance. Nevertheless the investigation is put through the design layout and parameters such as placement in addition to the area and proximity problems.

## 2. METHODS

The modified design of SRAM cells having less power dissipation. There are 5 PMOS transistors and 4 NMOS transistors are used to design the proposed structure of 9T SRAM cell and using Tanner tool the projected design is related with six transistor SRAM cell at high frequencies.

### *A.* Single SRAM with 6 Transistors

There are combination of NMOS and PMOS transistors formed simple SRAM cell. Here 4 NMOS transistors and 2 PMOS transistors are used, so it is known as 6 transistor SRAM cell or 6T SRAM cell. A cross coupled structure is used to create inverter by using two PMOS and two NMOS devices. The Q and Qbar are the simple and complemented output of inverter, stored within the inverter itself. The bit line and bit line bar of the memory is used for read or write operations, which are connected to the cell using two NMOS transistors called access transistors. When WL is on ie, Word Line, the access transistors will turn on therefore Bit Line and Bit Line bar will connect to the cell. Thus, the two access transistors plays an important role in the read-write process of the cell[2].The schematic of SRAM cell in Figure 1,designed using S-Edit of Tanner tool.

The bit lines will attain a value of Vdd in read operation. Also, the PMOS access transistors will turn on when a logic 1 is applied to Word Line in a particular cell. If one cell carries a value of logic 0 then the bit lines are discharged. Similarly, if one cell carries a value of logic 1 then the bit lines are pre-charged or remains same. Thus, the bit lines are updated with the exact value stored inside cell. So, in read operation the sense amplifier will sense the voltage difference of bit lines.

If the data needs to written into the cell is 1 then load the bit line as 1(bit line bar as 0) and change word line as high. Therefore, the pass transistors will turn on and the value will move from bit line to cell. In write operation, if the data is logic 0 then load the bit line as 0(bit line bar as 1) and change word line as high [3].

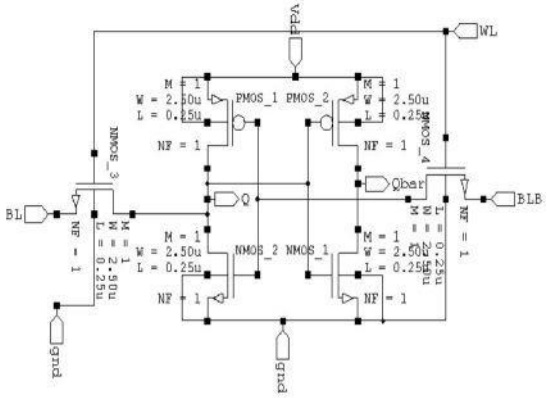


**Fig. 1.Conventional 6T SRAM cell**

*B.* Proposed 9T SRAM Cell

Forced sleep technique[4] is a mixture of forced stack and sleep effect technique. In sleep transistor technique PMOS is coupled between pull-up track and Vdd however NMOS is coupled between the pull-down track and ground whereas in forced sleep technique this connection is reversed. Here NMOS is connected to Vdd and PMOS to ground. For reducing average power consumption, swing voltage reduction method is combined with forced sleep technique[5].

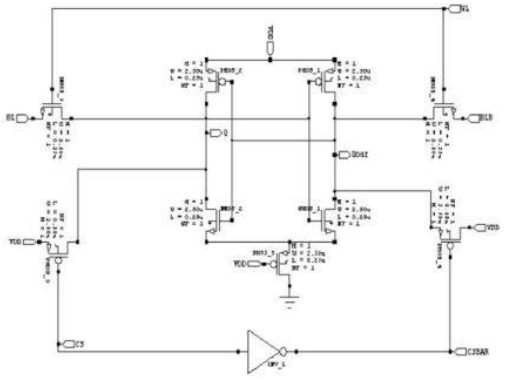

**Fig. 2.Proposed Forced Sleep SVR 9T SRAM cell**

A pair of PMOS and NMOS is connected back-to-back as in a cross coupled inverter fashion similar to conventional 6T SRAM. There are two NMOS transistors connect bit lines to the cell, they are entitled as access transistors. The coupled voltage sources may reduce bit line swing voltage, the two PMOS transistors are controlling this swing. In forced sleep technique sleep transistors are designed using PMOS and which are in the pull-down path.

The control signal will control the operations of sleep transistors which are PMOS in structure [6] also the voltage sources are coupled to PMOS transistors.

*C.* Array of 6T and 9T SRAM Cells

A low power 4X4 array with a storage capacity of 16 bits is designed using proposed SRAM cell which is in forced sleep SVR. Array structure including peripherals such as SRAM cell, Prechargecircuit [7], write driver circuit, Row decoder and Sense amplifier are connected to the basic array block.

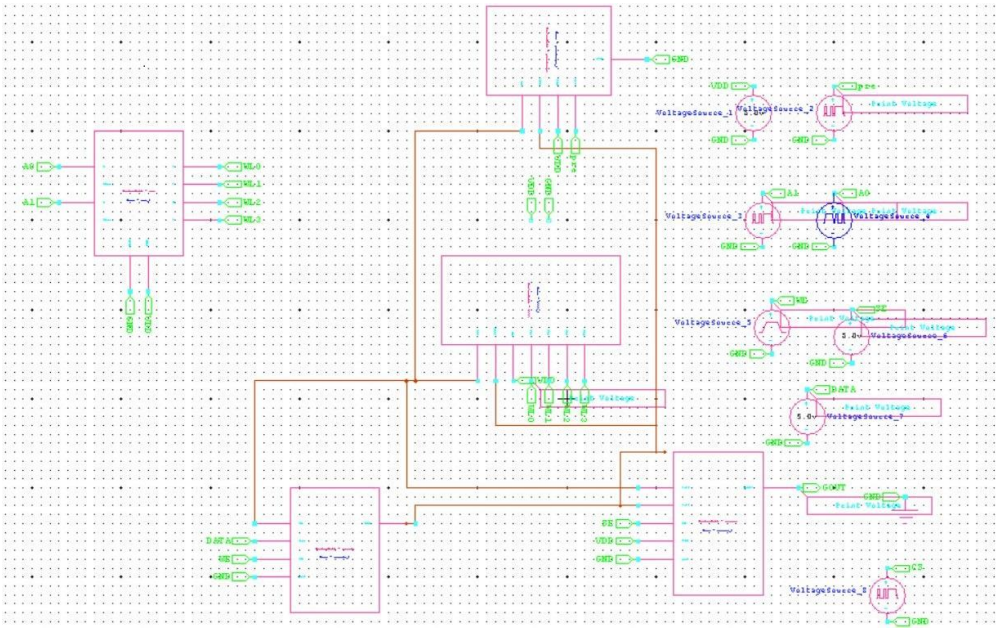

**Fig. 3.Schematic of 9T SRAM array**

The output of 4X4 9T SRAM cell[8] is compared with that of previously obtained 6T array results in terms of total power consumption.

## 3. PERFORMANCE EVALUATION

The proposed 9 Transistor SRAM cell is analyzed and power dissipation is compared with 6 transistor SRAM cell. Additionally, the parameters such as speed, power consumption and the PDP as performance parameter are evaluated then frequency analysis is done for various frequencies like 500MHz, 1GHz, 2GHz.

The power dissipation in SRAM cell is the sum of static and dynamic power dissipation.

$$P_{tot} = P_{sta} + P_{dyn} \text{----- (1)}$$

Where $P_{tot}$ is the total power dissipated,$P_{sta}$is the static power dissipation, which is due to the effect of all leakage currents such as subthreshold leakage, drain induced barrier lowering, reverse current of PN junction in mosfet, gate-induced drain leakage, punch through currents, gate oxide tunneling, and hot carrier effects [8] and $P_{dyn}$ is the dynamic power dissipation which is due to the short circuit current and capacitive switching current.

$$P_{\text{dynamic}} = aCV^2f \quad \text{----- (2)}$$

The dynamic power dissipation of SRAM is given in the above equation [9]. Where C is the load capacitance, which is due to the load connected in the bit lines and α is the activity factor, f is the clock frequency and V is the voltage swing at output node. So the power dissipation is directly proportional to the frequency of operation, voltage swing and the load capacitance. In static power dissipation the subthreshold leakage current is shown below. This is one of the major contributors of static power dissipation.

$$I_{Dsub} = I_{s0}\,.\,[1 - e^{\frac{-\text{Vds}}{Vt}}].\,e[^{\frac{-\text{Vgs}-\text{VT}-\text{Voff}}{nVt}}] \text{----- (3)}$$

$I_{Dsub}$ : subthreshold drain current, it is the current flows from drain to source when the transistor is off or when the gate voltage is less than threshold voltage.

$I_{s0}$ :drain current depends on transistor geometry

$v_{off}$ : model parameter which will vary from device to device

$v_T$ :volt equivalent of temperature

$v_{gs}$ : gate to source voltage

$v_{ds}$ : drain to source voltage

$v_t$ :threshold voltage, it is the minimum voltage required to turn on the device.

From the equation (3), it is very clear that the subthreshold leakage increases exponentially with decreasing threshold voltage.

$P_{sc} = t_{sc} V_{DD} I_{peak} f_{0\to1}$----- (4)

The short circuit power dissipation due to leakage current is given in equation (4), where

$P_{sc}$ :power dissipation due to the short circuit current.

$t_{sc}$ : short circuit current duration

$V_{DD}$ : supply voltage

$I_{peak}$ : saturation current

$f_{0\to1}$ : gate switching factor

### A. *Forced Sleep SVR 9T SRAM Cell*

Proposed 9T SRAM structure is considered out of all other conventional models. Since it has less Power Dissipation, PDP and Delay [9]. The structure is power up with DC supply of 5V. The frequency of operation is chosen as 5MHz where the power reduction of 87% as compared to the existing structure. Similarly, a drop of 65% if the comparison is with 7Transistor SRAM cell structure. Correspondingly, in relation with 8 Transistor SRAM cell structure 87% power reduction is the yield of the suggested structure. This statistic shows by increasing number of transistors the dynamic power increases. But here leakage power is not counted [10].

### B. *Frequency Analysis*

Constant frequencies such as 5 MHz, 2 GHz, 1 GHz are selected for transient analysis. It is to compare and contrast 6 Transistor and 9 Transistor SRAM cells.

TABLE I. COMPARISON OF 6T SRAM AND 9T SRAM CELL.

| Type | Frequency (Hz) | Power (mW) | Delay (ps) | PDP (pJ) |
|---|---|---|---|---|
| Conven-tional 6T SRAM | 500M | 1.4362 | 862.69 | 1.2389 |
| | 1G | 3.7745 | 766.41 | 2.8928 |
| | 2G | 5.3096 | 277.47 | 1.4732 |
| Propos-ed9T SRAM | 500M | 0.8021 | 814.79 | 0.6535 |
| | 1G | 1.3464 | 734.35 | 0.9887 |
| | 2G | 2.0031 | 245.62 | 0.4920 |

The analysis about power dissipation was additionally added with the effect of delay and power delay product on various frequencies. All these studies carried out on the proposed structure of 9 Transistor SRAM and the compared with the conventional structure. It is done for the frequencies such as 500MHz, 1GHz and 2GHz [1]. All the results were tabulated and graphically represented. It will help to ease the analysis part.

The performance of CMOS circuit can be closely evaluated with device parameters such as Propagation delay and energy consumed [11]. High speed of operation is suggested for improved operating frequencies. Power Delay Product is a simple evaluating parameter that helps to weigh up the total energy consumption over a period of time in a device. To obtain the battery life the designers may use these parameters. And this is how, it is easy to maintain at minimum level.

### C. *Power Dissipation*

When the circuit performance increases and the speed improved, it requires power to work. So, both power dissipation and speed are directly proportional. The graph shows a linear increase in power level for various frequencies in the existing 6 transistor cell structure whereas in the proposed structure it is a gradual process [12]. The experimentally evaluated decrease is at 1 GHz ,it is 64.3% similarly at 2 GHz it is 62.2%.

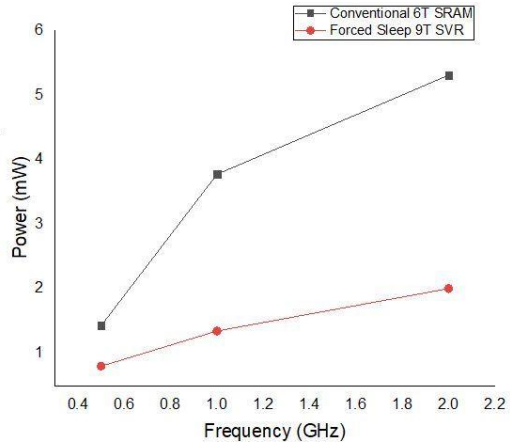


**Fig. 4.Power Dissipation v/s Frequency.**

The power results can further be improved by implementing a layout design. This optimizes the proximity and wire issues [13]. It also helps in optimizing the area occupied by the circuit. The W/L ratio of the circuit is also considered for device performance evaluation [14].

### *4. PROPAGATION DELAY*

Both the frequency and propagation delay are inversely proportional. Therefore, it helps to enable high speed operations. The product of power and delay gives the PDP value, which is accounted as performance parameter [15].

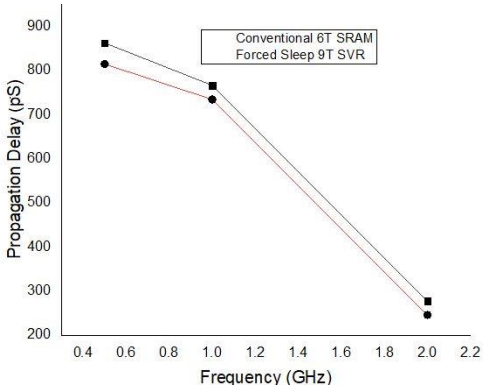


**Fig. 5. Propagation Delay v/s Frequency.**

### *5. POWER DELAY PRODUCT*

The power dissipation of proposed cell decreases drastically while analyzing the PDP factor. The PDP[16]. At 2 GHz the power delay product is 66.6% lesser than the conventional system. Similarly, at 1 GHz the difference is 65.8%. In high speed applications of VLSI the proposed 9 Transistor SRAM structure is better than the existing cells. Asthe number of transistors increases the effective area also increases, nevertheless at high frequencies the power dissipation decreases. This will overcome the drawbacks.

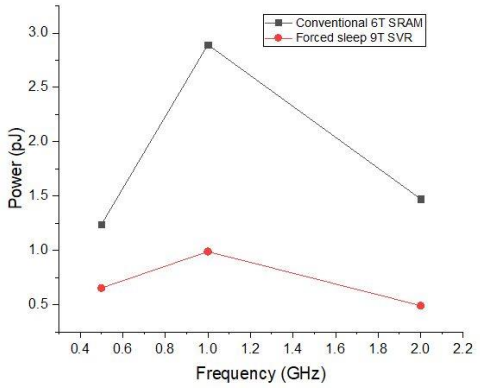


**Fig. 6. PDP v/s Frequency.**

### *6. COMPARISON OF ARRAYS*

The proposed structure and conventional structures were extended to an array for observing the factorization of power [17]. The basics of the array implementation as explained were carried out.

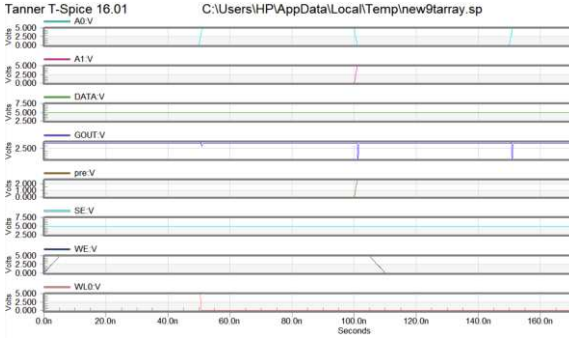


**Fig. 7. Waveform of 9T SRAM array**

The power consumed by 6T conventional 4x4 array was found to be 45.2209mW. The same peripherals were used to evaluate the effect of the power dissipation of the designed cell. The proposed 9T Forced-Sleep SVR SRAM 4x4 array was observed to have a power dissipation of 16.3617mW. Thus, a reduction in power occurs with the value of 62.83%, with respect to the existing structure. These power levels together account for the power dissipation contributed by the peripheral devices, wire lengths used, and a number of 16 cells of the particular design used. The power may further decrease by the effective use of wire and low power dissipating peripheral circuitry.

## 7. CONCLUSION

Practical components like memory devices with multiple units of the same structure contributes to power consumption, delay and area issues, hence during the technological development and evolution, to diminish and enhance power is significant. Here a stable 9 transistor SRAM structure is proposed and which has low power dissipation. In fabrication of device optimization in power is done by controlling static and dynamic power dissipation in 9T SRAM structure. The results validated the core underlying concept that by optimizing the powerconsumption of unique cell, the power dissipation in a whole array can be factorized. Additional voltage sources and forced sleep transistor in the pulldown path helps in lowering the leakage power of the cell. While comparing the dissipation in power, it is significantly low in 9 Transistor SRAM cell than 6 Transistor SRAM. Besides, the Power Delay Product, operations based on variation in frequency and dependency of dealy, power was investigated. It is concluded that the recommended structure noticeably dissipated lesserdelay, power, and PDP.Consequentlythe proposed system is good at high frequency operations. The 9T array was experiential to dissipate 16.3617mW of power, which accounts for the connected peripheral circuitry as well. At 2 GHz operating frequency, a 4x4 array of proposed 9T cell structure experimentally proved 62.273% of power reduction as compared with conventional system. Furthermore, 66.6033%lessening obtained at PDP while compare with 6 Transistor SRAM structure.Thus, as described in paper highly efficient SRAM array with low power consumption is designed. Which is suitable to operate at high frequency with adequate performance.

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**Ms. Ancy Joy** is a research scholar of Mar Athanasius College of Engineering and Technology under Kerala Technological University (Kerala, India). She completed graduation in Electronics and Communication Engineering from Rajagiri School of Engineering (India) and post-graduation in VLSI and Embedded Systems from Viswajyothi College of Engineering(India).Currently she is working as Assistant Professor in Mar Baselios College of Engineering Trivandrum (Kerala, India).Her area of interest includes VLSI, Embedded Systems. Low power VLSI, Memory Design. Ms. Ancy Joy published a number of papers in Journals and International Conferences. She is member of IEEE, IEEE-Wie.

**Dr. JinsaKuruvilla**is working as Assistant Professor of Electronics and Communication Department at Mar Athanasius College of Engineering and Technology under Kerala Technological University (Kerala, India). She completed graduation in Electronics and Communication Engineering from CUSAT (Kerala, India) and post-graduation in VLSI Design from Anna University (Tamilnadu, India). Also she received her PhD in Image Processing from Anna university(Tamilnadu, India) in 2014. Her area of interest includes VLSI, Embedded Systems. Low power VLSI, Memory Design and Image Processing. Dr. Jinsa Kuruvilla published a number of papers in Journals and International Conferences.