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Preface

In the post-Moore era, the further reduction of the energy consumption of computing systems cannot be achieved by transistor scaling. Multiple alternative paths are now being actively explored for continuous improvement in energy efficiency, including novel device research and novel computer architecture research. Meanwhile, it is noticed that many applications we widely use today are error-tolerant, that is, a controlled amount of errors occurred in their internal computation do not affect their application-level quality. Given this, a new computing paradigm, called approximate computing, has been attracting more attention in the past decade. Targeting at the error-tolerant applications, it allows some relaxation in the computation accuracy to achieve further reduction in energy consumption. Despite the recent progress in the research on approximate computing, there are still many new opportunities to design better approximate computing circuits and systems, due to the additional dimension brought by the approximate computing paradigm, namely, the error. Thus, we organize this special section on approximate computing circuits and systems at the Journal of Computer Science and Technology (JCST) jointly with the 2022 CCF Chip Conference. There are six articles in total in this special section.

The first and the second articles provide survey on approximate computing circuits and systems. The first article "A Survey of Approximate Computing: From Arithmetic Units Design to High-Level Applications" by Que *et al.* presents a survey of approximate computing from arithmetic units design to high-level applications. In this article, the authors try to give readers a comprehensive and insightful understanding of approximate computing. The second article "A Survey of Reliability Issues Related to Approximate Circuits" by Wang *et al.* reviews recent progress on approximate computing from another perspective, i.e., reliability. It focuses on three aspects: error analysis of approximate circuits, reliability prediction and vulnerability test of approximate circuits, and fault-tolerant techniques exploiting approximate computing.

The third, the fourth, and the fifth articles introduce new methods for analyzing and designing traditional CMOS-based approximate circuits and systems. The third article "An Optimization Technique for PMF Estimation in Approximate Circuits" by Dou and Wang studies how to efficiently evaluate the errors of a complex approximate system consisting of approximate adders and approximate multipliers. It proposes an effective error propagation method for obtaining the probability mass function of a complex approximate system. The fourth article "LMM: A Fixed-Point Linear Mapping Based Approximate Multiplier for IoT" by Wu *et al.* proposes a fixed-point approximate multiplier that employs a linear mapping technique, which enables the configurability of approximation levels. Besides, a dynamic truncation method and a normalization module are introduced to further optimize the hardware cost. The fifth article "Approximate Processing Element Design and Analysis for the Implementation of CNN Accelerators" by Li *et al.* proposes an approximate processing element dedicatedly designed for convolutional neural network (CNN) accelerators by synergistically considering the data representation, multiplication and accumulation.

The last article "LayCO: Achieving Least Lossy Accuracy for Most Efficient RRAM-Based Deep Neural Network Accelerators via Layer-Centric Co-Optimization" by Zhao *et al.* focuses on performing approximate dot products using emerging resistive random access memory (RRAM). Although there is much progress in the design of RRAM-based architecture, it still faces challenges on energy consumption and endurance. The authors

propose a co-optimizing scheme to address these two issues jointly, while still providing an inference accuracy guarantee.

Finally, we would also like to acknowledge the help from the 2022 CCF Chip Conference in jointly organizing this special section. The CCF Chip Conference is jointly organized by the CCF Technical Committees on Integrated Circuit Design, Fault Tolerant Computing, Computer Architecture, and Information Storage Technology. It provides a forum for researchers and engineers working in areas related to integrated circuits to present their latest technical development and research progress and exchange ideas. It is held once every two years. The 2022 CCF Chip Conference was the inaugural one, which was held in Nanjing, China, from July 29 to July 31, 2022. The conference attracted more than 1 300 participants. During the conference, the recent progress on chip design, electronic design automation, new computer architecture, advanced storage technology, application of fault-tolerant computing, etc. was presented and extensively discussed.

We hope you enjoy reading the articles in this special section of JCST on approximate computing circuits and systems and hope that you find them useful and informative.

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Hua-Wei Li is a professor in Institute of Computing Technology (ICT), Chinese Academy of Sciences (CAS), Beijing. Her current research interests include testing and fault tolerance of VLSI/SOC circuits, and automatic design of deep learning processors. She was a recipient of the 2012 National Technology Invention Award of China, a recipient of the Best Paper Awards of 2021 IEEE Transactions on Computers (TC), 2019 IEEE International Conference on Computer Design (ICCD), and 2018 IEEE International Test Conference in Asia (ITC-Asia). She serves as an associate editor for IEEE Design & Test, IEEE TVLSI, and JCST. She has served as the Secretary General of the China Computer Federation (CCF) Technical Committee on Integrated Circuit Design since 2019, the Chair of the CCF Technical Committee on Fault Tolerant Computing (2016–2019), and the Steering Committee Chair for IEEE Asian Test Symposium (2020–2022).