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EDITORIAL

Editorial of special issue on time-sensitive networking

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1 Introduction

New emerging applications of Internet of things (IoTs) and cyber-physical systems (CPS) have urged stringent real-time communication requirements in the future Internet. As the physical world is gradually connected, sensed, and controlled through computer networks, non-real-time communications may cause catastrophic consequences, e.g., traffic accidents or electric blackouts. Although massive research work has been done on quality-of-service (QoS) guarantee in computer networks, bandwidth over-provisioning is still the practical way in real deployments. Time-sensitive networking (TSN) is a promising technology to support these applications and an enabling technology for future applications of virtual reality or enhanced reality. Though IEEE has published some standards on time-sensitive networking to provide real-time features based on the extension of standard Ethernet techniques, there still exist some challenging issues, such as scalable time synchronization, fast response to network failures, flexible scheduling with the time and bandwidth constraints, and scaling time-sensitive networks beyond local area boundaries. The Deterministic Networking (DetNet) working group of IETF devotes efforts to a broader task to develop the protocols which can provide data paths with guaranteed delay and jitters, and bounded packet loss rates. This special issue is to provide researchers and engineers with a platform for discussing and propelling the research on time-sensitive networking and deterministic networking techniques.

2 Papers in this special issue

This special issue includes four papers that represent the following three important research topics in time-sensitive networking. (1) Scheduling in TSN switches: Scheduling plays a key role in providing a real-time guarantee for TSN equipment. Due to the dynamic nature of network traffic, it is challenging to optimize the utilization of network resources while satisfying the strict time requirements of applications. For example, a guard band is often used to ensure that packets can be emitted at a prescribed time, which may lead to a waste of bandwidth to some extent. Besides, how to implement a TSN scheduling algorithm in hardware efficiently is also an important problem, especially for small embedded connected things. We have two representative papers on this topic that present new designs in algorithmic and engineering aspects. (2) Real-time guarantee at the network edge: Theoretically, network delays and jitters can be bounded if the ingress traffic is deterministic with a fixed network topology. It is a cost-effective approach for TSN by imposing strict traffic regulation at the network edge since traditional off-the-shelf switches can be used as relays. We have a paper that presents a preliminary design in this research direction. (3) Applications through a flexible platform: Different TSN applications in various areas may have very different requirements which lead to an obvious gap between TSN standards

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and real-world systems. An open flexible platform will be valuable for TSN applications as it can be customized rapidly to satisfy application requirements through a software-defined framework. We have a paper that describes an open-source project on this topic which may be beneficial to both researchers and engineers.

2.1 Scheduling in TSN switches

The paper "Packet-size Aware Scheduling Algorithms in Guard Band for Time Sensitive Networking" studies the guard band issue introduced by the Time Aware Shaper (TAS) in IEEE 802.1Qbv standard. The problem varies with different optimization objectives, e.g., maximizing the bandwidth utilization or the sum of packet priorities. It is abstracted as a classic Precedence-Constrained Knapsack Problem (PCKP). An algorithm family named Packet-size Aware Shaping (PAS) is proposed to utilize the bandwidth of guard band by inspecting packet sizes. Several algorithms are designed using dynamic programming and greedy strategy. FPGA-based hardware designs are presented for both the standard TSN scheduler and a programmable one. The simulation results of the proposed algorithms show better performance on improving the bandwidth utilization or packet priority sum of guard bands. The FPGA prototypes also demonstrate better performance on scheduling rate and resource efficiency.

The paper "A Resource-Efficient Priority Scheduler for Time-Sensitive Networking Switches" considers how to design a scheduler efficiently for TSN switches which need to forward data flows of different priorities. It proposes a flattened-priority approach using priority selection and request evaluation to obtain a mapping from input ports to output ports iteratively. The approach can be implemented atop of the non-priority scheduler iSLIP. The proposed scheduler called f-iSLIP is implemented using FPGA and compared to another two priority schedulers. The experiment results demonstrate that the proposed scheduler has better performance in prioritized throughput and decision latency with less FPGA resource cost.

2.2 Real-time guarantee at network edge

The paper "SharpEdge: An Asynchronous and Core-Agnostic Solution to Guarantee Bounded-Delays" investigates the approach to provide delay guarantee by traffic regulation at the network edge. The problem is studied theoretically for networks with single deterministic delay bound under a single switch model and a multi-stage network model respectively. It is proved that hard delay bounds can be achieved if the network is work-conserving and incoming traffic is shaped properly at the network edge. Furthermore, the theoretic analysis is extended to scenarios with multiple delay bounds, and a Quantum shaper is proposed to demonstrate how to shape the ingress traffic. The approach is valuable as it can work with commodity switches and time synchronization is not required, although further research and experiment validation need be done in the future.

2.3 Applications through a flexible platform

The paper "OpenTSN: An Open-source Project for Time-Sensitive Networking System Development" focuses on the problem of a rapid prototype implementation of time-sensitive networking systems. As application scenarios and requirements may differ significantly, there is a large gap between TSN standards and real-world TSN systems. An open platform for rapid TSN system prototyping and evaluation based on software-defined networking (SDN) is valuable to deal with the issue. To this end, the paper introduces OpenTSN, an open-source project that supports rapid TSN system customization. Its design principles, architecture, key features are presented. The main components are detailed, including TSN switch, TSN network interface card (NIC) and TSN controller. This project provides a SDN-based TSN network control mechanism, a time-sensitive management protocol, and a time-sensitive switching model for building efficient TSN systems. Two FPGA-based prototyping examples and related experimental results are presented. The demonstration examples have shown an effective way to implement TSN systems quickly based on the platform, keeping good time synchronization precision and good transmission performance at the same time.

3 Summary

This special issue was initially proposed by Prof. Mingwei Xu from Tsinghua University and Prof. Zhigang Sun from National University of Defense Technology, China. By providing real-time communication guarantee, time-sensitive networking will be an enabling technology for many applications. A team of guest editors who have done or are working in this area was formed. This special issue only selects four papers to represent some research progress in TSN, although we believe that there are many ongoing works all over the world from academic research to industry practice. We hope that this special issue will bring more researchers and engineers together to make more advances in this area.

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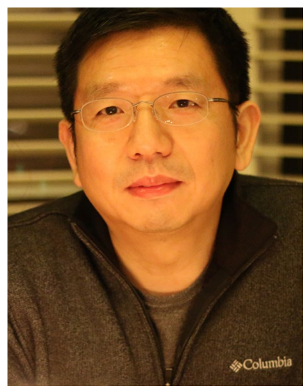

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