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EDITORIAL

Editorial for the special issue on disruptive computing technologies

Yiran Chen[1] · Deliang Fan[2] · Yanzhi Wang[3] · Shigeru Yamashita[4]

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The modern computing paradigm is experiencing many revolutions from almost every aspects: the introduction of emerging memories like spintronic memory and resistive memory dramatically as well as quantum computing change the design of memory hierarchy and interface; new applications such as artificial intelligence and deep learning trigger wide adaptation of deep neural network accelerators and neuromorphic computing circuits; new computing models induced by these applications such as in-memory computing also inspires the corresponding circuit- and architecture-level practices.

The goal of this special issue is to present the novel ideas, designs, implementations, and practices of new disruptive computing technologies for resolving the above challenges, by leveraging recent advances in materials, devices, architectures, system designs, and applications. We include seven papers for this special issue (including a regular paper) based on a peer-review procedure, covering various aspects of disruptive computing technologies.

The first paper presents a fast hardware simulator architecture for the Walsh–Hadamard transform, which is a core of many quantum algorithms including quantum heuristic algorithms. The authors develop a method to divide the whole computation of the Walsh-Hadamard transform into pieces and process them in a pipelined manner.

✉ Yiran Chen
yiran.chen@duke.edu

Deliang Fan
dfan@asu.edu

Yanzhi Wang
yanz.wang@northeastern.edu

Shigeru Yamashita
ger@cs.ritsumei.ac.jp

[1] Duke University, Durham, USA

[2] Arizona State University, Tempe, USA

[3] Northeastern University, Boston, USA

[4] Ritsumeikan University, Kyoto, Japan

The second paper first presents a quantum multiplier based on Quantum Fourier.

Transform (QFT), which is composed of a series of double-controlled phase gates. An optimization is then conducted on the proposed quantum multiplier to reduce the number of qubits in ancillary and reduce the resource cost of quantum multiplier greatly.

The third paper proposes an enhanced quantum scheme for generalized novel enhanced quantum image representation. Simulations show that the proposed scheme can greatly improve the security and processing efficiency of image encryption algorithm.

The fourth paper develops a flexible precise-time-dependent single-spike neuromorphic computing architecture, namely "FPT-Spike". "FPT-spike" relies on three hardware-favorable components: precise ultra-sparse spike temporal encoding, efficient supervised temporal learning and fast asymmetric decoding, to realize flexible spatial–temporal information trade-off for neural network size reduction without scarifying data processing capability.

The fifth paper proposes a reconfigurable computing-in-memory architecture for general purpose computing based on STT-MRAM (GCIM). The proposed GCIM could significantly reduce the energy consumption of data transformation and effectively process both fix-point calculation and float-point calculation in parallel.

The sixth paper proposes a novel write-only in-memory computing paradigm based on interplay bitwise operation in two terminal or three terminal MRAM bit-cell. The proposed design can reduce the layout overhead of peripheral computing circuits and eliminate read decision failure in the procedure of in-memory computing.

The seventh paper is a regular paper about a congestion aware cluster buffer base routing algorithm with minimal cost on Network-on-Chip.

We would like to take this chance to thank all the authors and the reviewers for their splendid contribution to this special issue of CCF THPC, and the guidance and supports from the Editor-in-Chief and administration office of CCF THPC.

Dr. Yiran Chen received B.S and M.S. from Tsinghua University and Ph.D. from Purdue University in 2005. After five years in industry, he joined University of Pittsburgh in 2010 as Assistant Professor and then promoted to Associate Professor with tenure in 2014, held Bicentennial Alumni Faculty Fellow. He now is the Professor of the Department of Electrical and Computer Engineering at Duke University and serving as the director of NSF Industry–University Cooperative Research Center (IUCRC) for Alternative Sustainable and Intelligent Computing (ASIC) and co-director of Duke University Center for Computational Evolutionary Intelligence (CEI), focusing on the research of new memory and storage systems, machine learning and neuromorphic computing, and mobile computing systems. Dr. Chen has published one book and more than 400 technical publications and has been granted 94 US patents. He serves or served the associate editor of several IEEE and ACM transactions/journals and served on the technical and organization committees of more than 50 international conferences. He is now serving as the Editor-in-Chief of IEEE Circuits and Systems Magazine. He received 6 best paper awards, 1 best poster award, and 14 best paper nominations from international conferences and workshops. He is the recipient of NSF CAREER award, ACM SIGDA outstanding new faculty award, the Humboldt Research Fellowship for Experienced Researchers, and the IEEE SYSC/CEDA TCCPS Mid-Career Award. He is the Fellow of IEEE, Distinguished Member of ACM, and a distinguished lecturer of IEEE CEDA.

Dr. Deliang Fan is currently an Assistant Professor in the School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ, USA. Before joining ASU in 2019, he was an assistant professor in Department of Electrical and Computer Engineering at University of Central Florida, Orlando, FL, USA. He received his M.S. and Ph.D. degrees, under the supervision of Prof. Kaushik Roy, in Electrical and Computer Engineering from Purdue University, West Lafayette, IN, USA, in 2012 and 2015, respectively. Dr. Fan's primary research interests include Energy Efficient and High Performance Big Data Processing-In-Memory Circuit, Architecture and Algorithm, with applications in Deep Neural Network, Data Encryption, Graph Processing and Bioinformatics Acceleration-in-Memory system; Hardware-aware deep learning optimization; Brain-inspired (Neuromorphic) Computing; AI security. He has authored and co-authored 100+ peer-reviewed international journal/conference papers in above area. He is the receipt of best paper award of 2019 ACM Great Lakes Symposium on VLSI, 2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), and 2017 IEEE ISVLSI. His research paper was also nominated as best paper candidate of 2019 Asia and South Pacific Design Automation Conference. He served as technical reviewers for over 30 international journals/conferences, such as Nature Electronics, IEEE TNNLS, TVLSI, TCAD, TNANO, TC, TCAS, etc. He also served as the Technical Program Committee member of DAC, ICCAD, HPCA, MICRO, WACV, GLSVLSI, ISVLSI, ASP-DAC, etc. He is also the technical area chair of GLSVLSI 2019/2020, ISQED 2019/2020, and the financial chair of ISVLSI 2019. Please refer to https://dfan.engineering.asu.edu/ for more details.

Yanzhi Wang is currently an assistant professor at Dept. of ECE at Northeastern University, Boston, MA. He received the B.S. degree from Tsinghua University in 2009, and Ph.D. degree from University of Southern California in 2014. His research interests focus on model compression and platform-specific acceleration of deep learning applications. His research maintains the highest model compression rates on representative DNNs since 09/2018. His work on AQFP superconducting based DNN acceleration is by far the highest energy efficiency among all hardware devices. His recent research achievement, CoCoPIE, can achieve real-time performance on almost all deep learning applications using off-the-shelf mobile devices, outperforming competing frameworks by up to 180X acceleration. His work has been published broadly in top conference and journal venues (e.g., DAC, ICCAD, ASPLOS, ISCA, MICRO, HPCA, PLDI, ICS, PACT, ISSCC, AAAI, ICML, CVPR, ICLR, IJCAI, ECCV, ICDM, ACM MM, FPGA, LCTES, CCS, VLDB, PACT, ICDCS, Infocom, C-ACM, JSSC, TComputer, TCAS-I, TCAD, TCAS-I, JSAC, TNNLS, etc.), and has been cited over 7,200 times. He has received four Best Paper Awards, has another ten Best Paper Nominations and four Popular Paper Awards. He has received the ARO Young Investigator Program Award (YIP), Massachusetts Acorn Innovation Award, and other research awards from Google, MathWorks, etc. Three of his former Ph.D./postdoc students become tenure track faculty at Univ. of Connecticut, Clemson University, and Texas A&M University, Corpse Christi.

Dr. Shigeru Yamashita is a professor of College of Information Science and Engineering, Ritsumeikan University. He received his B. E., M. E. and Ph.D. degrees in information science from Kyoto University, Kyoto, Japan, in 1993, 1995 and 2001, respectively. In 1995, he joined NTT Communication Science Laboratories, where he engaged in research of computer aided design of digital systems and new type of computer architectures. During 2000 to 2003, he was also a researcher at Quantum Computation and Information, ERATO, Japan Science and Technology Corporation. During 2003 to 2009, he was an associate professor of Graduate School of Information Science, Nara Institute of Science and Technology. He also served a Visiting Professor at National Institute of Informatics from 2012 to 2017. He received the 2000 IEEE Circuits and Systems Society Transactions on Computer-Aided Design of Integrated Circuits and Systems Best Paper Award, SASIMI 2010 Best Paper Award, 2010 IPSJ Yamashita SIG Research Award, SASIMI 2018 Outstanding Paper Award, Marubun Academic Achievement Award of the Marubun Research Promotion Foundation. He is a senior member of IEEE and IEICE, and a member of ACM and IPSJ.