CORRECTION



Correction to: Efficient Architecture for Block Parallel Convolution Using Two-Dimensional Polyphase Decomposition

Anitha Arumalla¹ •• Madhavi Latha Makkena²

Published online: 18 October 2021

© The Author(s), under exclusive licence to Springer Science+Business Media, LLC, part of Springer Nature 2021

Correction to: Circuits, Systems, and Signal Processing https://doi.org/10.1007/s00034-021-01811-9

In the section '3 Scalable Recursive Convolution (SRC)', the sentence beginning 'The input matrix is a column matrix with 2m-1..', the term ' $[\mathbf{W_{m,n-m+1}}, ..., \mathbf{W_{m,n-1}}, \mathbf{W_{m,n}}, \mathbf{W_{m,n+1}}, ..., \mathbf{W_{m,n+m-1}}]$ ' should have read ' $[W_{m,n-m+1}...W_{m,n-1}, ..., \mathbf{F_{m,n+1}}, ..., \mathbf{F_{m,n+m-1}}]$ ' should have read ' $[F_{m,n}, F_{m,n+1}, ..., F_{m,n+m-1}]$ '. In the sentence beginning ' $\mathbf{G_{mS}}$ is a pre-computed matrix that can be further... .', the term ' $[G_{m-1}, G_{m-2}, ..., G_1, G_0]^T$ ' should have read ' $[G_{m-1}, G_{m-2}, ..., G_1, G_0]^T$ ' should have

In the section '4.1 Mathematical Formulation', the sentence beginning 'Figure 2b represents an OSB for 2×2 BPC...', the term 'Yuv' should have read ' Y_{uv} '. In the sentence beginning 'The resulting 2D BPC....', the term ' $X_{m\times m}S$ ' should have read ' $X_{m\times m}S$ ' and the term ' $P_{m\times m}S$, $Q_{m\times m}S$ ' should have read ' $P_{m\times m}S$, $Q_{m\times m}S$ '.

In the section, '4.2 BPSRC Architecture', the sentence 'The throughput of DFA for BPSRC filter is m samples per clk.' should have read 'The throughput of DFA for $m \times m$ BPSRC filter is m samples per clock.'

The original article has been corrected.

Publisher's Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

The original article can be found online at https://doi.org/10.1007/s00034-021-01811-9.

Anitha Arumalla anithaarumalla83@gmail.com Madhavi Latha Makkena mlmakkena@yahoo.com

ECE Department, Jawaharlal Nehru Technological University Hyderabad, Hyderabad, India



¹ ECE Department, Velagapudi Ramakrishna Siddhartha Engineering College, Vijayawada, India