

# Minor-embedding heuristics for large-scale annealing processors with sparse hardware graphs of up to 102,400 nodes

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**Abstract** Minor embedding heuristics have become an indispensable tool for compiling problems in quadratically unconstrained binary optimization (QUBO) into the hardware graphs of quantum and CMOS annealing processors. While recent embedding heuristics have been developed for annealers of moderate size (about 2000 nodes) the size of the

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latest CMOS annealing processor (with 102,400 nodes) poses entirely new demands on the embedding heuristic. This raises the question, if recent embedding heuristics can maintain meaningful embedding performance on hardware graphs of increasing size. Here, we develop an improved version of the probabilistic-swap-shift-annealing (PSSA) embedding heuristic [which has recently been demonstrated to outperform the standard embedding heuristic by D-Wave Systems (Cai et al., 2014)] and evaluate its embedding performance on hardware graphs of increasing size. For random-cubic and Barabasi-Albert graphs we find the embedding performance of improved PSSA to consistently exceed the threshold of the best known complete graph embedding by a factor of 3.2 and 2.8, respectively, up to hardware graphs with 102,400 nodes. On the other hand, for random graphs with constant edge density not even improved PSSA can overcome the deterministic threshold guaranteed by the existence of the best known complete graph embedding. Finally, we prove a new upper bound on the maximal embeddable size of complete graphs into hardware graphs of CMOS annealers and show that the embedding performance of its currently best known complete graph embedding has optimal order for hardware graphs with fixed coordination number.

**Keywords** graph minor · heuristic · scalability · annealing · QUBO

## 1 Introduction

The last decade has witnessed impressive progress in the development of a new hardware architecture, which is commonly known as annealing processor. This development was sparked by the discovery of a new model for quantum computation (Farhi et al., 2001; Kadowaki and Nishimori, 1998), which led to the development of annealing hardware based on superconducting quantum bits (D-Wave Systems Inc.,

since 2007; Johnson et al., 2011). Simultaneously, the performance of hardware processors executing simulated annealing (Kirkpatrick et al., 1983) has improved considerably, e.g., due to algorithmic advances (Aramon et al., 2018; Isakov et al., 2015; Zhu et al., 2015) as well as customized hardware circuits based on CMOS or laser technology, see (Hitachi Ltd., 2018; Matsubara et al., 2018; Okuyama et al., 2017; Takemoto et al., 2019; Tsukamoto et al., 2017; Yamaoka et al., 2016) or (Inagaki et al., 2016; McMahon et al., 2016) for references. While hardware realizations may differ in their implementation, all annealing processors perform exactly the same task. That is, they provide a fast method for finding the ground state configuration, which minimizes the energy of an Ising model. In that, they represent the ideal hardware for solving combinatorial optimization problems in quadratic unconstrained binary optimization (QUBO) (see, e.g., Kochenberger et al., 2014; Lucas, 2014) and related applications, e.g., in quantum chemistry (Xia et al., 2018) or machine learning (Neven et al., 2009).

A general problem in quadratically unconstrained binary optimization results in Ising models which consist of  $N$  binary spin variables  $\{\sigma_i\}$  which take values  $\sigma_i \in \{-1, 1\}$ ,  $i = 1, \dots, N$ . The energy of each spin configuration is given by

$$H(\sigma_i) = - \sum_{i,j=1}^N \sigma_i J_{ij} \sigma_j - \sum_{i=1}^N h_i \sigma_i, \quad (1)$$

where  $h_i \in \mathbb{R}$  and  $J_{ij} \in \mathbb{R}$  are externally fixed model parameters, known as magnetic fields and spin-spin couplings, respectively. These model parameters encode the energy landscape (or cost function) of the optimization problem. Unfortunately, present day quantum annealers can only provide for a finite amount of couplings between spins (D-Wave Systems Inc., since 2007; Johnson et al., 2011), resulting in tangible restrictions on  $J_{ij}$ . In particular, the non-zero  $J_{ij}$  of a quantum annealer induce the famous hardware topology known as chimera graph. Similarly, large-scale CMOS annealing processors with up to 102,400 spins and fast parallel updates have only been realized with sparse hardware topologies (Hitachi Ltd., 2018; Takemoto et al., 2019; Yamaoka et al., 2016). In this case, the non-zero spin-spin couplings  $J_{ij}$  induce the hardware topology of a King’s graph, as illustrated in Fig. 1. In order to solve QUBO problems on such annealing processors, the ground state search of the given Ising model has to be mapped to a given hardware by means of minor embedding (Choi, 2008). See Fig. 1(a) for a general work flow. In minor embedding each spin of the original Hamiltonian is represented by a tightly connected group of spins on the hardware, which are forced to point into the same direction, see Fig. 1(c). Such a group of hardware spins is called a *super vertex*, representing a single spin of the original input problem. In contrast to a single spin, a super vertex can be adjacent to many other super vertices

on the hardware. Precisely this property allows for encoding the spin-spin couplings of the original Ising model between super vertices, see Fig. 1(b, c) for an example.

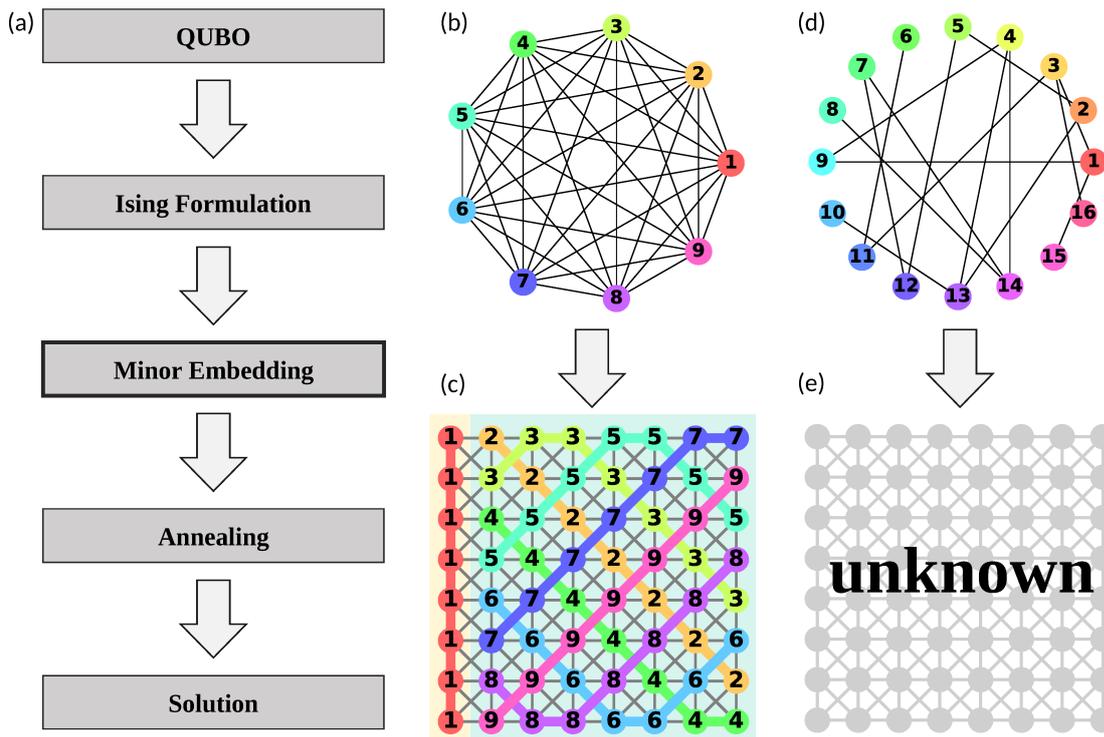
Minor embedding for annealing processors, i.e., embedding an input graph  $I$  (induced by the non-zero couplings of a given optimization problem) into a hardware graph  $H$  (induced by the non-zero couplings of the hardware) has attracted significant attention over the past decade. In particular, for optimization problems whose input graph  $I$  posses a predefined structure fast deterministic and often optimal embeddings into the static hardware graphs  $H$  are known. See (Boothby et al., 2016; Choi, 2011; Klymko et al., 2014; Okuyama et al., 2016; Venturelli et al., 2015) for embeddings of complete graphs, (Goodrich et al., 2018; Okuyama et al., 2016) for embeddings of bipartite graphs, or (Zaribafiyani et al., 2017) for embeddings of Cartesian product graphs. On the other hand, many problems in combinatorial optimization, such as solving the clique problem on social networks, produce sparse input graphs whose connections appear random. Such optimization problems do not posses a tangible structure which can systematically be exploited for minor embedding. Yet, embedding such problems by resorting to minor embeddings of complete graphs seems wasteful. For example, for the presently best quantum annealer with 2048 hardware spins, it would result in representing input problems with only 65 spins. Similarly, for the currently largest CMOS annealer with 102400 spins, it would result in representing input problems with only 321 spins. Hence, improving over the embeddability threshold ensured by the best known complete graph embeddings is desirable.

To this end, one could, in principle, resort to the exact algorithms invented by (Robertson and Seymour, 1995) and later improved by (Kawarabayashi et al., 2012) and (Adler et al., 2011). However, these algorithms are not constructive and have prohibitively large runtime

$$\mathcal{O} \left( 2^{(2k+1) \log k} |V(I)|^{2k} 2^{2|V(I)|^2} |E(H)| \right), \quad (2)$$

which scales exponentially with the number of vertices of the input graph  $|V(I)|$ , linearly in the number of edges on the hardware graph  $|E(H)|$ , and further depends on the branch width  $k$  of the hardware graph. For this reason, it is important to have efficient heuristics which find graph minors with high probability, rather than attempting an exhaustive search or proving minor exclusion. Such a heuristic was, for example, proposed in (Cai et al., 2014) and has subsequently become state of the art due to its inclusion in the standard software package provided by D-Wave Systems. An alternative heuristic, called probabilistic-swap-shift-annealing (PSSA), was subsequently invented by YY as a submission to the “Hokkaido University & Hitachi 2nd New-Concept Computing Contest 2017.”<sup>1</sup> There it showed outstanding perfor-

<sup>1</sup> <https://hokudai-hitachi2017-2.contest.atcoder.jp/>



**Fig. 1** (a) Work flow for solving QUBO problems on annealing hardware, emphasizing the role of graph-minor embeddings for representing (b, d) the spin-spin connectivity graphs of a given QUBO input on (c, e) annealing hardware with sparse spin-spin connectivity. (b, c) Minor embedding of a complete graph  $K_9$  into a King's graph  $KG_{8,8}$ . Each super vertex is marked by the corresponding vertex label of the input graph.

formance as compared to hundreds of other submissions, eventually winning the contest. Its superior performance to (Cai et al., 2014) was later demonstrated by the authors in (Sugie et al., 2018). While both heuristics have initially been developed for annealers of moderate size (about 2000 spins) the release of the latest CMOS annealing processor with 102,400 spins poses entirely new demands on the performance of the embedding heuristics. With D-Wave Systems doubling the number of qubits of its annealers roughly every two years a similar demand on embedding heuristics is expected for quantum annealers in the near future.

In this paper, we present an improved version of PSSA and use it in a case study to evaluate the performance of embedding heuristics on ever larger hardware graphs of up to 102,400 spins. The algorithmic improvements of PSSA include (i) an additional search phase, (ii) a degree-oriented super-vertex shift rule, and (iii) optimized annealing schedules. The performance of improved PSSA is then investigated with respect to various types of random input graphs on hardware graphs of increasing size. An embedding performance consistently exceeding the embedding threshold of the best known complete graph embedding by a constant factor  $c$  is observed for random-cubic ( $c = 3.2$ ) and Barabási-Albert ( $c = 2.8$ ) graphs for hardware graphs up to 102,400 spins. Incidentally this constitutes an average per-

formance gain of 42% and 28%, respectively, over the previously published version of PSSA (Sugie et al., 2018). On the other hand, for sparse random graphs with constant edge density even the embedding performance of improved PSSA shrinks to the deterministic threshold guaranteed by the existence of the best known complete graph embedding on large hardware graphs. Finally, this paper provides a new upper bound on the maximal complete graphs embeddable into a King's graph hardware of present CMOS annealing processors. In addition, we prove that the baseline performance of the currently best known complete graph embedding has optimal order for hardware graphs with fixed coordination number.

This paper is organized as follows. In Sect. 2 we lay out the basic notation, define graph minors, and specify the algorithm task. In Sect. 3, we briefly outline PSSA as previously published in (Sugie et al., 2018) in order to make the paper self-contained. In Sect. 4 we present several improvements of PSSA, including (i) an additional terminal search phase, (ii) a degree-oriented super vertex shift rule, and (iii) optimized annealing schedules. Finally, in Sect. 5 we evaluate the embedding performance of the improved PSSA on hardware graphs of increasing size (up to 102,400 nodes) with respect to various input problems. In Sect. 6 we prove an upper bound on the maximal complete graphs embeddable

into a hardware King's graphs of CMOS annealers and show that the baseline performance of the currently best known complete graph embedding has optimal order for hardware graphs with fixed coordination number. We summarize in Sect. 7 and discuss open questions for future research.

## 2 Preliminaries

In this section we introduce some basic notations and definitions. In particular, we define minor embeddings and super vertex placements, describe the hardware graph, specify the algorithm task, and discuss several input graphs which will be used for evaluating the embedding performance of improved PSSA on hardware graphs of ever larger size.

### 2.1 Graph minor and super vertex placement

In what follows we consider undirected and simple graphs. Let  $I = (V(I), E(I))$  denote an input graph. Its vertex set  $V(I)$  represents the spin indices  $i = 1, \dots, N$  of the original QUBO problem, Eq. (1). Its edges  $(i, j) \in E(I) \subset V(I) \times V(I)$  are induced by the non-zero entries of the corresponding symmetric connectivity matrix  $J_{ij}$ ,  $i, j = 1, \dots, N$ . Let  $H = (V(H), E(H))$  denote a hardware graph. Its vertex set  $V(H)$  shall represent the spins of the hardware, while its edges  $E(H)$  are induced by the non-zero couplings of the annealing processor.

We now define a minor embedding, similar to (Cai et al., 2014). Our definition will proceed in two stages. In the first stage we define a super vertex placement.

**Definition 1 (Super Vertex Placement)** Let  $I, H$  be two graphs. A super vertex placement is a function  $\phi : V(I) \rightarrow 2^{V(H)}$  which assigns each vertex  $i \in V(I)$  to a subset of vertices  $\phi(i) \subset V(H)$ , such that:

(M1)  $\forall i \in V(I)$ :  $\phi(i) \neq \emptyset$  and the subgraph induced by  $\phi(i)$  in  $H$  is connected.

(M2)  $\forall i, j \in V(I)$  with  $i \neq j$ :  $\phi(i) \cap \phi(j) = \emptyset$ .

In the second stage we define a minor embedding.

**Definition 2 (Minor Embedding)** Let  $I, H$  be two graphs. A super vertex placement  $\phi$  is a minor embedding, if in addition to property (M1) and (M2) we have

(M3)  $\forall (i, j) \in E(I)$ :  
 $\exists (u, v) \in \phi(i) \times \phi(j)$  such that  $(u, v) \in E(H)$ .

In what follows we refer to each set  $\phi(i)$ , induced by a super vertex placement  $\phi$ , as a super vertex. In order for  $\phi(i)$  to represent a single spin from the input problem, we require super vertices to be non-empty and connected, hence (M1). In addition, a single spin of the hardware cannot represent multiple spins of an input problem, hence (M2). Finally, a

valid representation of a given Ising model can be provided, if and only if all edges of the input graph  $I$ , induced by non-zero values of  $J_{ij}$ , can be represented by at least one edge between the corresponding super vertices on the hardware graph. Hence, a given super vertex placement  $\phi$  is a suitable hardware mapping, if and only if it is a minor embedding. See Fig. 1(b, c) for an example.

In order to rate the quality of a super vertex placement  $\phi$ , we define a function which counts the edges that a super vertex placement faithfully represents on the hardware graph.

**Definition 3 (Number of Embedded Edges)** Let  $I, H$  be two graphs and  $\phi$  a super vertex placement. The number of edges embedded by  $\phi$  is defined as

$$E_{\text{emb}}(\phi) := |\{(i, j) \in E(I) \mid \exists u \in \phi(i), v \in \phi(j) \text{ with } (u, v) \in E(H)\}|. \quad (3)$$

For a general super vertex placement we have that  $E_{\text{emb}}(\phi) \leq |E(I)|$  and a valid minor embedding, satisfying condition (M3), is found, if and only if  $E_{\text{emb}}(\phi) = |E(I)|$ .

Note that for certain inputs  $I$  and a fixed hardware  $H$ , it may be the case that no minor embedding exists. In that case the number of embedded edges will be strictly smaller than the number of edges of the input graph, such that  $E_{\text{emb}}(\phi) < |E(I)|$  for any super vertex placement  $\phi$ . In this case the heuristic we propose in the next sections is bound to fail. Furthermore, throughout the annealing phase of PSSA, we restrict our implementation to super vertex placements where each super vertex  $\phi(i)$  can be parametrized by a path. We denote the endpoints of the vertex path, i.e., the set of its leaves by  $\text{Leaf}[\phi(i)]$ .

Finally, we emphasize that finding a minor embedding is the key ingredient for mapping QUBO problems, Eq. (1), onto the spin-spin couplings and external magnetic fields of an annealing processor. Prior to finding the minor embedding one determines the input graphs  $I$  from the non-zero entries of the matrix  $J_{i,j}$ . After a minor embedding is found, the the spin-spin couplings and external magnetic fields of the annealing processor can be determined from the input parameters and the minor embedding  $(J_{i,j}, h_i, \phi)$  as described in (Choi, 2008).<sup>2</sup> Both processes are straight forward and will no further be mentioned in this paper.

### 2.2 Hardware graphs

The development of annealing processors with sparse hardware topology currently knows two pertinent hardware ar-

<sup>2</sup> Roughly speaking, (i) the coupling  $J_{i,j}$  will be applied to exactly one coupler connecting the super vertices  $\phi(i)$  and  $\phi(j)$ , (ii) The internal connections of super vertex  $\phi(i)$  are set to a strength of order  $\mathcal{O}(\sum_{j \in \text{nbr}(i)} |J_{i,j}| - |h_i|)$ , where  $\text{nbr}(i)$  denotes the vertex neighbors of  $i \in V(I)$ , and (iii) the magnetic field  $h_i$  is distributed across the spins of the super vertex  $\phi(i)$ .

chitectures. One is the Chimera graph topology adopted by quantum annealers (Choi, 2011; Klymko et al., 2014). The other is the King’s graph topology adopted by the CMOS annealing processors (Okuyama et al., 2016, 2017). Both hardware graphs have very similar general features, i.e.: (i) both graphs have a fixed coordination number, (ii) for both graphs the tree-width grows as a square root of vertices  $\mathcal{O}(\sqrt{|V(H)|})$ , and (iii) for both hardware graphs constructive minor embeddings of complete graphs ensure the embeddability of input graphs with  $\mathcal{O}(\sqrt{|V(H)|})$  vertices. (See next section for details.)

In this study, we will focus on hardware topologies  $H$  forming a square King’s graph (Okuyama et al., 2017) while omitting Chimera-type hardware graphs entirely. We made this choice due to the following arguments: (i) The large scale hardware structures on which we benchmark the performance of improved PSSA has so far only been realized for CMOS annealers with hardware King’s graphs of up to 102,400 spins. (ii) A performance analysis of PSSA on Chimera graphs has previously been published in (Sugie et al., 2018) and is no longer the main objective of this paper. (iii) We believe that our evaluation of the embedding performance of PSSA on hardware King’s graphs of increasing size would not fundamentally change, if carried out on Chimera graphs due to the similarity of both graphs with respect to general features.

A square King’s graph represents all valid moves of the king chess piece on a chessboard, i.e., each vertex represents a square of the chessboard and each edge is a valid move. We denote the King’s graph by the symbol  $KG_{L,L}$ , where  $L$  denotes the width of the chessboard and  $L \times L$  denotes the total number of vertices  $|V(H)|$ . See Fig. 1(c, e) for an example. In what follows, the King’s graph  $KG_{L,L}$  defined by the hardware is usually fixed. The goal is to find minor embeddings for large input graphs which have as many vertices  $|V(I)|$  as possible.

### 2.3 Best known complete graph embedding

A simple and fast baseline strategy for minor embedding into a fixed hardware graph exploits the existence of known complete graph embeddings. In particular, if a minor embedding of a complete graph  $K_N$  with  $N$  vertices is known, embedding of other input graphs with  $N$  vertices is trivial. For a fixed King’s graph hardware  $KG_{L,L}$ , embedding complete graphs  $K_N$  with up to  $N = L + 1$  vertices, is always possible using the construction of (Okuyama et al., 2016). See Fig. 1(b, c) for a sketch. Hence, minor embedding of any graph  $I$  with  $|V(I)| \leq L + 1$  is trivial. On the other hand, a systematic embedding of complete graphs  $K_N$  with  $N > L + 1$  is currently unknown and believed to be impossible. (A proof showing that complete graphs  $K_N$  with  $N > 2L$  are not embeddable into King’s graph  $KG_{L,L}$  is given

in Sect. 6.) In absence of a proof of optimality we refer to the embedding of complete graphs according to (Okuyama et al., 2016) as the *best known complete graph embedding*.

### 2.4 Sparse random input graphs

While the best known complete graph embedding does not allow for embedding complete graphs with  $|V(I)| > L + 1$  into a King’s graph, going beyond this embedding threshold should be feasible, if the input graph is sparse. See Fig. 1(d, e). PSSA tries to find minor embeddings precisely for this kind of input, in order to widen the range of QUBO problems amenable to the hardware of annealing processors. However, if a certain QUBO problem induces sparse input graphs  $I$  with a predefined structure, it is advisable to resort to a deterministic minor embedding. This is usually faster and most likely produces embeddings for larger input graphs than a general purpose heuristic. This strategy has, for example, been applied for the minor embedding of bipartite graphs (Goodrich et al., 2018; Okuyama et al., 2016) or the minor embedding of Cartesian product graphs (Zaribafiyani et al., 2017). In that, an embedding heuristic should be applied to sparse input problems whose structure is not known in advance. In other words, an embedding heuristics is used on input graphs which appear to be random to some degree. Such randomized sparse input graphs can appear, e.g., in graph coloring or when solving the clique problem (Lucas, 2014) on social network graphs (Albert and Barabási, 2002). To benchmark PSSA on a wide variety of potential input types, this paper considers the following three famous classes of random input graphs. (i) Random cubic graphs as a model of super low edge density, (ii) Barabási-Albert random graphs (Albert and Barabási, 2002) as a prototype of scale-free graph structures from social network science, and (iii) Erdős-Rényi random graphs (Bollobás, 1985; Erdős and Rényi, 1959) with constant edge density as a prototype of a sparse random graph with high complexity. For a detailed description of these graphs, the reader is referred to Appendix 8.1.

### 2.5 Embedding probability and embedding threshold

We now define our performance measures.

**Definition 4 (Embedding Probability)** Let  $\mathcal{G}$  denote a class of input graphs  $I \in \mathcal{G}$ , e.g., random cubic graphs. Let  $\mathcal{A}$  denote an embedding algorithm such as PSSA. For a fixed hardware graph  $H$  we define the embedding probability

$$p_{\text{emb}}(|V(I)|, H, \mathcal{G}, \mathcal{A})$$

as the ratio of input samples from graph class  $\mathcal{G}$  restricted to graphs of vertex size  $|V(I)|$  for which the embedding algorithm  $\mathcal{A}$  finds a minor embedding.

Note that the probabilistic nature of the embedding probability originates both from the potentially probabilistic elements of the embedding algorithm as well as the probabilistic nature of the input graphs. Further note that, the definition of the embedding probability may in principal be augmented by including further dependencies, such as the number of edges  $|E(I)|$  of an input graph. In this paper, we chose the number of vertices  $|V(I)|$  because it directly corresponds to the number of spins of the input problem. In addition, for all graph classes considered in this paper the number of edges  $|E(I)|$  immediately follows from  $|V(I)|$ .

In this paper we will evaluate the embedding probability on a fixed hardware graph  $H$  for ever larger sizes  $|V(I)|$  of the input graphs  $I \in \mathcal{G}$ . Up to fluctuations this typically results in a monotonically decreasing function with high embedding probability at small sizes of  $|V(I)|$  and zero probability for large sizes of  $|V(I)|$ . See Fig. 3 for a preview. We then define the embedding threshold as follows.

**Definition 5 (Embedding Threshold)** Let  $H$  be a fixed hardware graph. Let  $\mathcal{G}$  denote a class of input graphs  $I \in \mathcal{G}$ . Let  $\mathcal{A}$  be an embedding algorithm and  $p_{\text{emb}}(|V(I)|, H, \mathcal{G}, \mathcal{A})$  the corresponding embedding probability. For a fixed constant  $p$  with  $0 < p \leq 1$ , we define the embedding threshold

$$\bar{V}(H, \mathcal{G}, \mathcal{A}, p) = \min\{|V(I)| \in \mathbb{N} \mid p_{\text{emb}}(|V(I)|, H, \mathcal{G}, \mathcal{A}) < p\}, \quad (4)$$

as the minimal vertex size  $|V(I)|$  for which the embedding probability  $p_{\text{emb}}$  falls below a prescribed threshold  $p$ .

Throughout this paper we will often denote the embedding probability as  $p_{\text{emb}}(|V(I)|)$  and the embedding threshold as  $\bar{V}(L)$  because: (i) The graph class  $\mathcal{G}$  (random cubic, Barábasi-Albert, or Erdős-Rényi) will always be specified from the context. (ii) The embedding algorithm  $\mathcal{A}$  will always be some version of PSSA whose details are specified from the context. (iii) The hardware graph  $H$  will always be a King's graph  $KG_{L,L}$ , whose size is either specified from context or through the side length  $L$ . The latter is convenient since the embedding threshold is often found to be a linear function of the side length  $L$  empirically. (iv) We fix the value of  $p$  at high and constant probability  $p = 0.95$ . (The precise value of  $p$  is usually not important, since the transition of  $p_{\text{emb}}(|V(I)|)$  from 1 to 0 as a function of increasing  $|V(I)|$  is usually quite sharp.)

## 2.6 Performance target and evaluation methodology

From the preceding discussion it is obvious that a good heuristic should never fall below the embedding threshold ensured by the best known complete graph embedding. Furthermore, a good heuristic should be able to maintain an embedding

threshold which exceeds the best known complete graph embedding as the size of the hardware graph increases. In particular, on a King's graph we want a heuristic which can maintain an embedding threshold  $\bar{V}(L) > L + 1$  as  $L$  increases.

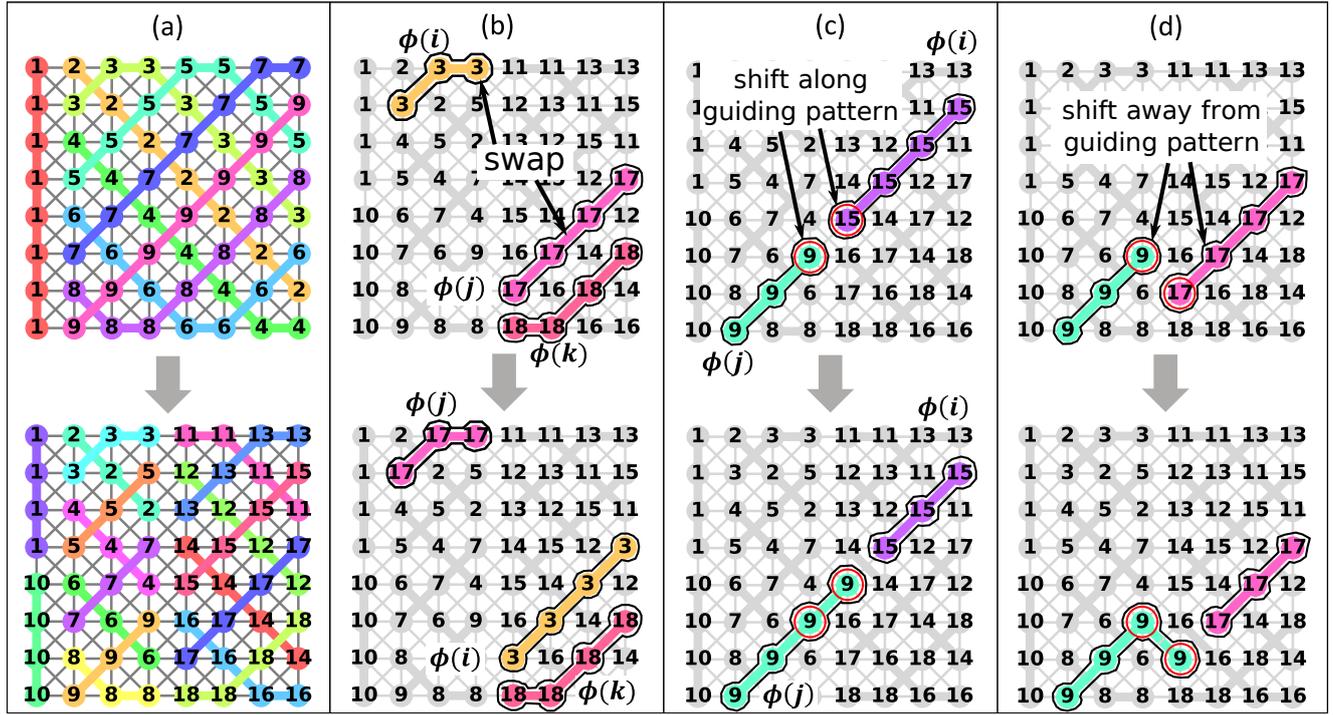
In this paper we will demonstrate that improved PSSA can maintain an embedding threshold  $\bar{V}(L) > L + 1$  even on large hardware graphs for certain types of input graphs, such as random cubic and Barábasi-Albert graphs. On the other hand, we also show that not even improved PSSA can beat the embedding threshold of the best known complete graph embedding for Erdős-Rényi graphs as the size of the hardware increases. To corroborate these statements we will now introduce PSSA as previously described in (Sugie et al., 2018) in the next section. Subsequently, we introduce improved PSSA and tune it on hardware King's graphs with  $320 \times 320$  spins, as described in Sect. 4. Finally, we evaluate the embedding threshold of improved PSSA phenomenologically on King's graphs of ever larger size in Sect. 5.

## 3 Probabilistic-Swap-Shift-Annealing (PSSA)

In order to make this paper self-contained, we outline the core elements of the probabilistic-swap-shift-annealing heuristic, previously published in (Sugie et al., 2018).

For a given input graph  $I$  and a given hardware  $H$  PSSA tries to find a minor embedding by implementing the following general framework: (i) First, an *initial super vertex placement* representing the vertices of the input graph  $I$  on the hardware  $H$  is prepared. See Fig. 2(a). In general, the initial super vertex placement will not embed all edges of the input graph such that  $E_{\text{emb}}(\phi) < |E(I)|$ . In this case PSSA proceeds to the annealing search phase. (ii) In the annealing phase PSSA will successively propose new super vertex placements. To this end it either *swaps* two super vertices, see Fig. 2(b), or *shifts* hardware vertices from one super vertex to its neighbor, see Fig. 2(c, d). The proposed super vertex placement is accepted, if the number of embedded edges  $E_{\text{emb}}(\phi)$  grows. On the other hand, a proposed super vertex placement is accepted with finite probability, even if the number of embedded edges decreases. This avoids trapping the algorithm on incomplete super vertex placements which maximize  $E_{\text{emb}}(\phi)$  locally. (iii) The annealing search phase terminates, if a super vertex placement representing all edges of the input graph,  $E_{\text{emb}}(\phi) = |E(I)|$ , i.e., a valid minor embedding is found. Alternatively, PSSA may terminate unsuccessfully after reaching a maximum amount of prescribed iterations  $t_{\text{max}}$ , because a minor embedding was either not found or does not exist.

In addition to the general framework, PSSA is currently implemented with the following specifications: (i) PSSA uses super vertices  $\phi(i)$  which are parametrized as path on the hardware. (ii) *Initial super vertex placements* are generated



**Fig. 2** Visualizing the main components of PSSA on a King's graph  $KG_{8,8}$ . (a) The guiding pattern induced by the best known complete graph embedding of  $K_9$  and the division of its super vertices for initial placement. (b) Swapping of super vertices. (c, d) Shifting the leaves of a super vertex to its neighbor (c) along and (d) away from the guiding pattern. Each super vertex is marked by the corresponding vertex label of the input graph.

by splitting the super vertices of the best known complete graph embedding on  $H$  into  $|V(I)|$  super vertices of almost equal size to represent the vertices of the input graph  $V(I)$  on the hardware  $H$ . See Fig. 2(a) for an example on a King's graph. Incidentally, this guarantees that PSSA never falls below the embedding threshold of the best known complete graph embedding. In addition, this initial placement generates a super vertex placements where each super vertex has many neighbors resulting in a high connectivity of super vertices. This is expected to facilitate finding a minor embedding in the successive annealing search phase. (iii) A *swap* is implemented by randomly selecting an edge  $(i, k) \in E(I)$  and swapping the super vertex  $\phi(i)$  with a super vertex  $\phi(j)$ , adjacent to  $\phi(k)$  on  $H$ . See Fig. 2(b). (iv) A *shift* is implemented by randomly selecting a super vertex  $\phi(i)$  (with  $|\phi(i)| > 1$ ) and one of its leaf nodes  $u \in \text{Leaf}[\phi(i)]$ . The shift proposal is completed by deleting  $u$  from  $\phi(i)$  and attaching it to a leaf  $v$  of a neighboring super vertices  $\phi(j)$  on  $H$ . See Fig. 2(c, d). If a neighboring leaf  $v$  does not exist, the shift proposal is skipped and the algorithm proceeds to the next proposal. If there are multiple candidates for  $v$  the algorithm randomly selects one of the available nodes with equal probability. (v) PSSA further uses the super vertices of the best known complete graph embedding as a guiding pattern in order to distinguish two types of shift moves. See top of Fig. 2(a) for an example of the guiding pattern. A shift move

is along the guiding pattern, if the leaf  $u \in \text{Leaf}[\phi(i)]$  is attached to a leaf  $v \in \text{Leaf}[\phi(j)]$  with both  $u$  and  $v$  belonging to the same super vertex of the best known complete graph embedding. See Fig. 2(c). On the other hand, a shift move is away from the guiding pattern, if the leaf  $u \in \text{Leaf}[\phi(i)]$  is attached to a leaf  $v \in \text{Leaf}[\phi(j)]$  with  $u$  and  $v$  belonging to distinct super vertices of the best known complete graph embedding. See Fig. 2(d). PSSA favors shifts along the guiding pattern, in order to prioritize super vertices with diagonal orientation. This is expected to increase the connectivity of the super vertices, and thus, to prevent PSSA from getting trapped in a local maximum of the score function  $E_{\text{emb}}(\phi) < |E(I)|$ . For more details the reader is referred to the pseudo-code summary of improved PSSA, given in Algorithm 1.

*Schedule* – The original implementation of PSSA divides the annealing time into two search phases of equal length. During both phases the temperature is initialized at a finite value and then decreased to zero

$$T(t) = \begin{cases} T_0 \times \left(1 - \frac{2t}{t_{\max}}\right) & \text{if } 0 \leq t < \frac{t_{\max}}{2}, \\ T_{\frac{t_{\max}}{2}} \times \left(2 - \frac{2t}{t_{\max}}\right) & \text{if } \frac{t_{\max}}{2} \leq t \leq t_{\max}, \end{cases} \quad (5)$$

allowing for a finite acceptance of suboptimal moves in the beginning of each phase, while suppressing them towards the end of each phase. In the first search phase conventional PSSA suppresses shift moves which lead away from the

**Algorithm 1:** PSSA (Sugie et al., 2018)

---

```

Input   : Input graph  $I$  and hardware graph  $H$ 
Output  : Super vertex placement  $\phi_{best}$ 
Ensure  :  $|V(I)| \leq |V(H)|$ ,  $|E(I)| \leq |E(H)|$ 
Require : Function  $E_{emb}(\phi)$ , Eq. (3),  $t_{max}$ , schedule,
           guiding_pattern

// prepare initial placement of super vertices
1  $\phi \leftarrow$  guiding_pattern divided into  $|V(I)|$  super vertices;
  // see Fig. 2(a)
2  $\phi_{best} \leftarrow \phi$ ; if  $E_{emb}(\phi_{best}) = |E(I)|$  return  $\phi_{best}$  and terminate;
  // minor found

// improve super vertex placement through
  simulated annealing
3 for  $t = 0$  to  $t_{max}$  do
4   move  $\leftarrow$  swap or shift, randomly selected according to
   schedule;
5   if move is swap then // see Fig. 2(b)
6      $i, k \leftarrow (i, k) \in E(I)$ , randomly selected;
7      $j \leftarrow j \in V(I)$  with  $\phi(j)$  neighboring  $\phi(k)$  in  $H$ ,
     randomly selected;
8      $\phi_{proposed} \leftarrow \phi$  with  $\phi(i)$  and  $\phi(j)$  swapped;
9   else if move is shift then // see Fig. 2(c, d)
10     $i, u \leftarrow i \in V(I)$  with  $|\phi(i)| > 1$  and  $u \in \text{Leaf}[\phi(i)]$ ,
    both randomly selected;
11    allow_any_direction_shift  $\leftarrow$  true or false according
    to schedule;
12    if allow_any_direction_shift then // see
    Fig. 2(d)
13       $j, v \leftarrow j \in V(I)$ ,  $v \in \text{Leaf}[\phi(j)]$  with  $v$  adjacent to
       $u$  in  $H$ , randomly selected;
14    else // see Fig. 2(c)
15       $j, v \leftarrow j \in V(I)$ ,  $v \in \text{Leaf}[\phi(j)]$  with  $v$  adjacent to
       $u$  along guiding_pattern, randomly selected;
16     $\phi_{proposed} \leftarrow \phi$  with  $u$  deleted from  $\phi(i)$  and assigned
    to  $\phi(j)$ ;

// evaluate acceptance of proposed move
17  $\Delta E \leftarrow E_{emb}(\phi_{proposed}) - E_{emb}(\phi)$ ;  $T(t) \leftarrow$  temperature
    according to schedule;
18 if  $\exp(\Delta E/T(t)) > \text{random.float} \in [0, 1)$  then
  // accept and update
19    $\phi \leftarrow \phi_{proposed}$ ;
20   if  $E_{emb}(\phi_{best}) < E_{emb}(\phi)$  then
21      $\phi_{best} \leftarrow \phi$ ;
22     if  $E_{emb}(\phi_{best}) = |E(I)|$  return  $\phi_{best}$  and
    terminate; // minor found

23 return  $\phi_{best}$  // even if  $E_{emb}(\phi_{best}) < |E(I)|$ , i.e.,
    minor not found

```

---

guiding pattern. This policy is expected to protect PSSA from being trapped in suboptimal super vertex placements. If the first search phase fails to produce a valid minor embedding, PSSA enters the second phase. During that second phase we consider a wider search space by allowing for a higher proportion of shifts away from the guiding pattern. To this end, PSSA schedules shifts with probability  $p_s(t)$  and swaps with probability  $1 - p_s(t)$ . If a shift is proposed, an arbitrary shift direction is allowed with probability  $p_a(t)$ , while shifts along the guiding pattern are guaran-

teed with probability  $1 - p_a(t)$ . Both  $p_s(t)$  and  $p_a(t)$  probabilities are scheduled with simple linear schedules. The detailed scheduling parameters used in numerical experiments are summarized in the Appendix 8.1. For further comments on scheduling the reader is referred to Sect. 4.3 on improved annealing schedules.

## 4 Improvements of PSSA

In order to improve the performance of PSSA on large input graphs, we implemented several modifications which shall be described in the following. These include (i) an additional terminal search phase, (ii) a degree-oriented super-vertex shift rule, and (iii) optimized annealing schedules.

### 4.1 Terminal search phase

If standard PSSA fails to produce a valid minor embedding after  $t_{max}$  iterations, it usually returns a super vertex placements  $\phi_{best}$  (henceforth referred to as  $\phi$  for brevity) with two pertinent properties: (i)  $\phi$  occupies all vertices  $u \in V(H)$  of the hardware. This can potentially lead to unnecessary assignments  $u \in \phi(i)$  which are neither needed for preserving the connected structure of a super vertex  $\phi(i)$  nor for connecting super vertices  $\phi(i)$ ,  $\phi(j)$  with  $(i, j) \in E(I)$ . Even worse, these unnecessary super vertex assignments may obstruct potential connections between super vertices  $\phi(i)$ ,  $\phi(j)$  with  $(i, j) \in E(I)$ . (ii) The super vertex placement  $\phi$  returned by PSSA usually represents most edges of the input graph already ( $E_{emb}(\phi) \lesssim |E(I)|$ ). Thus, finding a few more path connecting super vertices  $\phi(i)$ ,  $\phi(j)$  with  $(i, j) \in E(I)$  may already result in a valid minor embedding which fulfills (M3). Hence, the terminal search tries to transform  $\phi$  into a valid minor embedding by addressing properties (i) and (ii) as follows. For details see the pseudo-code summary in Algorithm 2.

*Creating free hardware vertices* – First the hardware vertices  $u \in V(H) = \{0, \dots, |V(H)| - 1\}$  are iterated over repeatedly and it is checked by the subroutine `is_deletable( $\cdot$ )`, if  $u$  can be removed from its corresponding super vertex  $\phi(i) \ni u$ . In this step a vertex  $u$  is removable from  $\phi(i)$ , if (p1) removing  $u$  from  $\phi(i)$  does not destroy the non-empty connected structure of the super vertex  $\phi(i)$  (M1) and (p2) removing  $u$  from  $\phi(i)$  does not decrease the number of embedded edges  $E_{emb}(\phi)$ . Vertices  $u \in V(H)$ , which have been removed from a super vertex are collected in a set of *free* vertices

$$U = V(H) \setminus \left( \bigcup_{i \in V(I)} \phi(i) \right). \quad (6)$$

The cleanup process is terminated, if no more vertices  $u \in V(H)$  can be removed from their super vertex  $\phi(i) \ni u$  after

**Algorithm 2:** Improved PSSA with terminal search

---

```

Input   : Input graph  $I$  and hardware graph  $H$ 
Output  : Super vertex placement  $\phi$ 
Require : PSSA, is_deletable( $\cdot$ ), bfs_path( $\cdot$ )
// get super vertex placement from PSSA
1  $\phi \leftarrow \text{PSSA}(I, H)$ ;
// --- Start terminal search ---
// Create free hardware vertices
2 Init:  $U \leftarrow \emptyset$  // Set of free vertices
3 Init:  $u \leftarrow 0$  // hw vertex  $u \in V(H) = \{0, \dots, |V(H)| - 1\}$ 
4 Init: no_del  $\leftarrow 0$  // Vert. scanned since last del.
5 while no_del  $<$  ( $|V(H)| - 1$ ) do
    // scan hardware vertices  $u = \{0, \dots, |V(H)| - 1\}$ 
6    $i \leftarrow \phi^{-1}(u)$  // get preimage of  $u$ 
7   if ( $u \notin U$ ) and (is_deletable( $u, i$ )) then
    // shift  $u$  to set of free vertices
8      $\phi(i) \leftarrow \phi(i) \setminus \{u\}$ ;
9      $U \leftarrow U \cup \{u\}$ ;
10    no_del  $\leftarrow 0$ ;
11  else
12    no_del  $\leftarrow$  no_del + 1;
13   $u \leftarrow (u + 1) \bmod |V(H)|$  // check next hw vertex

// Find new super vertex links by breadth first
// search on graph induced by free vertices
14 for  $i = 0, \dots, |V(I)| - 1$  do
15   if  $\exists (i, j) \in E(I)$  with  $\phi(i), \phi(j) \subset H$  not connected then
    // search BFS path from  $\phi(i)$  to  $\phi(j)$ 
16    $\phi, U \leftarrow \text{bfs\_path}(i, j)$ 

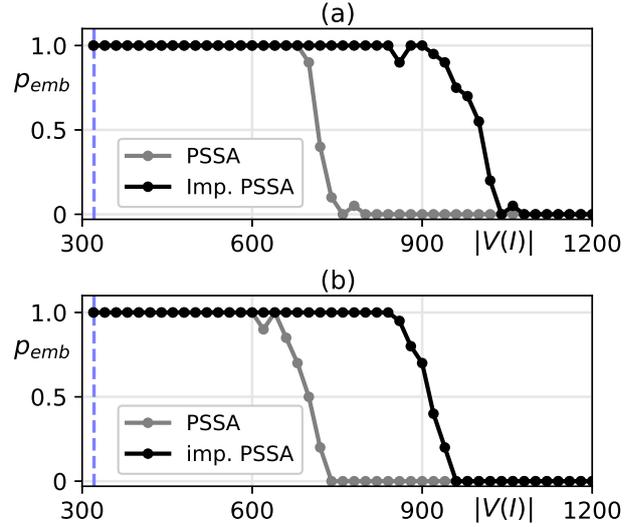
17 return  $\phi$  // even if  $E_{\text{emb}}(\phi) < |E(I)|$ , i.e., minor
    not found

```

---

a sweep of the whole hardware. For a possible implementation of the subroutine `is_deletable( $\cdot$ )` the reader is referred to Appendix 8.2.

*Super vertex links from breadth first search (BFS)* – After the cleanup phase the free hardware vertices  $u \in U$  are used to create representations of edges  $(i, j) \in E(I)$  whose super vertices  $\phi(i), \phi(j)$  are not yet linked on the hardware. As described in Algorithm 2 this is done by successively iterating through the vertices  $i = 0, \dots, |V(I)| - 1$  of the input graph and checking for edges  $(i, j) \in E(I)$  whose super vertices  $\phi(i), \phi(j)$  are not yet linked on the hardware. If such an edge is found the terminal search makes a call to the subroutine `bfs_path( $\cdot$ )` which tries to link up the super vertices  $\phi(i), \phi(j)$ . In this step breadth first search (Cormen et al., 2009) is used on the graph induced by the free vertices  $U$  on the hardware graph  $H$  to search for a path connecting the pair of super vertices  $\phi(i), \phi(j)$ . If such a path is found, the corresponding vertices are included in  $\phi(i)$  and deleted from  $U$ . The algorithm then proceeds to the next vertex pair  $\phi(i), \phi(j)$ . For a possible implementation of the subroutines `bfs_path( $\cdot$ )` the reader is referred to Appendix 8.2.



**Fig. 3** Comparing the empirical embedding probability (20 inputs) of PSSA (gray) and improved PSSA with terminal search (black) for (a) random cubic and (b) Barabasi-Albert type input graphs on a King's graph  $KG_{320,320}$  hardware. A (dashed) vertical line indicates the embedding threshold 321 of the best known complete graph embedding.

Note that the terminal search algorithm has already been a part of the original PSSA as designed by YY. However, since the terminal search phase had almost no impact on the embedding probability on King's graphs of moderate size ( $L = 52$ ) its details have previously been omitted in (Sugie et al., 2018). On the other hand, for large hardware King's graphs ( $L = 320$ ) the terminal search phase does have a profound impact on the embedding performance. This is depicted in Fig. 3 which compares the embedding performance of standard and the improved PSSA, showing that the improved PSSA allows for increasing the size of the embeddable input problems both for random cubic and Barabasi-Albert type input graphs  $I$ . For Erdős-Rényi-type input graphs with 20% edge density even the improved PSSA fails to construct minor embeddings for inputs beyond the embeddability threshold ( $|V(I)| > 321$ ) ensured by the existence of the best known complete graph embedding. Reasons for the difficulty of embedding Erdős-Rényi graphs will be discussed in Sect. 7.

We close this section with a short discussion: (i) Note that the terminal search phase will never decrease the number of embedded edges  $E_{\text{emb}}(\phi)$ . (ii) While PSSA produces super vertex placements  $\phi$  which occupy the whole hardware, the terminal search phase may leave hardware vertices unused. Similarly, while standard PSSA produces super vertices  $\phi(i)$  which induce a path in  $H$ , this property may be destroyed in the terminal search phase due to the deletion of vertices  $u \in V(H)$  as well as growing additional path. (iii) Breadth first search is an efficient algorithm for finding the shortest path between two vertices and two super vertices

can be connected by including all the vertices of the path into one super vertex. Searching for the shortest path is beneficial since the number of nodes needed to connect two super vertices is smallest. However, there is no guarantee that the shortest path between two super vertices is the optimal choice. In particular, there may be cases, where the shortest path connecting a pair of super vertices may obstruct the paths connecting another pair of super vertices, which could be avoided by choosing a longer path. For this reason the total number of links produced by the terminal search phase may depend on the order in which links between super vertex pairs are created by breadth first search. In a similar manner, the deletion of vertices  $u$  from their super vertex  $\phi(i)$  and thus the set  $U$  of free vertices may depend on the order in which the deletion of  $u$  is tried. Ultimately, it is not even guaranteed that the super vertex placement  $\phi$  produced by PSSA is necessarily the input which produces the largest amount of embedded edges in the terminal search phase.

#### 4.2 Degree-weighted shift proposals

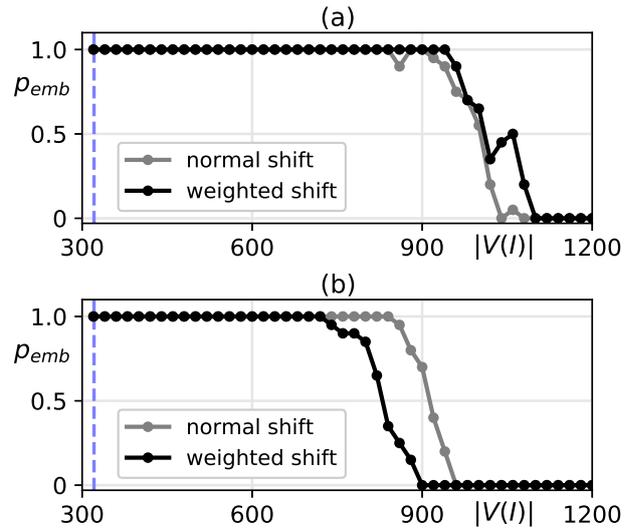
We further improve the PSSA embedding performance, by exploiting the degree distribution of the original input graph  $I$ . The basic idea is that vertices with a large amount of neighboring vertices should correspond to large super vertices comprising many nodes of the hardware, while nodes with few neighboring vertices should correspond to tiny super vertices, comprising only few vertices on the hardware. Most of our attempts to include the information on the degree distribution, in particular when creating the initial super vertex placement, went unsuccessful and shall not further be reported. However, including the information of the degree distribution to bias shift proposals, gave mild improvements on the embedding probability of random cubic graphs, see Fig. 4, and shall be described in more detail.

To begin with, the degree  $\deg(i)$  of a vertex  $i \in V(I)$  is defined as the number of edges incident to the vertex  $i$ . On the other hand, the size of the corresponding super vertex  $\phi(i) \subset V(H)$  shall be denoted as  $|\phi(i)|$ . The degree-weighted shift rule is then applied as follows. First, we schedule two neighboring leaf nodes  $u, v$  with  $u \in \phi(i), v \in \phi(j)$  for a shift move exactly as in conventional PSSA. Subsequently, we compute the degree ratio's, which we define as

$$dr(x) := \frac{|\phi(x)|}{\deg(x)} \quad x = i, j \in V(I), \quad (7)$$

as a measure to which extent the vertex size matches the degree of the input graph. Finally, we propose assigning  $u \in \phi(i)$  to  $\phi(j)$  with probability

$$\mu(u \in \phi(i) \rightarrow u \in \phi(j)) := \frac{dr(i)}{dr(i) + dr(j)}, \quad (8)$$



**Fig. 4** Comparing the empirical embedding probability (20 inputs) of improved PSSA with (black) and without (gray) degree-weighted shift proposals for (a) random cubic and (b) Barabasi-Albert type input graphs on a King's graph  $KG_{320,320}$  hardware. A (dashed) vertical line indicates the embedding threshold 321 of the best known complete graph embedding.

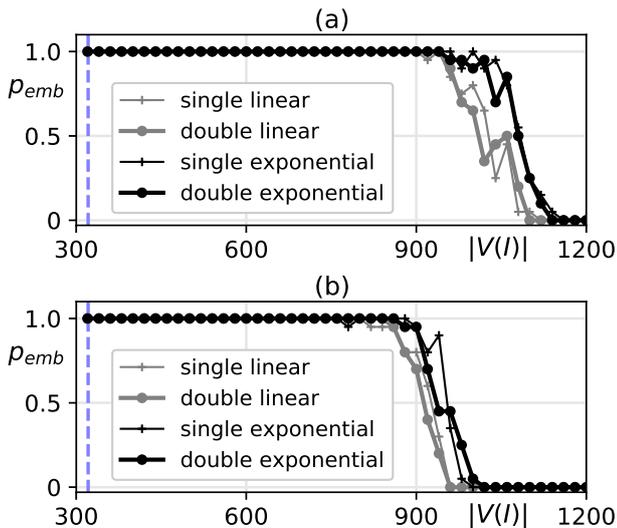
or alternatively propose shifting  $v \in \phi(j)$  from  $\phi(j)$  to  $\phi(i)$ . This biases the shift proposal to assign a leaf node to the super vertex with lower degree ratio.

In order to evaluate the impact of the degree-weighted shift proposal, we compared the embedding performance of improved PSSA using the conventional shift rule and the degree-weighted shift rule. In both cases we applied the terminal search phase. The embedding performance for a King's graph hardware  $KG_{320,320}$  is shown in Fig. 4, for (a) random cubic and (b) Barabasi-Albert-type input graphs. The degree-weighted shift rule shows mild improvements for random cubic graphs. Surprisingly, it clearly decreases the embedding probability for Barabasi-Albert graphs, for which its design was originally intended. Finally, it has no effect on the embedding probability of Erdős-Rényi graphs with 20% edge density. Those remain embeddable only by resorting to the best known complete graph embedding of  $K_{321}$ .

#### 4.3 Improved annealing schedules

As a last step towards designing an improved PSSA, capable of embedding even more edges of a given type of random input graphs, we tried to optimize the functional form of the annealing schedules. In particular, we tested four different functional forms of the temperature schedule which shall henceforth be described in more detail.

*Schedules* – (s1) Our investigation started out with the double linear schedule of conventional PSSA, exactly as described in the last paragraph of Sect. 3. (s2) In addition, we



**Fig. 5** Comparing the empirical embedding probability (20 inputs) of improved PSSA using single or double linear (thin/thick gray lines) as well as single or double exponential (thin/thick black lines) schedules for (a) random cubic and (b) Barabasi-Albert type input graphs on a  $KG_{320,320}$  hardware. A (dashed) vertical line indicates the embedding threshold 321 of the best known complete graph embedding. Improved PSSA (a) includes (b) excludes degree-weighted shifts.

tried a single linear schedule which omits the second annealing phase of the double linear schedule and immediately jumps towards the terminal search phase of improved PSSA after completing  $t_{\max}/2$  annealing steps. (s3) The third temperature schedule we tried is a double exponential schedule. Its total runtime, gets exactly the same amount of annealing steps  $t_{\max}$  as the original double linear schedule. It further initiates the first and the second annealing phase at exactly the same temperatures  $T_0$  and  $T_{t_{\max}/2}$  as the original double linear schedule. However, rather than decreasing the temperature linearly, the temperature is decreased exponentially. To this end the temperature is updated every 1000 annealing steps by multiplying the current temperature with a cooling factor  $\beta < 1$ . A larger value of  $\beta$  corresponds to a slower cooling rate and tends to give better results. However, one has to ensure that the system is sufficiently cooled at the end of each annealing phase in order not to jump out of the optimal configuration. Here, we used the cooling rate  $\beta = 0.9999$ . (s4) The fourth and last schedule we tried is a single exponential schedule which is identical to the double exponential schedule in the first annealing phase. Subsequently it skips the second annealing phase and directly jumps to the terminal search phase of improved PSSA after completing  $t_{\max}/2$  annealing steps. Finally, we remark that the schedules  $p_s(t)$  and  $p_a(t)$  which coordinate swap and shift proposals as well as shift directions, remain exactly as described in the last paragraph of Sect. 3.

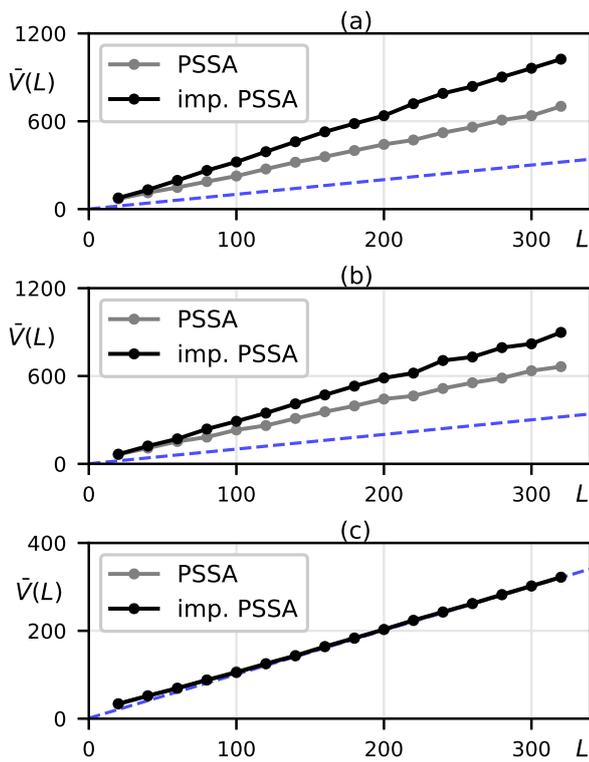
Admittedly, our methodology of improving the embedding performance based on the functional form of the an-

nealing schedule is rather phenomenological. Our motivation for doing so originates from our experience with simulated annealing on large spin systems, where we observed that exponential schedules tend to perform better than linear ones. In a similar manner our methodology is justified by the phenomenological results depicted in Fig. 5. In this figure we compare the performance of improved PSSA using the four different temperature schedules (s1-s4) for embedding (a) random cubic graphs and (b) Barabasi-Albert random graphs into a King's graph  $KG_{320,320}$ . Our results corroborate that the temperature schedules from the exponential family (black lines) tend to outperform the linear temperature schedules (gray lines), both on (a) random cubic and (b) Barabasi-Albert random graphs. In addition we observe that the performance of single and double linear as well as single and double exponential schedules, respectively, is identical within the bounds of statistical fluctuations. Meanwhile it has remained impossible to find a single instance of a random Erdős-Rényi graph with 20% edge density and more than 321 vertices which could be embedded into the King's graphs  $KG_{320,320}$  even with exponential scheduling.

## 5 Embedding performance on increasing hardware

Finally, we evaluate the empirical embedding threshold  $\bar{V}(L)$  of PSSA on hardware graphs of increasing size. To this end we proceed as follows: (i) We fix the size of the hardware by setting the parameter  $L = 20$ . (ii) Starting from  $|V(I)| = L$  we successively increase the size of the input problem. For each pair  $(L, |V(I)|)$  we create 20 input samples  $I_s, s = 1, \dots, 20$  and try to embed them into  $KG_{L,L}$  using (improved) PSSA. If at least 19 out of 20 input graphs could successfully be embedded we proceed by increasing the number vertices  $|V(I)|$ . The first time we find a pair  $(L, |V(I)|)$  for which less than 19 out of 20 cases were embeddable, we record  $|V(I)|$  as the embedding threshold  $\bar{V}(L)$  and reinitiate step (ii) on a larger King's graph  $L \leftarrow L + 20$ . We stop, if  $L > 320$ .

The results are shown in Fig. 6 which depicts the embedding threshold  $\bar{V}(L)$  up to which (improved) PSSA finds minor embeddings with 95% embedding probability on hardware King's graph  $KG_{L,L}$  of increasing size  $L$ . For (a) random cubic and (b) Barabasi-Albert type input graphs we phenomenologically observe a linear scaling of  $\bar{V}(L)$  with  $L$ . In both cases  $\bar{V}(L)$  approximately scales as  $\bar{V}(L) = c \times L$  with (a)  $c = 3.2$  and (b)  $c = 2.8$ . Thus it maintains a clear advantage over the deterministic minor embedding of  $K_N$  for which  $\bar{V}(L) = L + 1$ . In addition, this constitutes an average performance gain of 42% and 28%, respectively, over the previously published version of PSSA (Sugie et al., 2018). On the other hand, for (c) Erdős-Rényi type input graphs with 20% edge density  $\bar{V}(L)$  is hardly larger than  $L + 1$  even for small hardware graphs  $KG_{L,L}$ , eventually approaching the threshold of the best known complete graph embedding



**Fig. 6** Embedding threshold  $\bar{V}(L)$  of PSSA (gray) and improved PSSA (black) for increasing hardware King's graph  $KG_{L,L}$  for (a) random cubic, (b) Barabasi-Albert, and (c) Erdős-Rényi type input graphs. A dashed (blue) line indicates the minimal embedding threshold ensured by the existence of the best known complete graph embedding.

$K_{L+1}$  as  $L$  gets larger. The results in Fig. 6 use improved PSSA with terminal search phase and double exponential schedules. Degree-weighted shifts are applied only for random cubic graphs. A discussion of these results will be given in Section 7.

## 6 Can the best known complete graph embedding be improved?

The results of the previous section show that PSSA can maintain an embedding threshold  $\bar{V}(L)$  which exceeds the minimal embedding performance ensured by the best known complete graph embedding for certain inputs even on large hardware graphs. Yet, it also shows that the embedding threshold of Erdős-Rényi graphs with constant edge density cannot exceed the minimal embedding performance ensured by the best known complete graph embedding on large hardware graphs. This result emphasizes the outstanding role of the best known complete graph embedding as a baseline embedding which ensures a minimal embedding performance. This naturally raises two questions. (i) Can a King's graph host minor embeddings of larger complete graphs? (ii) Can

the hardware graph be optimized to host larger complete graphs?

In this section we address both issues in part. (i) We use the concept of treewidth to show that a King's graph  $KG_{L,L}$  cannot contain the minor embeddings of a complete graph  $K_N$  with  $N > 2L$  vertices. We believe this bound is still quite loose but cannot prove that the best known complete graph embedding hosting input graphs  $K_N$  with  $N = L + 1$  vertices is (close to) optimal. (ii) We show that any hardware graph  $H$  with bounded coordination number  $d$  (a common restriction for quantum and CMOS annealers) can, at most, embed complete graphs with  $\mathcal{O}(\sqrt{|V(H)|})$  vertices. Both the King's graph and the Chimera graph take this order and are thus in some sense optimal. Note that the style of the paper will henceforth become more mathematical. A reader who is more interested in the discussion of our improved PSSA is advised to skip to the summary section.

### 6.1 Upper bound on complete graphs embeddable into a King's graph

In this section we prove that a complete graph  $K_N$  with  $N$  vertices cannot be embedded into a King's graph  $KG_{L,L}$ , if  $N > 2L$ . The cornerstone of our proof is the following property, based on the concept of treewidth, which will be defined further below.

*Property 1 (Halin (1976))* Let  $I$  and  $H$  be two graphs. If  $I$  is a minor of  $H$ , its treewidth  $\text{tw}(I)$  is smaller or equal than the treewidth  $\text{tw}(H)$  of  $H$

$$I \text{ being a minor of } H \Rightarrow \text{tw}(I) \leq \text{tw}(H). \quad (9)$$

We then exploit this property by identifying the input with a complete graph  $I = K_N$ , whose treewidth is known  $\text{tw}(K_N) = N - 1$  (Fomin and Kratsch, 2010). Finally, we identify  $H$  with a King's graph  $KG_{L,L}$  and prove the following upper bound on the treewidth of a King's graph further below

$$\text{tw}(KG_{L,L}) \leq 2L - 1. \quad (10)$$

Incidentally, this implies that a complete graph  $K_N$  with vertices  $N > 2L$  cannot be minor embedded into a King's graph  $KG_{L,L}$ , by means of property 1.

In order to prove Eq. (10) we require some additional definitions. Let  $H$  be a general graph. A path of the graph  $H$  is a sequence of vertices  $\langle v_1, v_2, v_3, \dots, v_n \rangle$  without any repetition such that  $(v_l, v_{l+1}) \in E(H)$  holds for all  $l = 1, \dots, n - 1$ . A cycle of the graph  $H$  is a sequence of vertices without any repetition  $\langle v_1, v_2, v_3, \dots, v_n \rangle$  such that  $(v_n, v_1) \in E(H)$  and  $(v_l, v_{l+1}) \in E(H)$  holds for all  $l = 1, \dots, n - 1$ . A graph  $H$  is connected, if for all the pairs of vertices  $v, v'$  ( $v \neq v'$ ), there is a path connecting  $v$  and  $v'$ . A tree  $\bar{T}$  is a connected graph without any cycle. Note that if  $H$  is a tree, there exists a unique path for each pair of vertices in  $V(H)$ .

**Definition 6 (Tree Decomposition (Robertson and Seymour, 1986))** A tree decomposition of  $H$  is a family  $\{X_i\}_{i \in \bar{I}}$  of vertex subsets  $X_i \subseteq V(H)$  together with a tree graph  $\bar{T}$  connecting the indices  $i \in \bar{I}$  of the subsets  $X_i$ , such that the following properties hold. The vertex subsets  $X_i \subseteq V(H)$  cover the vertices and edges of the graph  $H$  according to

- (T1)  $\bigcup_{i \in \bar{I}} X_i = V(H)$ ,  
 (T2) for every edge  $(v, v') \in E(H)$ , there exists  $i \in \bar{I}$  such that  $v, v' \in X_i$  holds.

In addition we require that

- (T3) for all  $i, j, k \in \bar{I}$ , if  $j$  is on the path of  $\bar{T}$  from  $i$  to  $k$ , then  $X_i \cap X_k \subseteq X_j$ .

Subsequently, for each tree decomposition, we define its width as  $\max_{i \in \bar{I}} |X_i| - 1$  through the subset  $X_i$  which contains the maximal amount of vertices  $|X_i|$ . Finally, the treewidth of a graph  $H$  is the minimal width among all the possible tree decompositions of  $H$ . The treewidth is denoted by  $\text{tw}(H)$ .

*Upper bound for treewidth of King's graph* – We now prove Eq. (10) by constructing a concrete tree decomposition of a King's graph and computing its width. To this end, let  $KG_{L,L}$  be the King's graph of size  $L \times L$  and denote its vertex set as

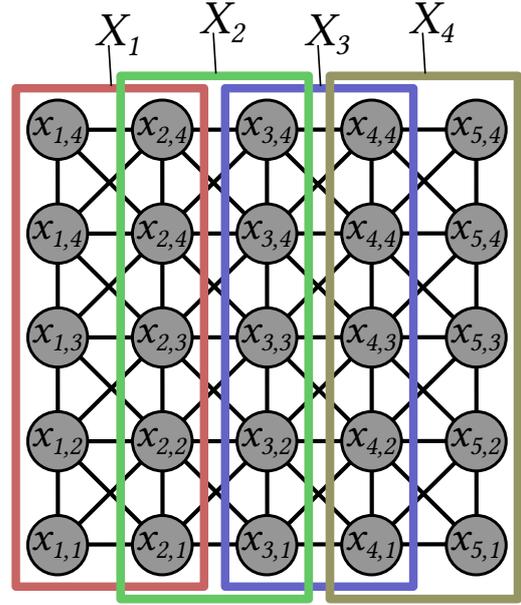
$$V(KG_{L,L}) = \{x_{i,j} \mid i, j = 1, \dots, L\}, \quad (11)$$

where  $x_{i,j}$  is the vertex located at the point  $(i, j)$  in the plane. See Fig. 7 for an example.

We construct a tree decomposition of the King's graph  $KG_{L,L}$  as follows: Let  $\{X_i\}_{i \in \bar{I}}$  be a family of vertex subsets

$$X_i = \{x_{i,j}, x_{i+1,j} \mid j = 1, \dots, L\}, \quad (12)$$

with  $i \in \bar{I} = \{1, \dots, L-1\}$ . Let  $\bar{T}$  be a tree on the index set  $(V(\bar{T}) = \bar{I})$  with edges  $E(\bar{T}) = \{(1,2), (2,3), \dots, (L-2, L-1)\}$  forming a simple path graph  $\langle 1, 2, 3, \dots, L-1 \rangle$  on the indices  $i$  of  $X_i$ . See Fig. 7 for an example. Then, the family of the subsets  $\{X_i\}_{i \in \bar{I}}$  along with the tree  $\bar{T}$  is a tree decomposition of  $KG_{L,L}$ . This can be checked as follows: (T1) holds because  $\bigcup_{i \in \bar{I}} X_i = V(KG_{L,L})$ . (T2) holds because (i) all horizontal edges  $(x_{i,j}, x_{i+1,j})$  with  $i = 1, \dots, L-1$  and  $j = 1, \dots, L$  are contained in  $X_i$ , (ii) all diagonal  $(x_{i,j}, x_{i+1,j+1})$  and anti-diagonal edges  $(x_{i+1,j}, x_{i,j+1})$  with  $i, j = 1, \dots, L-1$  are contained in  $X_i$ , (iii) vertical edges  $(x_{i,j}, x_{i,j+1})$  with  $i, j = 1, \dots, L-1$  are contained in  $X_i$  while (iv) vertical edges  $(x_{L,j}, x_{L,j+1})$  with  $j = 1, \dots, L-1$  are contained in  $X_{L-1}$ . (T3) holds as well which can be seen as follows: (i) For indices  $i, k$ , with  $|i-k| > 1$  the intersection  $X_i \cap X_k$  is empty and (T3) is fulfilled. (ii) For indices  $|i-k| = 1$  assume without loss of generality  $i < k = i+1$ . In this case  $j$  is either  $i$  or  $k$  and the intersection  $X_i \cap X_k = \{x_{i+1,j} \mid j = 1, \dots, L\}$  which is both a subset of  $X_i$  and  $X_{k=i+1}$ . (iii) Finally, consider the case  $|i-k| = 0$ . In this case  $j = i = k$  and  $X_i \cap X_k \subseteq X_j$  is



**Fig. 7** Illustration of the proposed tree decomposition for constructing the upper bound on the treewidth of a King's graph  $KG_{L,L}$  using the example  $L = 5$ . The corresponding sets  $X_i$  for  $i = 1, 2, 3, 4$  are indicated by boxes with thick fat boundaries.

also true. Altogether this shows that our above definition is a proper tree decomposition.

To complete the proof of Eq. (10) we compute the width of the tree decomposition, given as  $\max_{i \in \bar{I}} |X_i| - 1 = 2L - 1$ , since all sets in the decomposition contain  $2L$  vertices, i.e.  $|X_i| = 2L \forall i \in \bar{I}$ . By the definition of the treewidth, we conclude that  $\text{tw}(KG_{L,L}) \leq 2L - 1$ .

## 6.2 Embedding complete graphs into hardware with fixed coordination number

We now touch upon the question of constructing an alternative hardware graph, which may potentially embed larger complete graphs.

*Hardware graph with a fixed coordination number* – To start with, let  $H$  be a connected hardware graph. Since we are evaluating the question of an optimal hardware graph for the embedding of complete graphs, we will not yet fix its concrete structure. For the moment, we only specify a fixed upper bound on the coordination number  $d$  for each vertex of the hardware graph  $H$ . We believe that a fixed upper bound  $d$  on the coordination number of each vertex is a reasonable hardware restriction which cannot easily be overcome in the foreseeable future. In particular, current quantum annealers (D-Wave Systems Inc., since 2007) can hardly couple more than a few super-conducting quantum bits due to technical restrictions. On the other hand, CMOS annealers (Okuyama et al., 2017; Takemoto et al., 2019) exploit the sparsity of the hardware graph for parallel simultaneous spin updates

and thus require a fixed upper bound on the coordination number. In order to avoid pathological cases we assume  $d > 2$ . (If  $d = 2$ ,  $H$  could at most be a cycle or a path graph).

We now show that hardware graphs with fixed upper bound  $d$  on the coordination number require a minimum of

$$|V(H)| \geq \frac{N(N-3)}{d-2} \quad (13)$$

vertices to host a minor of a complete graph  $K_N$  with  $N$  vertices. In order to prove this, recall that a complete graph  $K_N$  requires connecting each of its vertices to all of its other  $N-1$  vertices. However, a single vertex of the hardware graph can connect to at most  $d$  neighbors and can thus in general not be connected to  $N-1$  neighbors. On the other hand, a super vertex comprising a total of  $S$  vertices on the hardware can be connected to many more hardware vertices. More specifically, a super vertex with  $S$  vertices has  $S \times d$  incoming edges. In order to keep the super vertex connected we have to connect its vertices with at least  $(S-1)$  internal edges, which requires sacrificing at least  $2(S-1)$  incoming edges of the super vertex. (Note that each internal edge is incident to two vertices and thus equates to two incoming edges.) Finally, utilizing the remaining incoming edges (at most  $S(d-2) + 2$ ) to connect the super vertex to at least  $N-1$  hardware vertices which represent all other vertices of the original complete graph  $K_N$  requires  $S(d-2) + 2 \geq (N-1)$ . This results in a minimal size of a super vertex according to

$$S \geq \frac{N-3}{d-2}. \quad (14)$$

Further embedding a complete graph  $K_N$  requires the super vertices of all  $N$  vertices to take the aforementioned minimal size, thus, resulting in a hardware requirement as specified in Eq. (13).

Incidentally, the forgoing discussion demonstrates that for hardware graphs with fixed upper bound on the coordination number, the hardware spin resources  $|V(H)|$  are of order  $\Omega(N^2)$ . On the other hand, the number of vertices  $N$  of the largest embeddable complete graph is inevitably of order  $\mathcal{O}(\sqrt{|V(H)|})$ . Both for King's graphs and for Chimera graphs (Klymko et al., 2014) the best known complete graph embeddings fulfill the above orders and are thus optimal in a certain sense. On the other hand, it remains an interesting question for future research, if graph structures turning Eq. 13 into an equality exists for arbitrary  $d$ . If so, it would pave the way for constructing hardware graphs with more efficient resource utilization with respect to complete graphs.

## 7 Summary

We presented an improved version of PSSA and used it to evaluate the performance of embedding heuristics on hardware King's graphs of unprecedented size of 102,400 spins

as released with the latest CMOS annealing processor (Hitachi Ltd., 2018). The algorithmic improvements of PSSA included (i) an additional search phase, (ii) a degree-oriented super-vertex shift rule, and (iii) optimized annealing schedules. The embedding performance of the improved PSSA was investigated with respect to various types of input graphs for hardware graphs of increasing size. An embedding performance consistently exceeding the embedding threshold of the best known complete graph embedding by a factor of  $c > 1$  was observed for random-cubic ( $c = 3.2$ ) and Barábasi-Albert ( $c = 2.8$ ) graphs. This constitutes an average performance gain of 42% and 28%, respectively, over the previously published version of PSSA (Sugie et al., 2018). On the other hand, for sparse random graphs with constant edge density we observe that even the improved PSSA cannot exceed the embedding threshold of the best known complete graph embedding on large input graphs. Finally, we derived a new upper bound on the vertex number of complete graphs embeddable into a hardware King's graph and showed that its size attains the maximal attainable order on hardware structures with a fixed coordination number.

### 7.1 Discussion

We now discuss several open questions of our research. (i) Our results demonstrate that the improved PSSA can outperform the best known complete graph embedding on large hardware graphs for certain inputs, such as random cubic and Barábasi-Albert graphs. Yet, it remains a future task to evaluate whether the improved PSSA would also outperform the best known complete graph embedding for input graphs induced by concrete applications in quadratically unconstrained binary optimization. We believe that graph coloring problems or solving the clique problem (Lucas, 2014) on social networks are suitable candidate applications. (ii) It is currently unclear whether the improved PSSA performs close or far from optimality. To address this question it would be desirable to compare its embedding threshold to the optimal embedding threshold attainable by means of exact algorithms (Adler et al., 2011),

$$\bar{V}(H, \mathcal{G}, \mathcal{A}_{\text{PSSA}}, p) \leq \bar{V}(H, \mathcal{G}, \mathcal{A}_{\text{exact}}, p). \quad (15)$$

This would allow for evaluating the headroom for further improvements of PSSA. (iii) The results of Sect. 6 show that current hardware graphs are close to optimal for representing complete graphs. Yet, it remains a question of future research, if hardware graphs  $H$  could be optimized to increase the embedding threshold  $\bar{V}(H, \mathcal{G}, \mathcal{A}, p)$  for certain classes  $\mathcal{G}$  of input graphs. (iv) It remains a task for future research to develop easily accessible criteria which indicate whether an embedding heuristic such as improved PSSA can outperform the best known complete graph embedding for increasing hardware graphs on a certain class of input problems  $\mathcal{G}$ .

Empirically, we observed that PSSA can outperform the best known complete graph embedding on large hardware graphs for random cubic and Barabási-Albert graphs whose edge set grows only linearly in the number of vertices  $|E(I)| \propto |V(I)|$ . On the other hand, we observed that PSSA cannot outperform the best known complete graph embedding on large hardware graphs for Erdős-Rényi graphs whose thicker edge set grows quadratically with the number of vertices  $|E(I)| \propto |V(I)|^2$ . Yet, it is by no means clear, that the reverse should hold. That is, we cannot prove that the number of edges scaling linearly in the size of the vertex set would guarantee embedding performance superior to the best known complete graph embedding. Similarly, it is unclear, if the number of edges growing quadratically in the number of vertices necessarily implies that the embedding threshold shrinks to the performance of the best known complete graph embedding as the hardware increases. (v) The main objective of improved PSSA is a high embedding threshold which outperforms the best known complete graph embedding even on large hardware graphs. In particular for input problems where this objective fails, it is advisable to optimize the minor embedding heuristic with respect to other objectives. Such an objective could, for example, be the runtime of the embedding heuristic (Goodrich et al., 2018). In addition, a good minor heuristic should attempt to minimize the size of its super vertices to avoid invalid solutions in the subsequent annealing phase (Boothby et al., 2016; Venturelli et al., 2015). This secondary objective has partially been addressed by the cleanup process in the terminal search phase of our improved PSSA. Investigating its effect in terms of precise data on the final distribution of super vertex sizes, before and after the cleanup of improved PSSA, remains a subject of future research.

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## 8 Appendix

### 8.1 Experimental conditions

*Random cubic* graphs are generated using Algorithm 1 from (Steger and Wormald, 1999) for a target of  $|V(I)|$  vertices of degree  $d = 3$ . Note that this implies that the number of edges grow as  $|E(I)| = 3|V(I)|/2$ .

*Barabasi-Albert* graphs are generated as described in (Albert and Barabási, 2002). In order to keep the graph connected we start out with  $m_0 (= 2)$  connected vertices. We then successively add new vertices to the graph. Every time we add a new vertex we connect it with the existing vertices by adding  $m (= 2 \leq m_0)$  edges based on preferential attachment. The procedure is repeated until the graph has reached a prescribed number of vertices  $|V(I)|$ . Note that the final graph has  $|E(I)| = m_0(m_0 - 1)/2 + m(|V(I)| - m_0)$  edges.

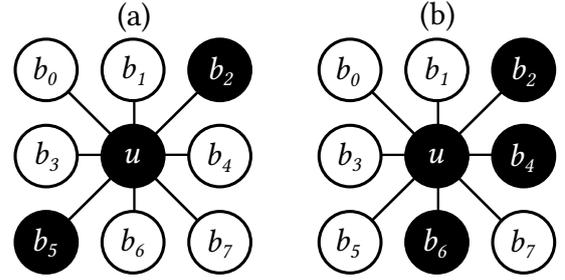
*Erdős-Rényi* graphs are created by growing a tree up to the desired number of vertices. To this end we add one vertex at a time and connect it to one of the existing vertices with equal probability. Subsequently, we add edges to the tree by filling unoccupied edges with equal probability until the prescribed edge density  $\rho$  is reached. The slight modification from the standard Erdős-Rényi procedure ensures that the resulting random graph is connected. Note that the number of edges of our random graphs grows as  $|E(I)| = \rho|V(I)|(|V(I)| - 1)/2$ . In this paper we always set  $\rho = 0.2$  using an edge density of 20%. Our results on the scalability do not crucially depend on the precise value of  $\rho$ , that is, for large hardware graphs PSSA cannot improve over the embedding performance of the best known complete graph embedding, also for other values of  $\rho$ .

*Schedule parameters* – All data in this paper is produced using a maximum of  $t_{\max} = 7 \times 10^7$  iterations and initial temperatures  $T_0 = 60.315$  and  $T_{t_{\max}/2} = 33.435$ . Linear schedules always terminate each annealing phase with temperature  $T = 0$ . Exponential schedules use a cooling coefficient  $\beta = 0.9999$  to update the temperature every 1000 annealing steps as  $T \leftarrow \beta * T$ . Swap and shift proposals are scheduled with linear schedules using  $p_s(0) = 1, p_s(t_{\max}) = 0, p_a(0) = 0.095, p_a(t_{\max}) = 0.487$ .

### 8.2 Implementation of the terminal search phase

In this appendix we describe possible implementations of the subroutines `is_deletable(·)` and `bfs_path(·)` as required in the terminal search phase of the improved PSSA.

The subroutine `is_deletable(·)` returns that a hardware vertex  $u \in V(H)$  is deletable from its super vertex  $\phi(i)$ , if both (p1) deleting  $u$  from  $\phi(i)$  does not destroy the non-empty connected structure of the super vertex (M1) and (p2) deleting  $u$  from  $\phi(i)$  does not decrease the number of embedded edges  $E_{\text{emb}}(\phi)$ . The subroutine `is_deletable(·)` checks



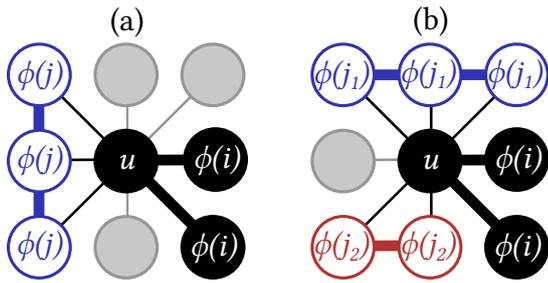
**Fig. 8** Illustration of the bit pattern encoding the neighborhood of  $u \in V(H)$ . Bits  $b_j$  of neighboring vertices belonging to the same super vertex as  $u$  are set to 1 and shown in black, while bits belonging to a super vertex different from  $u$  are set to 0 and shown in white. Bit patterns for which (a)  $u$  is not deletable and (b)  $u$  is deletable from its super vertex without destroying property (M1), respectively.

for property (p1) by encoding the super vertex occupation of the 8 neighboring vertices  $v_0, \dots, v_7 \in V(H)$  of  $u$  with  $(u, v_v) \in E(H)$  into a pattern of 8 bits  $b_v, v = 0, \dots, 7$ . See Fig. 8. In particular, the  $v$ th bit is set to 1, if  $v_v$  belongs to the same super vertex  $\phi(i)$  as  $u$  and 0 otherwise

$$b_v = \begin{cases} 1 & \text{if } v_v \in \phi(i) \text{ with } u \in \phi(i), \\ 0 & \text{if } v_v \notin \phi(i) \text{ with } u \in \phi(i). \end{cases} \quad (16)$$

The subroutine `is_deletable(·)` then checks property (p1) by computing the bit pattern of the current vertex  $u$  and comparing it to a precomputed list of deletable patterns. Deletable patterns have been obtained by inspecting all the 256 possible bit patterns and hard coding the deletable ones into the subroutine. If the bit pattern of the current vertex  $u$  is not in the list of deletable bit patterns, the subroutine decides that  $u$  is not deletable and returns. If the bit pattern of the current vertex  $u$  is in the list of deletable bit patterns, the subroutine proceeds to checking (p2).

To check if  $u$  is deletable in the sense of (p2), the subroutine proceeds as follows. First, it scans the 8 neighbors  $v_v, v = 0, \dots, 7$  of  $u \in \phi(i)$  and checks the corresponding edges  $(u, v_v) \in E(H)$ . During this process the corresponding pre-images  $j_v = \phi^{-1}(v_v) \in V(I), v = 0, \dots, 7$  are computed. If none of the pairs  $(i, j_v)$  represents an edge of the input graph  $(i, j_v) \in E(I)$  the subroutine decides that  $u$  is deletable and returns. On the other hand, for every pair  $(i, j_v) \in E(I)$  which represents an edge of the input graph the subroutine records the vertex  $j_v \in V(I)$  in a unique and sorted list. The number of occurrences  $n(i, j_v)$  is tracked in a corresponding list. Finally, the subroutine checks if  $\forall j_v$  in the unique and sorted list of vertices the amount of hardware representations  $n(i, j_v)$  of the edge  $(i, j_v)$  is smaller than the total number of hardware representations  $N(i, j_v)$ . If this condition is fulfilled, the subroutine updates  $N(i, j_v) \leftarrow N(i, j_v) - n(i, j_v)$  for all  $\forall j_v$  in the unique and sorted list of vertices and returns with  $u$  being deletable. Otherwise, it returns with  $u$  not being deletable. Note that the data on the amount of hardware edges  $N(i, j)$  representing the edge  $(i, j) \in E(I)$



**Fig. 9** Illustration of (a) a non-deletable and (b) a deletable vertex  $u$  in the sense of (p2). (a) Checking the neighborhood of the vertex  $u \in \phi(i)$  gives  $n(i, j) = 3$  hardware representations of the edge  $(i, j) \in E(I)$  and five vertices and edges (gray and black), respectively, which do not represent an edge of the input graph. Assuming that  $\phi(i)$  and  $\phi(j)$  have no further links elsewhere on the hardware, results in  $u$  being not-deletable. (b) Checking the neighborhood of the vertex  $u \in \phi(i)$  gives  $n(i, j_1) = 3$  hardware representations of the edge  $(i, j_1) \in E(I)$  and  $n(i, j_2) = 2$  hardware representations of the edge  $(i, j_2) \in E(I)$ . Furthermore, there are three vertices and edges, respectively, (gray and black) which do not represent an edge of the input graph. Since,  $\phi(i)$  is linked with  $\phi(j_1)$  by more than  $n(i, j_1) = 3$  edges and  $\phi(i)$  is linked with  $\phi(j_2)$  by more than  $n(i, j_2) = 2$  edges,  $u$  is deletable from  $\phi(i)$ .

on the hardware has to be computed before the subroutine `is_deletable( $\cdot$ )` is called for the first time. A sketch illustrating the check of deletability in the sense of (p2) is illustrated in Fig. 9.

The subroutine `bfs_path( $\cdot$ )` will operate on the hardware graph  $H$ . It will try to create a hardware link between  $\phi(i)$  and  $\phi(j)$  using the breath first search algorithm described in (Cormen et al., 2009, pp 594-602) with slight modifications, as follows: (i) The queue will be initialized by including all vertices of  $\phi(i)$  into the queue, marking their current status as gray, i.e., in the queue. The free hardware vertices  $U$ , Eq. (6), are initialized as white, i.e., unvisited. The vertices of  $\phi(j)$  are marked as green, i.e., target reached. Finally, all other vertices are marked as red, denoting occupied vertices of the hardware. (ii) The subroutine `bfs_path( $\cdot$ )` will then successively dequeue vertices  $u$  from the queue and check all its adjacent nodes  $v$  in  $H$ . If  $v$  is an occupied or a visited node, it will be skipped. If  $v$  is an unvisited node,  $v$  is enqueued,  $u$  is registered as its parent and  $v$ 's status is set to gray, i.e., in the queue. Finally, if  $v$  is a target node with  $v \in \phi(j)$ , breadth first search is stopped and the subroutine proceeds to the cleanup. After checking all nodes  $v$  adjacent to  $u$  in  $H$  the color of  $u$  is updated to black, i.e., visited and breadth first search proceeds to dequeuing the next vertex from the queue. (iii) If a target node  $v \in \phi(j)$  is found, its parents are traced back to  $\phi(i)$  and the corresponding path of vertices is removed from the the set of free hardware vertices  $U$ , Eq. (6), and assigned to the super vertex  $\phi(i)$ . After doing so `bfs_path( $\cdot$ )` returns successfully and proceeds to the next edge  $(i, j) \in E(I)$  whose super vertices  $\phi(i), \phi(j)$  are not yet linked on the hardware  $H$ . Alternatively, `bfs_path( $\cdot$ )` might

return unsuccessfully with an empty queue without hitting a single target vertex. In this case  $U$  and  $\phi$  remain unchanged.