Low-power integrated transmitter design using frequency multiplication techniques

Edge-combining and third harmonic extraction

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This paper proposes an approach to employ frequency multiplication techniques like edge-combining and third harmonic extraction in ultra-low-power integrated transmitter design. The overall power demand of the transmitter is reduced by keeping operating frequency of its components low. For that reason, edge-combining and third harmonic extraction are integrated directly into a switched mode power amplifier. Hence, the radio frequency signal is generated just before it is fed to the antenna. This leads to a reduced power demand of the overall transmitter in comparison to conventional designs where the oscillator and other components are operated directly at the radio frequency.

Within this paper we propose an amplifier that generates a 2.4 GHz carrier frequency from a ring oscillator running at a low 200 MHz resulting in a frequency multiplication factor of twelve. The exemplary design is targeted to be used in ultra-low-power short range applications. Hence, our simulations using extracted layout models show that the amplifier provides an output power of approximately -12 dBm at a supply voltage of 0.6 V while consuming 2.4 mW of power fully integrated in a 180 nm 1P6M CMOS process.

This demonstrates that the proposed techniques are especially suitable for ultra-low-power transmitter in short range applications. That includes medical and body area network applications.

Keywords: edge-combining; frequency multiplication; low power; third-harmonic extraction; transmitter

Entwurf integrierter Sender zur Verringerung des Leistungsbedarfs unter Verwendung von Frequenzmultiplikationstechniken: „Edge-Combining" und Extraktion der dritten Oberwelle.

In diesem Artikel wird ein Ansatz zur Anwendung von Frequenzmultiplikationstechniken, wie „Edge-Combining" und Extraktion der dritten Oberwelle, bei integrierten Sendern mit geringem Leistungsverbrauch präsentiert. Dabei wird der Gesamtleistungsbedarf des Senders verringert, indem die Betriebsfrequenz seiner Komponenten gesenkt wird. Für diesen Zweck können die Methoden „Edge-Combining" und Extraktion der dritten Oberwelle direkt in den Leistungsverstärker integriert werden. Das Hochfrequenzsignal wird dadurch erst direkt an der Antenne erzeugt.

Im Vergleich zu herkömmlichen Architekturen, bei denen der Oszillator und andere Komponenten auf der Sendefrequenz betrieben werden, führt die dadurch erreichte Senkung der Betriebsfrequenz zu einem reduzierten Leistungsverbrauch. Zur Veranschaulichung der Konzepte wird in diesem Artikel ein Verstärker vorgestellt, der eine Trägerfrequenz von 2,4 GHz aus einem 200-MHz-Ringoszillator erzeugt, was zu einer Frequenzmultiplikation um den Faktor zwölf führt. Die Schaltung ist für Kurzstreckenanwendungen bei geringem Leistungsverbrauch ausgelegt. Die Simulationsergebnisse unter Verwendung von extrahierten Layout-Modellen zeigen, dass der Verstärker eine Ausgangsleistung von ungefähr -12 dBm bei einer Versorgungsspannung von 0,6 V liefert. Der Verstärker ist vollintegriert in einem 180 nm-1P6M-CMOS-Prozess und besitzt einen Gesamtleistungsverbrauch von 2.4 mW.

Das Beispiel zeigt, dass die vorgeschlagenen Techniken besonders geeignet sind für leistungseffiziente Sender in Nahbereichsanwendungen wie beispielsweise Medizinanwendungen und Körperbereichsnetzwerke.

Schlüsselwörter: Edge-combining; Frequenzmultiplikation; geringer Leistungsverbrauch; dritte Obwerwelle; Sender

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1. Introduction

In recent years the Internet-of-Things (IoT) is expanding rapidly. It connects many autonomous nodes, often by using wireless networks. As most of the nodes are battery powered, they need to have a low power consumption in order to extend charging cycles and battery lifetime. The power demand of the devices is mainly defined by the transmitter as it needs energy to transmit data over a range of a few meters. Several approaches have been proposed with the target to reduce power demand in integrated transmitter design as [11] summarizes.

One approach to decrease the power consumption of the transmitter is to correspondingly reduce the complexity as well as the number of components. The simplest architecture just consists of an oscillator that runs at radio frequency. It is switched on and off (OOK,

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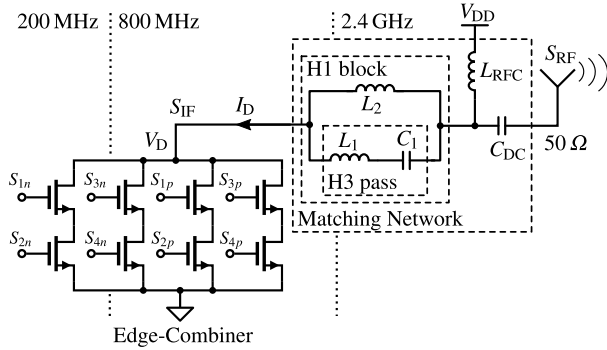
Fig. 1. Edge-combining power amplifier with third-harmonic extraction

Fig. 2. Edge-combining using a 4-stage differential ring oscillator for $4\times$ frequency multiplication

on-off-keying) for information transmission. In this case, the oscillator frequency is not regulated and suffers from high frequency-inaccuracy. The architecture can be used in impulse-radio ultra-wideband (IR-UWB) transmitters [1, 10] as high frequency accuracy is typically not needed there. Moreover, often IR-UWB transmitters are highly duty-cycled and are transmitting only one pulse during a long time period. Therefore, advanced implementations utilize fast startup oscillators [10].

Narrow-band transmitters need a regulated oscillator in order to fulfill spectral regulations summarized in frequency accuracy and phase noise requirements. Hence, they are often locked to a reference oscillator by using either injection locking or a phase locked loop. Injection locking architectures [4, 9, 12] have the lowest power demand as they are directly locked to the reference oscillator and do not need a regulation loop. In general, as reference oscillators run at a low frequency, this architecture is only suitable for a transmit frequency below 1 GHz. If a higher frequency and flexible frequency adjustment is needed a phase locked loop (PLL) is utilized. Several PLL architectures [5, 8] apply an oscillator directly running at radio frequency. The output signal is either sent directly, or amplified by a power amplifier, depending on the desired output power, to the antenna.

This work proposes a way to further reduce power demand of the transmitter by using frequency multiplication techniques. The general idea is to save power by keeping the frequency of the transmitter components low. Therefore, the oscillator and frequency regulation do not run at radio frequency. The transmit signal is generated directly before the antenna by using either of the two methods—edge-combining or third harmonic extraction. Both methods are shown in this paper and a possibility to integrate them into the power amplifier is proposed as pictured in Fig. 1. A radio frequency signal S_{RF} at 2.4 GHz is generated by an eight-stage differential ring oscillator running at 200 MHz. The ring oscillator node signals $S_{k\{p|n\}}$ are in a first step used for four times frequency multiplication to an intermediate frequency signal S_{IF} at 800 MHz by applying a method called edge-combining. In doing so the time delay output signals of the ring oscillator are connected logically in order to generate pulses. These pulses are added up to generate the radio frequency signal S_{RF} as discussed in detail in Sect. 2.1. Similar approaches can be found in [2, 7, 9, 12].

However, this work goes one step further and additionally extracts the third harmonic frequency from S_{IF}. For this procedure, the output matching network is utilized to block the fundamental frequency while the third harmonic is matched and thus fed to the output of the transmitter. Therewith, an additional inherent multiplication factor of three is gained, leading to a reduced power con-
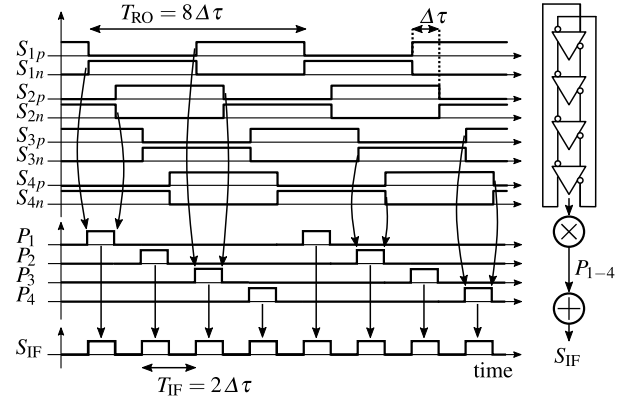
sumption especially at a low output power as shown in Sect. 4. The presented methods are suitable for low-power applications where only small output power values needed, for example, body area networks and medical applications.

The paper is structured as follows: Initially, Sect. 2 introduces edge-combining and third harmonic extraction. Then in Sect. 3 an approach is shown how both techniques can be implemented in integrated circuits for switched-mode power amplifiers. Finally, in Sect. 4 an exemplary design is evaluated by simulation and Sect. 5 concludes the work and gives a short outlook.

2. Frequency multiplication techniques
As mentioned in the introduction (cf. Sect. 1) several techniques have been published in order to reduce the power demand of low power integrated transmitters. In this section two methods—edge-combining and third-harmonic extraction—that keep the operating frequency of the transmitter components low and perform frequency multiplication are discussed.

2.1 Edge-combining
Edge-combining uses several time-delayed signals $S_{k\{p|n\}}$ at a low frequency f_{RO} and connects them logically in order to generate a high frequency signal S_{IF}. The time-delayed signals $S_{k\{p|n\}}$ are generated by a K-stage delay line having a unity delay of $\Delta\tau$. To illustrate the method a $K=4$ pseudo-differential ring oscillator with inverted feedback running at $f_{RO} = 1/T_{RO} = 1/(2k\Delta\tau)$ is utilized as pictured in Fig. 2 on the right side. It generates several $\Delta\tau$-shifted single-ended signals $S_{k\{p|n\}}$ at its nodes (2 per stage) as plotted on the left side. If the outputs of two consecutive stages (e.g. S_{1n} and S_{2n}) are multiplied, a pulse P_1 is generated at the points where the signals overlap. In the same manner several $2\Delta\tau$ time-shifted pulses P_1 to P_4 are generated as shown in Fig. 2. By adding up the pulses a signal S_{IF} having a frequency of $f_{IF} = 1/T_{IF} = 1/(2\Delta\tau)$ is created. In this example the generated frequency f_{IF} is 4-times higher (m_{EC}) than the oscillator frequency f_{RO}.

In general, using a K-stage delay-line results in a frequency multiplication factor $m_{EC} = K$ that equals the number of stages. However, the maximum frequency is not dependent on the number of stages but limited by the minimum $\Delta\tau$ that can be achieved by one delay stage as calculated in (1).

$$f_{IF} = m_{EC} \cdot f_{RO} = m_{EC} \cdot \frac{1}{2K\Delta\tau} = \frac{1}{2\Delta\tau} \tag{1}$$

Edge-combining can be implemented, for example, in hardware by using logical gates as pictured in Fig. 3. The multiplication of the
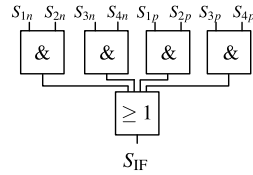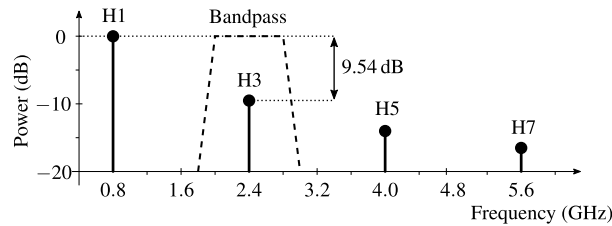
Fig. 3. Block diagram of the edge-combiner

Fig. 4. Extraction of the third harmonic from a rectangular signal using a band-pass filter

Fig. 5. Concept of switched-mode power amplifier

time-delayed signals is performed by an AND-gate and the addition of the pulses is realized as OR-gate. Several other implementation methods are shown in [7]. In this paper the edge combiner is realized by the circuit pictured in Fig. 1 and described in Sect. 3.2.

2.2 Harmonic extraction

Every continuously-differentiable periodic continued function $f(t)$ can be represented by a summation of oscillations at different frequencies and amplitudes also known as Fourier-series

$$f(t) = a_0 + \sum_{n=1}^{\infty} \left[a_n \cos(2\pi n f_1 t) + b_n \sin(2\pi n f_1 t) \right]. \tag{2}$$

The output voltages of the ring oscillator, logical gates and also the edge-combiner have a rectangular shaped output signal. A rectangular signal is an odd-signal and thus consists of odd-harmonic frequencies. By additionally having a single-ended signal ranging from e.g. 0–1 V and phase difference of $\varphi = 0\circ$ (2) simplifies to

$$v_{\text{rect}}(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos\left[2\pi(2n-1) f_0 t \right] \tag{3}$$

with the coefficients

$$a_0 = \frac{1}{2}, \quad a_n = \frac{2}{(2n-1)\pi}. \tag{4}$$

The resulting power spectrum of the rectangular Fourier-series (normalized to the fundamental H1) is plotted in Fig. 4. The signal exhibits power at odd multiples of the fundamental frequency $f_1 = 800$ MHz (H1). In order to perform frequency multiplication by the factor $m_{\text{H3}} = 3$, the third harmonic H3 has to be filtered from the spectrum by a band-pass as illustrated in Fig. 4. The proposed approach uses the output matching network of the switched-mode power amplifier to suppress the fundamental frequency and pass the third harmonic to the antenna (see Sect. 3.3).

3. Proposed design

Both frequency-multiplication techniques proposed in the previous section (Sect. 2) are integrated into a switched-mode power amplifier. Initially, the basic concept of the amplifier is explained by using a switch that is later on replaced by the edge-combiner and the output matching network is designed in order to extract the third harmonic
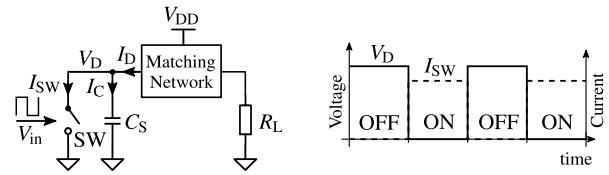
frequency. Hence, a radio frequency of $f_{\text{RF}} = 2.4$ GHz is generated from a ring oscillator frequency of $f_{\text{RO}} = 200$ MHz in two steps using the architecture pictured in Fig. 1. At first the edge-combiner performs a frequency multiplication of $m_{\text{EC}} = 4$ to generate a intermediate frequency signal S_{IF} at $f_{\text{IF}} = 800$ MHz. In a second step, an additional multiplication by $m_{\text{H3}} = 3$ is performed by extracting the third harmonic. That leads to an overall frequency multiplication factor of $m = m_{\text{EC}} \cdot m_{\text{H3}} = 12$ and an output signal S_{RF} at $f_{\text{RF}} = 2.4$ GHz.

3.1 Switched-mode power amplifier

The general block diagram of a switched-mode power amplifier is pictured in Fig. 5. The amplifier consists of a switch—controlled by the rectangular shape input voltage V_{in}—and a passive output matching network. In integrated CMOS circuits the switch is realized as a transistor typically showing a drain-source capacitance of C_{S}, an on-resistance R_{ON} and an off-resistance R_{OFF}. The output matching network provides power matching to the load R_{L} and forms the voltage V_{D} in order to reduce losses in the switch.

In theory, switched-mode power amplifiers have very low power dissipation $P_{\text{SW}} = I_{\text{SW}} \cdot V_{\text{D}}$ as either the switch-current I_{SW} (ideal: $R_{\text{OFF}} = \infty$) or switch-voltage V_{D} (ideal: $R_{\text{ON}} = 0$) are zero or near to zero. However, in hardware implementations the on-resistance will differ from $R_{\text{ON}} = 0\ \Omega$ and the off-resistance R_{OFF} will be finite. This causes losses in the switch as either a current (off-state) or a voltage (on-state) drop remains. As the switch is realized as a MOS-FET the resistance can be adjusted by the size. A large switch will reduce the on-resistance R_{ON} for better efficiency, but will also increase the overall power consumption and output power. For applications with limited power the switch must be designed according to the desired power consumption and output power.

In off-state the voltage V_{D} is dependent on the drain-source capacitance C_{S} and the output matching network. If the switch is opened while C_{S} is charged, the energy stored on the capacitor C_{S} will be lost from the system through the switch. That leads to a increased power dissipation and reduced efficiency. To avoid this effect zero voltage switching needs to be applied. That means that the capacitor C_{S} is discharged and the switch-voltage V_{D} is zero when the switch is opened. For this reason the matching network is designed in order to form the switch-voltage V_{D} to be zero at the switching points. Hence, the drain capacitance C_{S} is compensated, leading to matching the switch impedance including C_{S} to the load at the desired output frequency.

3.2 Edge-combiner

To further include the up-conversion procedure in the radio frequency amplifier, the switch of the switched-mode amplifier is replaced by the edge-combiner. The resulting circuit is shown in Fig. 1. The edge-combiner consists of four branches connected at the node V_{D}. Each branch is built up as a stacked NMOS-transistor pair. The gates of the transistors are connected to the ring oscillator nodes $S_{k\{p|n\}}$ as shown in Fig. 1 and Fig. 2. If the gate voltages, e.g. S_{1n} and S_{2n}, of both transistors located in one branch are pulled high to the supply voltage V_{DD}, the branch gets conductive and pulls
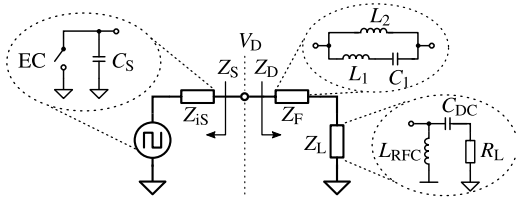
Fig. 6. Equivalent small-signal circuit of the edge-combining amplifier

Table 1. Requirements on the output matching network impedance

	$f_{IF} = 800$ MHz	$f_{RF} = 2.4$ GHz
Z_F	∞	0
Z_L	–	Z_S^*
Z_D	∞	Z_S^*

the node voltage V_D to the ground potential. Thereby a pulse P_1 is created (see Fig. 2). Like the first branch the other branches are used to generated the pulses P_2 to P_4. As the branches alternately pull the drain voltage V_D to ground a frequency f_{IF} of four times ($m_{EC} = 4$) the oscillator frequency f_{RO} is formed at node V_D. The edge-combiner shows the same behavior as having a single switch that is switched with a frequency of f_{IF}. Therefore it can be modeled as a switch having a parallel connected gate capacitance of C_S resulting in an output impedance of Z_S.

3.3 Output matching-network
For the presented design, the output matching network is designed to extract the third-harmonic frequency of the edge-combiner output S_{IF} (node voltage V_D) and perform an additional frequency multiplication by the factor $m_{H3} = 3$. A further target of the matching network is to suppress the fundamental frequency $f_1 = f_{IF} = 800$ MHz at its input as good as possible. Simultaneously, the third-harmonic frequency $f_3 = f_{RF}$ is matched to the load R_L to compensate the drain capacitance C_S. Moreover, the matching network needs to incorporate the functionality of a bias-tee and provide the supply voltage V_{DD} as well as a dc-block to avoid a direct current flowing into the load R_L.

The matching network is realized by the circuit shown in Fig. 1. L_1 and C_1 are designed to be a short at $f_{RF} = f_3$. However, by connecting L_2 in parallel to L_1 and C_1 a high resistance is created at the fundamental $f_{IF} = f_1$. L_{RFC} is needed to provide the supply voltage and C_{DC} is used as direct-current block. Moreover, L_{RFC} and C_{DC} are used to match the edge-combiner output to the load R_L.

In order to analyze the network and derived the values for its components, the output matching network is simplified to the circuit shown in Fig. 6. The edge-combiner is modeled as a rectangular voltage source having an input impedance of $Z_S = (43.6 - j45.3)\,\Omega$ (derived by extracted layout simulation) at the desired output frequency f_{RF}. The output matching network is divided into two impedance values Z_F and Z_L connected in series in order to reduce calculation complexity. The impedance Z_F is designed to realize a filter effect. It provides a high impedance at the fundamental frequency and a short at the third harmonic. In contrast Z_L is an equivalent representation of the load combined with the matching/biasing components L_{RFC} and C_{DC}. The requirements on $Z_D = Z_F + Z_L$ of the matching network are summarized in Table 1. Z_F and Z_L are dependent on the frequency f and components L_1, C_1, C_2, $L_{RFC}(f)$ and
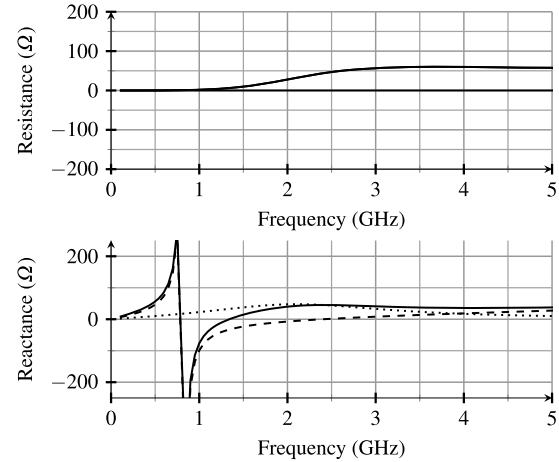

Fig. 7. Calculated impedance of the filter Z_F (- - -), the load Z_L ($\cdots$) and the resulting output matching network Z_D (—)

$C_{DC}(f)$ are calculated in (5) and (6), respectively.

$$Z_F(f) = \frac{2\pi f L_2 \left[C_1 L_1 (2\pi f)^2 - 1 \right]}{(C_1 L_2 + C_1 L_1)(2\pi f)^2 - 1} \tag{5}$$

Considering (5) the high impedance at f_{IF} is calculated by setting the denominator to zero ($Z_F^{-1} = 0$) and hence generating a pole at f_{IF}. Moreover, a short at f_{RF} is achieved by setting $Z_F = 0$ and thus bring L_1 and C_1 into resonance at f_{RF}. As calculating the values under given criteria provides one degree of freedom, L_2 is chosen to be 9.6 nH, and then $L_1 = 1.25$ nH and $C_1 = 3.51$ pF are calculated.

The equivalent load impedance $Z_L(f)$ is derived in (6). The values are calculated in order to match the third harmonic f_{RF} to the load R_L and thereby compensate the source capacitance C_S.

$$Z_L(f) = \frac{2\pi f L_{RFC} \left(j2\pi f C_{DC} R_L + 1 \right)}{j(2\pi f)^2 C_{DC} L_{RFC} + C_{DC} R_L 2\pi f - j} \tag{6}$$

Therefore, Z_L needs to be the conjugate complex value of Z_S as already shown in Table 1 (note that $Z_F(f_{RF}) = 0$ and has no influence on Z_D at f_{RF}). As mentioned before, the value for $Z_S(f_{RF})$ was determined to be $(43.6 - j45.3)\,\Omega$ by simulation with the extracted layout of the edge-combiner circuit. Consequently, the values for L_{RFC} and C_{DC} are calculated to be 3.1 nH and 1.47 pF, respectively. The resulting frequency-dependent impedance values Z_F, Z_L and their summation Z_D are plotted in Fig. 7. It can be observed that the impedance Z_D has the desired pole at $f_{IF} = 800$ MHz and a value of $Z_D(f_{RF}) = (43.6 + j45.3)\,\Omega$. Hence, the derived circuit fulfills the requirements summarized in Table 1. However, in the above consideration all passive components are ideal elements neglecting parasitics. As shown next in Sect. 4, the extracted component models will have parasitic effects that cause power dissipation and mismatch. Therefore, the lossy component values are adjusted due to the simulation results.

4. Simulation results and discussion
The proposed edge-combining amplifier with third-harmonic extraction is implemented in a 180 nm 1P6M CMOS process. To evaluate the expected performance of the proposed concept, post-layout parasitic extraction models of the main circuits are utilized. The edge-combining amplifier is driven by ring oscillator signals running at a frequency of $f_{RO} = 200$ MHz. It generates an intermediate frequency of $f_{IF} = 800$ MHz after the edge-combiner and results in an radio frequency signal of $f_{RF} = 2.4$ GHz after the third-harmonic frequency extraction by the matching network. The ideal component
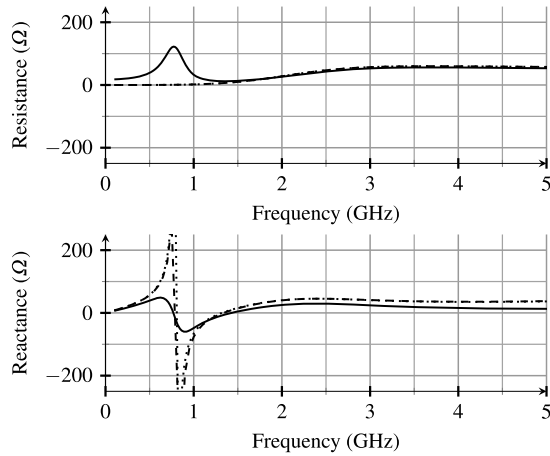
Fig. 8. Comparison between the calculated (- - -) and simulated impedance Z_D of the output matching network with ideal ($\cdots$) and extracted (—) components
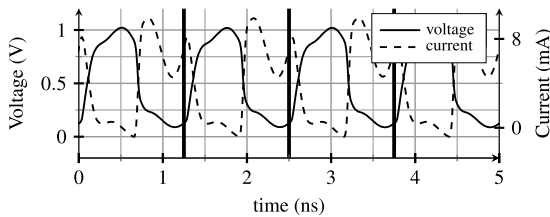

Fig. 9. Output voltage V_D and current I_D of the edge-combiner
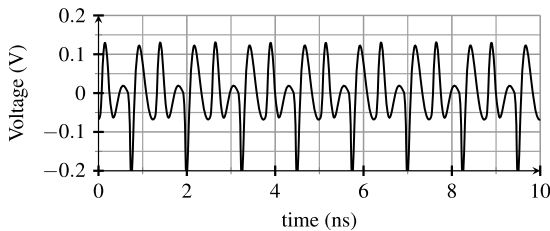

Fig. 10. Output voltage of the edge-combining amplifier at the antenna port

values derived in Sect. 3 are replaced by extracted simulation models incorporating the parasitic resistance values in the capacitors and the quality-factor of the inductors ranging from 5 to 10. In order to correct the matching of the output network, the inductor L_{RFC} and the capacitor C_{DC} are adjusted to 2.51 nH and 1.7 pF, respectively. The resulting input impedance of the output matching network Z_D in comparison to the calculated network is shown in Fig. 8. It can be seen that the imaginary pole at the fundamental frequency ($f_{IF} = 800$ MHz) turns to some extent into a resistance (real valued) which causes leakage of the fundamental frequency to the desired output found at the third harmonic.

As described in Sect. 3, either the drain voltage V_D or drain current I_D need to be zero in order to (at least approximately) have no power dissipation in the transistors of the edge-combiner. Figure 9 pictures the simulated drain current and voltage alternating inversely as desired. However, a small offset remains due to the finite on- and off-resistance of the transistors, especially when they come
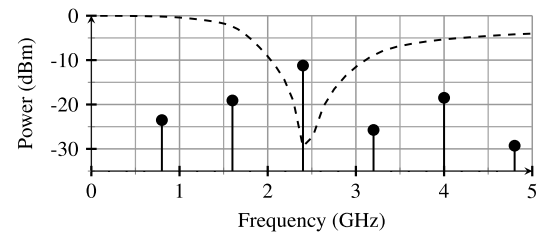

Fig. 11. Simulated harmonic power (●) and S22-parameter (- - -) at the amplifier output

out of strong inversion. The switching points of the edge-combiner are marked in Fig. 9 using vertical lines. They are located at the drain voltage minimums which offer near-to-zero voltage switching to further reduce losses (see Sect. 3.1). This additionally shows that the drain impedance values are matched properly as described in Sect. 3. The resulting output voltage of the amplifier (at the antenna port) is given in Fig. 10.

The output power of the harmonics is derived using a harmonic-balance simulation. The result is plotted together with the output matching S22 in Fig. 11. The power of the fundamental frequency $f_{IF} = 800$ MHz is suppressed to $P_1 = -22$ dBm, which lies 11 dB below the power $P_{out} = -11.8$ dBm of the desired third harmonic at $f_{RF} = 2.4$ GHz. The spectral behavior shows a high nonlinearity. However, the transmitter is used in low output-power applications for short-range communication, together with duty cycling. Hence, the nonlinearities will barely disturb other devices. Moreover, the linearity can be further improved by using a narrow-band antenna or external filter.

The power demand of the amplifier is $P_{PA} = 2.39$ mW, which results in a drain efficiency of $\eta = P_{out}/P_{PA} = 3.2$ % due to the high losses in the passive elements of the fully integrated circuit. The amplifier efficiency seems very low at the first look, but the overall transmitter power consumption is lower compared to traditional architectures where all components are utilized at radio frequency. This is discussed in the following paragraphs by comparing the power demand of transmitters using different frequency multiplication methods—ring oscillator running directly at 2.4 GHz (RO at RF), applying edge-combining (only EC), applying third harmonic extraction (only H3), and combining edge-combining with third harmonic extraction (EC and H3), respectively. The values taken for the following discussion are gained from a fully implemented and simulated edge-combining transmitter.

The total power P_{TX} of the transmitter is composed by constant power demand P_{const}, a frequency-dependent power demand P_{freq} (switched components like ring oscillator and parts of the PLL) and the power demand of the power amplifier P_{PA} having an efficiency of η

$$P_{TX} = P_{const} + P_{freq} + P_{PA} = P_{const} + k \cdot P_{RO, f_0} + \frac{P_{out}}{\eta}. \quad (7)$$

The constant power contribution stays the same for all multiplication methods and is in this case $P_{const} = 1$ mW. The frequency-dependent power increases linearly with frequency. The lowest considered oscillator frequency $f_{RO,1} = 200$ MHz is achieved using edge-combining together with third-harmonic extraction. At this frequency the frequency-dependent power demand is modelled to be $P_{RO,1} = 1.3$ mW. If just edge-combining ($\kappa = 3$) or third harmonic extraction ($\kappa = 4$) is used the frequency of the oscillator needs to be increased by the factor κ to get a radio frequency of $f_{RF} = 2.4$ GHz. By mainly having switched components also the

Table 2. Power-consumption model parameters used with (7) for evaluation in Fig. 12

	RO at RF	only EC	only H3	EC and H3
κ	12	3	4	1
$f_{\text{RO},\kappa}$ (GHz)	2.4	0.8	0.6	0.2
η (%)	40	40	3.2	3.2
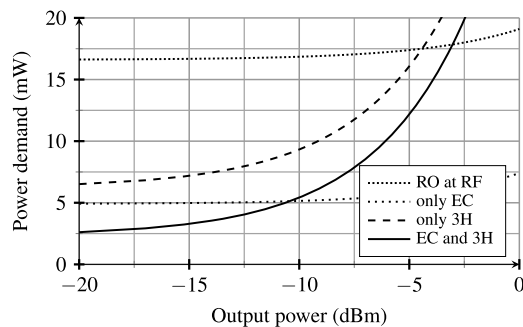
Fig. 12. Power dissipation of different frequency-multiplication methods

frequency-dependent power demand scales by κ and is calculated by $P_{\text{freq}} = \kappa \cdot P_{\text{RO},1}$.

Switched-mode power amplifiers without third-harmonic extraction have higher efficiencies η between 30–40 % [3, 6] compared to using third-harmonic extraction. The efficiency for running the ring oscillator at radio frequency and just using the edge-combiner for frequency multiplication is here considered as 40 %.

The power demand P_{TX} of the transmitters, depending on the output power P_{out}, is calculated with (7) and pictured in Fig. 12. The values for $f_{\text{RO},\kappa}$, κ and η are summarized in Table 2. It can be seen that at an output power below -10 dBm the edge-combiner combined with third harmonic extraction has the lowest power consumption, even with the poor amplifier efficiency of $\eta = 3.2$ %. With increasing output power, the efficiency of the PA becomes more important and using only the edge-combiner has the lowest power demand in this case.

5. Conclusion

This paper describes a design of ultra-low-power transmitters that are able to reduce the overall power consumption by using frequency-multiplication techniques. The edge-combining principle in conjunction with third-harmonic extraction is discussed and the utilization of frequency-multiplication techniques is demonstrated by a harmonic edge-combining amplifier that generates an radio-frequency signal of 2.4 GHz from a ring oscillator running at merely 200 MHz. The transmitter's capability to reduce the overall power consumption—by keeping the operation frequency of the transmitter components low, even when the efficiency of the amplifier suffers—is demonstrated. The concept of the third-harmonic extraction edge-combining amplifier was demonstrated by simulations for a 180 nm 1P6M CMOS process. The proposed transmitter uses on-chip matching and can be fully integrated as it does not require any external components. Especially at low RF output powers, which are typical for short-range medical and body-area network applications, the proposed edge-combining techniques improves the efficiency and overall power consumption of the transmitter.

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