J Electron Test (2010) 26:495
DOI 10.1007/s10836-010-5174-7

Editorial

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Published online: 5 October 2010

We begin with an article on a topic that we don't get to see much. That is because it is a new area and any large-scale implementation, manufacturing or testing is still several years away. In this paper, Biamonte, Allen and Perkowski from Portland State University, Portland, Oregon, USA, discuss a number of fault models for quantum computing devices. It will be interesting to watch which among these models gain widespread application. I hope this paper will serve as foundation for the future research.

The rest of this issue contains articles on test compression, analog fault diagnosis, fault tolerance, security and on-line test.

The second paper is authored by Al-Yamani of KFUPM, Dhahran, Saudi Arabia and McCluskey of Stanford University, Stanford, California, USA. They solve the problem of finding seeds for a pseudorandom pattern generator to reduce the test time.

The third paper provides a test point selection method for analog circuit diagnosis. A compact set of test points is selected and the paper shows that a new Boolean encoding of the fault dictionary is beneficial. The authors of this paper are Yang, Tian and Long from University of Electronic Science and Technology of China, Chengdu, China and Chen of Chengdu College of Sichuan Normal University, Chengdu, China.

In the fourth paper, Sedaghat and Miremadi of Sherif University of Technology, Tehran, Iran, examine the fault behavior of the FlexRay protocol that is used in safety-critical communication systems. This work first appeared at the *Fourteenth IEEE European Test Symposium* (ETS'09), Seville, Spain, in May 2009. Following that we have a paper by Park, Yoo, T. Kim and J. Kim from Sogang University, Seoul, South Korea. They propose an authentication procedure that will prevent illegal use of the JTAG port in a system. The next paper is authored by Wang, Karpovsky and Kulikowski of Boston University, Boston, Massachusetts. Their novel design of memories uses nonlinear single error correcting and double error detecting codes. These codes show significant improvement in reliability over the conventional linear Hamming codes.

The final paper is authored by Kochte, Zoellin and Wunderlich of University of Stuttgart, Stuttgart, Germany. They effectively demonstrate their work on concurrent on-line self-test using partially specified tests through an application to a superscalar RISC processor. The authors first presented this work at the *Fourteenth IEEE European Test Symposium* (ETS'09).

With this issue, we welcome Partha Pande of Washington State University as the editor for the Test Technology Newsletter. He replaces Mohammad Tehranipoor who having completed his term as the Newsletter Editor returns to his normal duties as a JETTA Editor. I would like to express my thanks to Cecilia Metra for the editing of two ETS'09 papers appearing in this issue.

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