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A 65nm CMOS ramp generator design and its application towards a BIST implementation of the reduced-code static linearity test technique for pipeline ADCs

Guillaume Renaud · Manuel J. Barragan · Asma Laraba · Haralampos Stratigopoulos · Salvador Mir · Hervé Le-Gall · Hervé Naudet

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Abstract This work presents an efficient on-chip ramp generator targeting to facilitate the deployment of Built-In Self-Test (BIST) techniques for ADC static linearity characterization. The proposed ramp generator is based on a fully-differential switched-capacitor integrator that is conveniently modified to produce a very small integration gain, such that the ramp step size is a small fraction of the LSB of the target ADC. The proposed ramp generator is employed in a servo-loop configuration to implement a BIST version of the reduced-code linearity test technique for pipeline ADCs, which drastically reduces the volume of test data and, thereby, the test time, as compared to the standard test based on a histogram. The demonstration of the pipeline ADC BIST is carried out based on a mixture of transistor-level and behavioral-level simulations that employ actual production test data.

Keywords Analog-to-Digital Converters · On-chip ramp generator · Built-In Self-Test · Static linearity testing · Reduced-code linearity testing

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1 Introduction

The advance of integration capabilities in current CMOS technologies makes possible the integration of highly complex mixed-signal systems. At the same time standard test procedures for the embedded mixed-signal devices are becoming a major bottleneck in the production line.

Nowadays, Automatic Test Equipment (ATE) suppliers are proposing a modular tester approach. The tester is equipped with different type of options depending on the Device Under Test (DUT) requirements: digital options, analog options, RF options, power options, etc. The nature of the DUT building blocks (i. e. digital, analog, RF, power, etc.) will then define the tester configuration (tester options) and obviously the tester cost. From an industrial point of view, test cost can be simplified and split into two main components. To a first order, the Capital Expenditure (CapEx) is defined as the cost of ATE hardware, and the Operational Expenditure (OpEx) is defined as the labor cost ensuring the ATE is up and running. Other expenses (recurrent or not) add to the total cost, as test boards, test sockets, or maintenance, and can be considered as second order costs. For high volume production, the main cost differentiator in this scheme is the CapEx component, and the presence of analog and mixed-signal components in the DUT has a direct impact in this cost component, as the cost of an analog tester channel is about ten times the cost of a digital tester channel.

For the particular case of standard static linearity tests for ADCs, there are stringent requirements regarding the linearity of the analog stimulus that must be provided by the ATE. Moreover, a large amount of samples have to be collected and analyzed due to the

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noise sensitivity of the measurements, which increases test time.

BIST approaches represent a promising solution to relax ATE requirements and reduce test time. BIST consists of integrating the analog test equipment inside the ADC under test (ADCUT). For example, the standard test of a 12-bit ADC should require one analog channel for the ADC input, twelve digital channels for the ADC outputs, and one additional channel for the ADC clock input. In a BIST configuration, it can be computed that 43% of the CapEx cost is skipped because the analog stimulus generator is integrated together with the ADCUT and, thereby, the analog channel in the tester is no longer needed. Another benefit of integrating the test stimulus generator within the ADC is the noise sensitivity. In the standard approach, generating the test stimulus in the ATE, routing it inside the chip, and then routing the test response back to ATE may provide ten times more noise to the measured performance of the ADC, which can be problematic for measurements that require high-resolution. In contrast, in the case of BIST, all test operations take place inside the chip, thus reducing the noise level in the measurements. In short, the development of BIST for high-resolution ADCs is a promising solution for simplifying the test and reducing costs. Test stimulus generation, signal manipulations, and test response analysis remain internal to the system, the problem of accessing a deeply embedded ADC is eliminated, and the requirements on the ATE, hence its cost, are greatly reduced.

On the other hand, BIST approaches are not free of shortcomings either. Embedded test instruments have to be co-designed together with the ADCUT, which incurs area and power consumption overheads and longer design time. The trade-off between benefits and disadvantages of BIST strategies has to be carefully considered for a successful application. Typically, industry standard practice accepts an area overhead up to 10% for analog and mixed-signal BIST. Power overhead is rarely an issue, since BIST circuitry is powered off during normal operation, and design effort can be reduced by devising reusable embedded test instruments that can be migrated across different technological nodes and reused in different devices under test.

In [20], an efficient on-chip ramp generator suitable for mixed-signal BIST applications is presented. In this paper we extend the work in [20]. In particular, we demonstrate the use of the ramp generator towards a BIST implementation of a reduce-code linearity test technique for pipeline ADCs [13]. Furthermore, the proposed BIST is validated using actual test data from an 11-bit 2.5 bits/stage pipeline ADC provided by STMicroelectronics.

This paper is organized as follows. Section II presents a review of previous works on this topic. Section III presents our proposal for an efficient on-chip ramp stimulus generator. Section IV discusses the practical on-chip implementation of a reduced-code linearity test technique for pipeline ADCs using the proposed ramp generator in a servo-loop configuration. Section V presents experimental results that prove the effectiveness of the proposed ramp generator and the feasibility of the on-chip implementation of the reduced-code linearity test technique for pipeline ADCs. Finally, Section VI summarizes the main contributions of this work.

2 Previous work

The on-chip generation of highly pure ramp stimuli for ADC static linearity test applications remains an open research topic and several works in this line have been presented in the recent years.

In [9], a linear ramp is generated from a closed-loop ramp generator with an eight-phase clock. It is composed of an integrator that senses the amplitude of the output ramp and generates a voltage that is proportional to its slope. This signal is then fed to a voltage-to-current converter and the transconductance of the converter is used to control the current at the input of the ramp integrator. The frequency of operation can be set between 100 Hz and 100 kHz for a ramp between -2 V and 2 V on a 1 μs to 1 s time range. However, the generator is not compensated for the operational amplifier offset and the amplitude feedback only guarantees the correctness of the starting and ending voltages and not the linearity of the ramp during the sweep.

In [7], a BIST scheme to test an ADC and a DAC on the same chip is proposed. The histogram is derived on an 8-bit ADCUT by using a 1-bit DAC converting a stored 1-bit $\Sigma\Delta$ stream into a sawtooth ramp. The maximum simulated INL estimation error is about 0.049 LSB for a test of 12781 clock cycles. However, extensive resources are needed to filter the shaped quantization noise in the $\Sigma\Delta$ sequence.

In [23], two different architectures for the implementation of on-chip ramp generators are presented. The first circuit is a slow-slope current source-C ramp generator which charges a large capacitor with a small current generated by a cascode current source. A voltage buffer is added to the output in order to prevent current leakage. The second circuit is a relaxation triangle-wave generator. It consists of a circuit controlling two switches to charge or discharge a capacitor. It is also intended to work at a higher frequency to explore the dynamic behavior of the ADC. Simulation results on an ideal 10-bit ADC show a maximum DNL estimation

error of 0.03 LSB for the first generator and a 0.15 LSB estimation error for the second generator.

In [3], a continuous-time ramp generator is designed by charging a capacitor with a constant current source. The ramp slope is very sensitive to process variations and a calibration scheme is presented to counter this issue. In [19], the authors also employ the charging capacitor concept with an adaptive scheme to calibrate the output ramp. Three circuits with increasing complexity are proposed.

The works in [10,11,8] present a different solution to the problem aiming at relaxing the linearity requirements of the generated test stimulus. In particular, the approach in [10] proposes to use a low resolution DAC with redundant and poorly matched elements together with a Deterministic Dynamic Element Matching (DDEM) strategy, in order to estimate the static characteristics of a high resolution ADC. This work demonstrates that a 8-bit DAC with DDEM can be used to test a 12-bit ADC. In [11,8], advanced post-processing techniques are proposed to identify and remove the non-linearity of the input stimulus from the output of the ADC. Both techniques rely on the sequential application of two non-linear stimuli that only differ by a constant DC offset.

Other works presented in the literature are focused on reducing the static test time for ADCs [6,12–16,18]. These strategies take advantage of the repetition of design structures in certain ADC architectures, such as pipeline and Successive Register Approximation (SAR) ADCs, to drastically reduce the number of samples that are needed for static linearity characterization. In [16], the authors propose a reduced-code selection technique for the 1.5-bit/stage architecture. However, only comparator offset errors are considered when analyzing the distribution behavior of the transition edges, thus this technique has limitations and can fail in practice. The technique in [16] is improved in [12–15] where the developed solution does not make any assumption on the error sources affecting the static linearity characteristic of the ADC and is also immune to noise in the ADC. Reduced-code linearity testing techniques provide a great reduction on test time and data volume transfer to the tester, which make them very suitable for high volume production test. On the other hand, these techniques so far were not intended for BIST since they still need a controlled and precise analog test stimulus that has to be provided by the tester. In this work, we detail the design of an efficient on-chip ramp generator and discuss its application towards a full BIST for pipeline ADCs based on the reduced-code test strategy described in [13].

3 On-chip discrete-time integrator-based ramp generator

3.1 Proposed ramp generation technique

The proposed ramp generation technique, originally described in [21] and further developed in [20], is based on a two-input switched-capacitor (SC) integrator with a small capacitance difference in its input sampling capacitors, C_{i1} and C_{i2}. Fig. 1 shows the schematic of the proposed ramp generator. The core of the proposed ramp generator is a fully-differential parasitic-insensitive SC integrator that operates with two non-overlapping clock phases, ϕ_1 and ϕ_2. Digital control signals ϕ_{up} and ϕ_{down} set the sign of the ramp slope for each integration step, signal ϕ_{reset} performs a reset of the integrating capacitor, and signal ϕ_0 is added to charge the output of the integrator to a reference voltage V_a for measurement calibration purposes. The interested reader is referred to [21] for a detailed description of the measurement calibration procedure.

The output of the integrator, under ideal conditions, is given by

$$V_{out}(n) = V_{out}(n-1) + \frac{C_{i2} - C_{i1}}{C_F} V_{ref} \quad (1)$$

at time $t = nT_{clk}$, where T_{clk} is the integrator clock period, V_{ref} is an input DC reference voltage, and C_F is the integrator's feedback capacitor. As it can be derived from (1), the integrator output is a stepwise ramp, and the magnitude of the steps depends on the capacitance difference between C_{i1} and C_{i2}. This capacitance difference is implemented at layout level by eliminating one metal finger from one of the capacitor plates to deliberately create a mismatch between the input capacitors. Clearly, this implementation choice, despite being simple, is prone to variations of the ramp step size due to random mismatch in the capacitors. Moreover, other non-idealities, such as noise, offset, integrator finite gain and leakage, switches charge injection and clock feedthrough, etc., have also an impact in the performance, i. e. resolution and linearity, of the ramp generator. In the next subsection, we analyze the effect of the main non-idealities in the ramp generator and we provide guidelines to reduce their impact in the generator performance.

3.2 Design considerations for a practical on-chip implementation

3.2.1 Operational amplifier design

The operational amplifier is a standard fully-differential two-stage folded-cascode topology with Miller com-

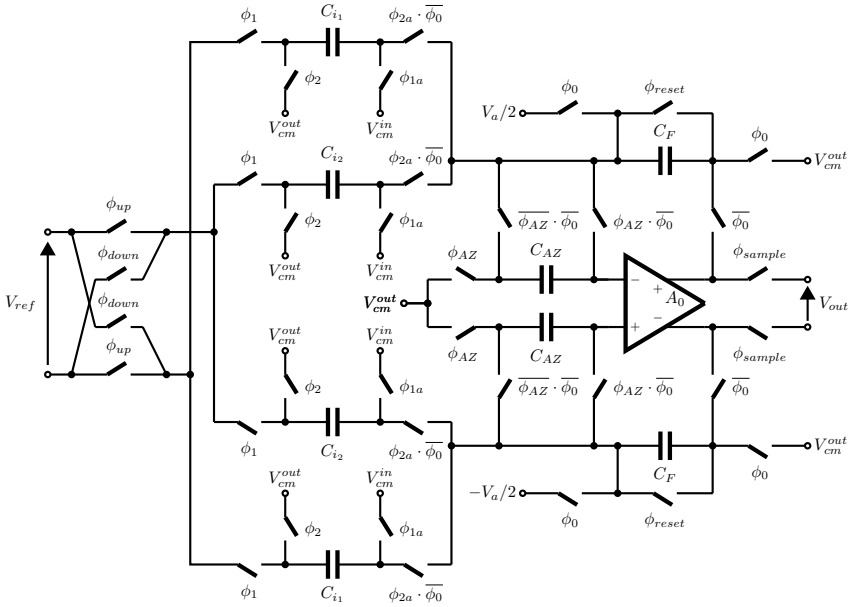


Fig. 1: Fully differential switched-capacitor ramp generator

pensation. Fig. 2a shows the topology of the amplifier (the bias voltage circuitry is not shown for simplicity). The outputs of the two stages are connected to a dynamic switched-capacitor common-mode feedback (SCCMFB) network [4], as shown in Fig. 2b, that defines the common-mode voltage for the differential output nodes. A differential configuration enables a high common-mode rejection ratio, improved immunity to charge injection and clock-feedthrough from the switches, and suppression of even harmonics, thus enhancing the linearity of the amplifier. Moreover, this topology with class-AB second stage yields a higher gain and larger output swing compared to the folded-cascode stage. Using a simple pole-zero analysis, the two-stage amplifier transfer function is modeled as

$$H_{OA}(\omega) = \frac{A_0(1 + j\omega/z_1)}{(1 + j\omega/p_1)(1 + j\omega/p_2)}, \tag{2}$$

where, assuming $1/p_1 >> 1/p_2$,

$$A_0 = \frac{g_{m1}g_{m3}g_{m4}g_{m7}}{(g_{m4}g_{ds3}(g_{ds1} + g_{ds2}) + g_{m3}g_{ds4}g_{ds5})(g_{ds7} + g_{ds8})}, \tag{3}$$

$$p_1 \approx \frac{g_{m1}}{A_0 C_C}, \tag{4}$$

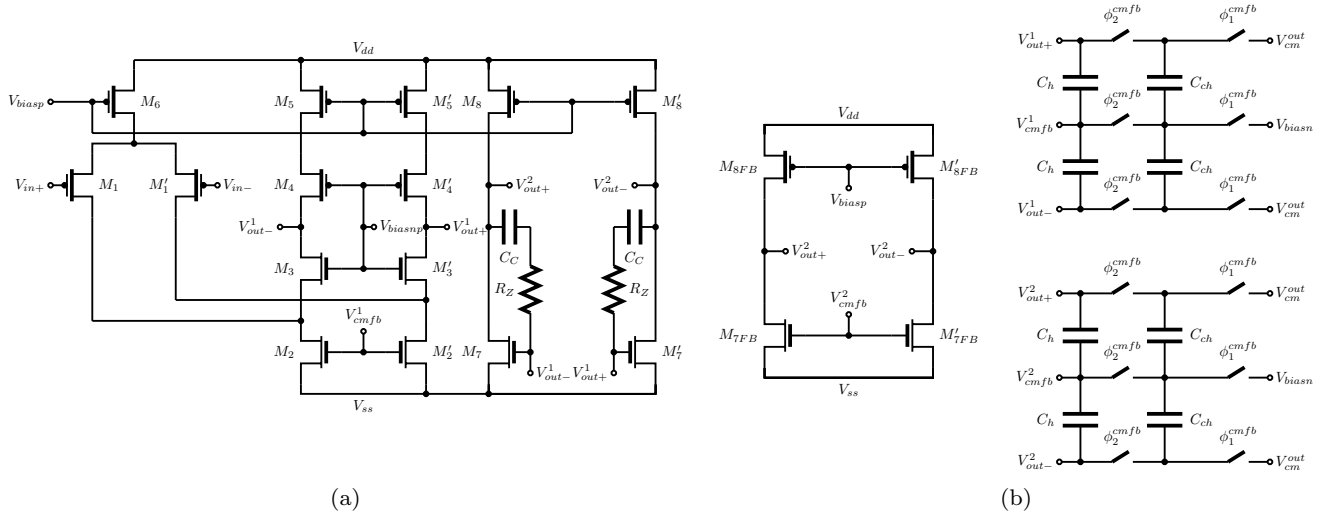
$$p_2 \approx \frac{g_{m7}}{C_L}, \tag{5}$$

$$z_1 = \frac{g_{m7}}{C_C(g_{m7}R_Z - 1)}, \tag{6}$$

$$GBW = A_0 p_1 \approx \frac{g_{m1}}{C_C}. \tag{7}$$

The resistance R_z is taken equal to the inverse of g_{m7} to suppress the zero pole. Alternatively, its value can be increased to enlarge the phase margin of the amplifier. The gain can be maximized by increasing the transconductance and reducing the output conductance of transistors $M_1 - M_1'$, $M_3 - M_3'$, $M_4 - M_4'$, $M_7 - M_7'$. Transconductance of transistors $M_7 - M_7'$ must be high enough to push the second pole to frequencies above the gain-bandwidth frequency.

The common-mode voltage for each stage is provided by dynamic SCCMFB networks. As shown in Fig. 2b, the two SCCMFB networks are controlled by non-overlapping clock phases ϕ_1^{cmfb} and ϕ_2^{cmfb}. The first SCCMFB samples the output voltage of the folded-cascode stage. When ϕ_1^{cmfb} is active, each charge capacitor C_{ch} is charged to the differential voltage between the reference common-mode voltage V_{cm}^{out} and the bias voltage V_{biasn} of transistors $M_2 - M_2'$. Then during the ϕ_2^{cmfb} phase, the charge kept in the charge capacitors are transferred to the hold capacitors C_h whose voltage is updated and compensates the common-mode voltage difference between the output nodes until the next clock cycle. If the output common-mode is below its ideal value, the $M_2 - M_2'$ bias voltage is raised to counter the deviation, and vice versa. Similarly, the second SCCMFB samples the output voltages of the second stage [24]. The output common-mode voltage is then used to control two common source amplifiers, M_{7FB} and M_{7FB}', that drive the output nodes by pumping or pushing current into the output branches. As it is described in [4], the common mode voltage settling time



(a) (b)

Fig. 2: (a) Fully differential two-stage folded-cascode operational amplifier; (b) First-stage and second-stage SC-CMFBs networks.

depends mainly on the ratio between the charge capacitor C_{ch} and the hold capacitor C_h. Their values are chosen to limit KT/C noise in the common-mode feedback branches and at the same time be reasonably small to reduce area overhead.

3.2.2 Finite gain and integrator leakage

A direct consequence of the finite amplifier gain is the integrator leakage. In each integration cycle, only a fraction α of the previous integrator output voltage is added to the input sample. The integrator leakage limits the gain of the integrator, as well as the ramp linearity. The Z-transform transfer function of the SC integrator with leakage can be expressed as

$$H_{INT}(z) = g\frac{z^{-1}}{1-\alpha z^{-1}} \tag{8}$$

with

$$g \approx \frac{C_{i_2}-C_{i_1}}{C_F}\left(1-\frac{1+\frac{C_{i_2}-C_{i_1}}{C_F}}{A_0}\right),$$

$$\alpha \approx 1-\frac{C_{i_2}-C_{i_1}}{A_0 C_F}.$$

These effects can be minimized by choosing a high gain A_0 as well as a small input capacitance difference $C_{i2}-C_{i1}$.

3.2.3 Gain bandwidth and slew rate

The proposed on-chip ramp generator is intended for ADC static linearity test applications. In order to characterize the linearity of an ADC, we must ensure that the ADC works under quasi-stationary conditions. This means that the ramp generator has to operate at a clock frequency that is significantly lower than the sampling rate of the ADC, such that practically the ADC samples a DC voltage. In other words, each output ramp step must settle completely on the integrating phase ϕ_2, such that the ADC digitizes a quasi-constant value when on its active phase. However, the clock frequency of the ramp generator should not be so slow to the point where the feedback capacitor starts discharging during the conversion significantly affecting the operation of the integrator. Given the above discussion, the GBW requirement can be relaxed while the slew rate (SR) requirement becomes more stringent. The SR can be expressed as

$$SR = \frac{I_{m6}}{C_C}, \tag{9}$$

where I_{m6} is the current flowing through transistor M_6. From equation (9), we can select I_{m6} and C_c to achieve a sufficiently high SR, keeping in mind that I_{m6} should be sufficiently small so as to avoid prohibitive power consumption (in any case, power consumption is not an important issue here since the ramp generator is powered on only in test mode), and C_c should have a value that guarantees the stability of the amplifier while incurring the smallest area possible. Thereafter, from (7), g_{m1} is selected to be sufficiently high enough to achieve the required GBW.

3.2.4 Noise

Due to the switch-capacitor implementation of the input branches, all noise sources are uncorrelated during phase ϕ_1 but correlated during phase ϕ_2 because C_{i_1} and C_{i_2} are sampling the amplifier noise simultaneously. In the presence of noise, the Z-transform transfer function of a single-ended integrator can be expressed as

$$V_{out}(z) = \frac{C_{i_2} - C_{i_1}}{C_F} \frac{z^{-1}}{1 - z^{-1}} V_{ref} + N_{out}(z), \tag{10}$$

with

$$N_{out}(z) = \frac{C_{i_1}}{C_F} \frac{z^{-1} N_{i_1}^{\phi_1}(z) - N_{i_1}^{\phi_2}(z)}{1 - z^{-1}} + \frac{C_{i_2}}{C_F} \frac{z^{-1} N_{i_2}^{\phi_1}(z) - N_{i_2}^{\phi_2}(z)}{1 - z^{-1}},$$

where $N_{i_1}^{\phi_k}$ and $N_{i_2}^{\phi_k}$, $k \in \{1, 2\}$, are the noise voltages sampled by the input capacitors C_{i_1} and C_{i_2} during phases ϕ_1 and ϕ_2.

The equivalent input voltage of the integrator in the differential case, integrated from 0 to $T_{clk}/2$, can be expressed as [17][22]

$$V_{in}^{noise} = \sqrt{K_b T \left(\frac{\theta_{C_{i_1}}}{C_{i_1}} + \frac{\theta_{C_{i_2}}}{C_{i_2}} \right)}, \tag{11}$$

with

$$\theta_{C_{i_1}} = 2(1 + \beta GBW(2R_{on} \frac{C_{i_2}^2}{C_{i_1}} + \frac{R_{OA}}{2}(C_{i_2} + \frac{C_{i_2}^2}{C_{i_1}}))),$$
$$\theta_{C_{i_2}} = 2(1 + \beta GBW(2R_{on} \frac{C_{i_1}^2}{C_{i_2}} + \frac{R_{OA}}{2}(C_{i_1} + \frac{C_{i_1}^2}{C_{i_1}}))),$$

where K_b is the Boltzmann constant, T the absolute temperature, T_{clk} the period of clock phases ϕ_1 and ϕ_2, R_{on} the resistance value of the switches when closed, $\beta = C_F/(C_F + C_{i_1} + C_{i_2})$ is the feedback factor of the integrator, and R_{OA} is the equivalent input-referred noise resistance of the amplifier

$$R_{OA} = \frac{2}{3g_{m1}}(1 + \frac{g_{m2}}{g_{m1}} + \frac{g_{m5}}{g_{m1}} + \frac{g_{m7}}{g_{m1} A_0^2}), \tag{12}$$

with

$$V_{OA}^{noise} = \sqrt{V_{n_1}^2 + (\frac{g_{m2}}{g_{m1}})^2 V_{n_2}^2} + \sqrt{(\frac{g_{m5}}{g_{m1}})^2 V_{n_5}^2 + (\frac{g_{m7}}{g_{m1} A_{0_1}})^2 V_{n_7}^2} = \sqrt{4 K_b T R_{OA}}, \tag{13}$$

$$V_{n_p}^2 = \frac{8 K_b T}{3 g_{m_p}}. \tag{14}$$

To minimize the amplifier input noise, the dimensions of the switches should be set appropriately high to reduce R_{on}, g_{m1} should be set sufficiently high to reduce R_{OA} (the last term in the expression of R_{OA} can be neglected since A_0 is very large), and C_{i_1} and C_{i_2} should be selected sufficiently high to limit KT/C noise, keeping in mind that the largest their values are the more difficult will be to achieve a small mismatch that results in a sufficiently small ramp step size.

3.2.5 Amplifier offset

Due to mismatch in transistors, a non-negligible offset voltage can appear at the amplifier input. This offset is integrated at each integration phase together with the input signal unless correction is applied. The integrator output can be expressed during phase ϕ_2 as

$$V_{out}(n) = V_{out}(n-1) + \frac{C_{i_2} - C_{i_1}}{C_F} V_{ref} + (1 + \frac{C_{i_1} + C_{i_2}}{C_F}) V_{os}. \tag{15}$$

The offset can significantly affect the ramp's step size, given that C_{i_1} and C_{i_2} are approximately equal. We can distinguish a deterministic and a random component in the amplifier offset. The former can be greatly reduced by careful design and dedicated layout techniques. The latter is due to mismatch in transistors of the differential branches. Various techniques have been proposed for the cancellation of the random offset component in SC circuits [5]. The proposed ramp generator design employs a simple closed-loop auto-zero technique to compensate the effect of the integrator offset. The employed auto-zero technique has a closed-loop implementation because the open-loop one would destroy the amplifier gain. As detailed in [5], it is a classical offset compensation technique that relies on the use of a capacitor to store the offset and subtract it from the output. As shown in Fig. 1, capacitor C_{AZ} is used to store the amplifier offset during the sampling phase and to subtract this offset in the integration phase. The interested reader is referred to [5] for an analytical description of the technique. It can be demonstrated that the residual offset at the integrator output is proportional to the ratio of the uncompensated charge injection produced by the integration switches and the amplifier gain. The fully differential architecture and a high amplifier gain contribute to reduce the effect of this residual uncompensated offset.

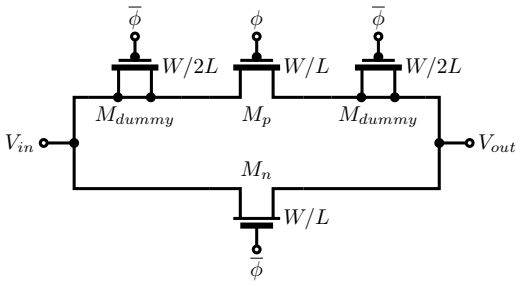


Fig. 3: Implementation of CMOS switches

3.2.6 Charge injection and clock feedthrough

Each switch is designed as a CMOS switch, consisting of a PMOS and a NMOS with shorted source and drain nodes. The CMOS implementation is useful to reduce the R_{on} equivalent resistance of the switch. Charge injection is caused by stray capacitance associated with the NMOS and PMOS transistors. The gate-drain capacitance associated with the PMOS device is about twice that of the NMOS device, because for both devices to have the same on-resistance, the PMOS device has to be about twice as large as the NMOS device. Charge injection occurs at the end of phase ϕ_1 when input voltage sampling is over and the input switches are turned off. The charge exiting the drain gets injected in the input capacitors, adding an offset to the sampled voltage. If the PMOS and NMOS switches had the same dimensions, the liberated charges would cancel each other due to their opposite signs. However, this is not true due to mismatch in transistors and because charge injection is signal dependent. Nevertheless, charge injection can be limited by using several design techniques as discussed in [5].

The proposed ramp generator design employs two techniques to reduce the charge injection in the switches. The first technique is to connect dummy transistors on both sides of the CMOS switch to reduce the stray capacitor mismatch, as shown in Fig. 3. They have the same length as the main switches but half their width and their drain and source are connected together. When the main switch turns off, the dummy switches turn on, and acquire the same amount of charge that the main switch has lost. The second technique employs the bottom plate of the sampling capacitor. Using advanced clock phases with respect to the integrator clock, labelled ϕ_{1a} and ϕ_{2a} in Fig. 1, the switch at the bottom plate of the capacitor opens before the switch at the top plate of the capacitor. When the top plate switch opens, the bottom plate is floating and no charge is injected into the capacitor. These two techniques are implemented on each switch and the clocking of the integrator is set accordingly. Additionally, the effects of charge injection are further reduced by the fully differential architecture of the integrator, since charge injection in the positive and negative signal paths tend to compensate.

Clock feedthrough is due to the gate-to-source capacitors, interconnect parasitic capacitors of the switches and substrate coupling. They cause the clock signal to be coupled into the analog signal path and add an offset to the sampled voltage as well. It is reported that in most cases this effect is dominated by clock injection effects. However, similar to the case of charge injection, it can be reduced by increasing the sampling capacitor.

4 Practical on-chip implementation of reduced-code static linearity test for pipeline ADCs

4.1 Underlying principle

The reduced-code linearity testing method for pipeline ADCs achieves significant static test time reduction through the exploitation of an inherent property of the pipeline ADC architecture [12–16]. This inherent property states that if we traverse the input dynamic range of the ADC, we observe that there exist different output transitions between consecutive codes that are due to same comparator being exercised (e.g. its threshold is crossed) in one of the pipeline stages. This is illustrated by the transfer characteristic in Fig. 4, where t_{ik} corresponds to an output transition that is due to the i^{th} comparator in the k^{th} stage being exercised. This inherent property can be exploited for reducing the static test time as explained below.

Any non-ideality in a pipeline stage (i.e. finite op-amp gain, capacitor mismatch, op-amp offset, sub-ADC comparators offset, etc.) will be translated to a DNL error of all ADC output codes that involve an output transition that is due to a comparator being exercised in this pipeline stage. An ADC output code shares two adjacent ADC output transitions that involve two different comparators, possibly belonging to two different pipeline stages, as shown in the example of Fig. 4. The stage that is closer to the front of the pipeline will dominate the DNL error that is finally produced. In the example of Fig. 4, let us assume that the k^{th} stage is closer to the front of the pipeline compared to the b^{th}, d^{th}, f^{th}, and h^{th} stages. This means that the width of codes μ, μ+1, λ, and λ+1 are principally affected by the non-idealities in the k^{th} stage. Furthermore, it means that the widths of the codes λ and $\lambda+1$ are practically equal to the widths of the codes μ and $\mu+1$, respectively. Thus, we need to measure the width of either μ

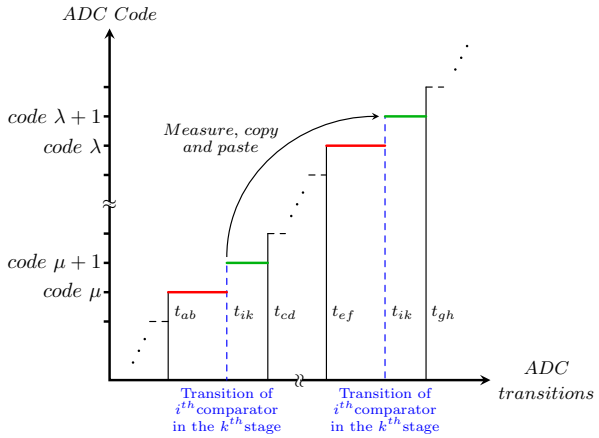


Fig. 4: Reduced-code testing technique principle

or λ and the width of either $\mu+1$ or $\lambda+1$. Extending this argument, let us assume that we know the mapping between the transitions in the ADC output and the comparators in the pipeline stage that are being exercised to produce these transitions. If we measure only the codes around a representative set of ADC output transitions such that this set covers all comparators in all stages and each comparator is represented once in this set, then, by relying on the mapping, we can readily assign values to the widths of unmeasured codes around the unselected ADC output transitions. In other words, we measure a reduced number of codes in the histogram and we fill in the rest of the histogram automatically by relying on the information in the extracted mapping.

With regard to static test time, it is mainly governed by the transfer time of data from the ADC under test to the memory of the ATE and from the ATE to the workstation where the data will be processed for constructing the histogram. The pure electrical test time is rather negligible compared to the data transfer time. The reason is that data produced during static test have a very high volume. Specifically, during static test the excitation of dynamic phenomena should be avoided. This imposes strict limitations to the frequency of the test stimulus, which has to be necessarily slow to ensure static operation. Moreover, static test is very sensitive to noise, which makes it necessary to average the measurements across multiple runs. In a standard histogram test, these requirements translate to using a slow ramp as test stimulus (a typical slope may be around 100 hits/code) and applying this ramp multiple times to average noise (typically around 100 full-scale ramps are applied). As an example, for an 11-bit ADC, these conditions would produce $N = 2048 \times 10^4$ 11-bit values to be read out. Thus, in the case of the reduced-code linearity test technique, if we measure X% of the codes, which compared to the standard histogram technique translates into transferring only X% of the data, then we drastically reduce the static test time. Overall, we expect to have a test time reduction slightly below (100-X)% given that compared with the standard histogram technique we have the extra step of deriving the mapping. The derivation of the mapping needs to be carried on a chip-by-chip basis because the mapping may change due to process variations. From the above discussion, it is clear that deriving an accurate mapping is a crucial step in the method. For this purpose, it has been proposed to monitor directly the outputs of the pipeline stages [14,15] and to cancel out the noise in the transitions of the pipeline stages [12,13]. Two important recommendations include (a) considering measuring more than two codes around the ADC output transitions that involve comparators which belong to the stages that are closer to the front of the pipeline so as to account for large linearity errors and (b) avoiding selecting an ADC output transition for a comparator in a given target stage that involves in addition a comparator in one of the previous stages so as not to overshadow the DNL error produced by the target stage. The interested reader is referred to [12–15] for more details on the method.

4.2 Practical BIST implementation

The proposed ramp generator is key for implementing a BIST version of the reduced-code linearity testing method for pipeline ADCs. The other key component is a digital BIST engine that makes use of the available on-chip DSP and memory resources, but this component is out of the scope of this paper. There are basically two test configurations, as shown in Fig. 5. In the first test configuration (Fig. 5a), the ramp signal is applied to the input of the pipeline ADC. The BIST engine monitors the outputs of the pipeline stages and the ADC output transitions as we traverse the input dynamic range and provides the mapping between the ADC output transitions and the comparators that are being exercised in the pipeline stages, as well as the reduced set of ADC output transitions and the surrounding codes whose widths will be measured directly. In the second test configuration (Fig. 5b), the pipeline ADC is connected in a servo-loop where the ramp signal generator is used to measure the widths of the codes around the selected ADC output transitions. The code widths measurements are transferred to the BIST engine and are combined with the mapping information to reconstruct the histogram and calculate the DNL and INL profiles.

The proposed servo-loop configuration is a modified version of the classical servo-loop [1,2]. As depicted in Fig. 5b, the continuous-time ramp stimulus generator

used in the standard servo-loop is replaced by the proposed discrete-time ramp stimulus generator. The operation is quite similar to the classical servo-loop. The code width is measured by counting the number of ramp steps with a digital counter as we traverse the input range between the two transitions that correspond to the target code. Specifically, starting at the transition at the left of the target code, if the output ADC code is the target code, the ADC input is raised in steps and the counter starts incrementing until the transition at the right of the code is crossed, in which case the output ADC code becomes the code next to the target code. Then, the ADC input is lowered in steps, and the counter continues to increment until the transition at the left of the target code is crossed, in which case the output ADC code becomes the code before the target code. The process is repeated r times oscillating the ADC input around the input range that corresponds to the target code so as to average the combined ramp generator and ADC noises. The number of steps per code for code c_k is expressed as

$$\widehat{m_k} = \frac{\sum_{i=1}^{r} m_i^{cnt}}{2 \cdot r}, \qquad k = 1, 2, ..., 2^N - 1 \tag{16}$$

where m_i^{cnt} the number of steps counted during excursion i. The expression is divided by a factor 2 because the number of steps is summed in both upward and downward excursions. The number of steps per code $\widehat{m_k}$ is then multiplied by the step size to evaluate the width of code c_k. Once the width of the target codes around the selected set of representative ADC transitions have been measured, we can reconstruct the full ADC static transfer characteristic by mapping these measurements to the rest of unmeasured codes in the ADC as explained in[13]. DNL and INL figures can be then easily extracted from the static ADC characteristic using their standard definitions.

5 Results

5.1 Discrete-time integrator-based ramp generator

The proposed ramp generator was designed using STMicroelectronics 65nm CMOS technology. The ADCUT is an 11-bit 2.5 bits/stage pipeline ADC with a 1 V full scale. Given this target application, our design goal is a ramp generator that is able to generate a linear stepwise ramp with a step magnitude of around 100 μV, that is, around 0.2 LSB regarding the target ADC, in the voltage range from 0 to 1 V. Taking into account the design trade-offs discussed in the previous sections,

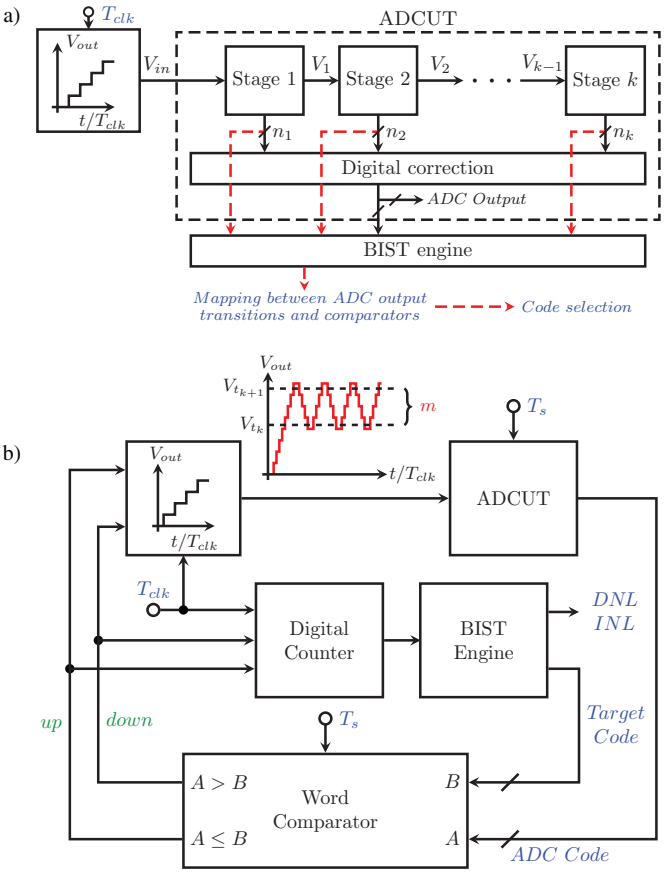


Fig. 5: Practical BIST implementation of the reduced-code linearity testing technique for pipeline ADCs: a) Code selection; b) Discrete-time integrator-based servo-loop.

Table 1 shows the main design parameters for the practical implementation of the ramp generator, such that it complies with the requirements set by the target application, as well as and the achieved performance obtained by electrical transistor-level simulation. The layout of the ramp generator has been designed and its area is 0.1 mm^2, which is below 10% of the area of practical high-performance ADCs at this resolution. This BIST area overhead is deemed acceptable by the industry.

The ramp generator is simulated under typical process conditions, with a 200 kHz clock frequency, and using a 2 V differential DC input as voltage reference. The generated stepwise ramp has a nominal resolution of 13.3 bits, with an average step of 96.7 μV. As a measure of the ramp linearity, Fig. 6 shows the difference between each integration step in the generated ramp and the average step. As it can be seen, the deviation of the step size is very well contained within the range $[-3, 3]$ μV along the considered voltage range. We define the slope error per step as the difference between the slope of the ramp connecting the middle points of

Table 1: Ramp generator parameters

Parameter	Units	Design target	Electrical simulation
A_0	dB	>80	92.5
Phase Margin	°	>60	75
GBW	MHz	>90	95
Common mode input range	V	>2	-2.38/2.39
Common mode output range	V	>2	-2.28/2.28
SR	V/μs	>100	156
$t_{settling}$	ns	<100	60
Nominal clock frequency	kHz	200	–
Minimum clock frequency	kHz	1	–
C_i	pF	1	–
$Ci_1 - Ci_2$	fF	1	–
C_F	pF	10	–

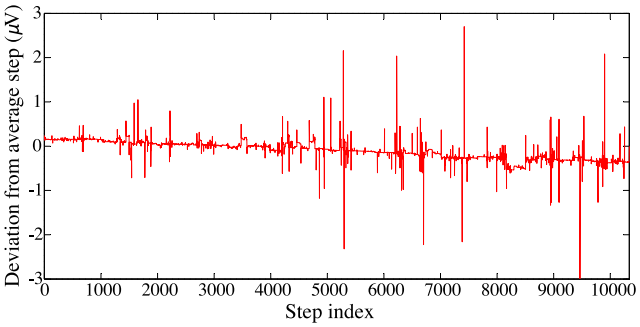


Fig. 6: Deviation of the magnitude of the steps with respect to the average ramp step.

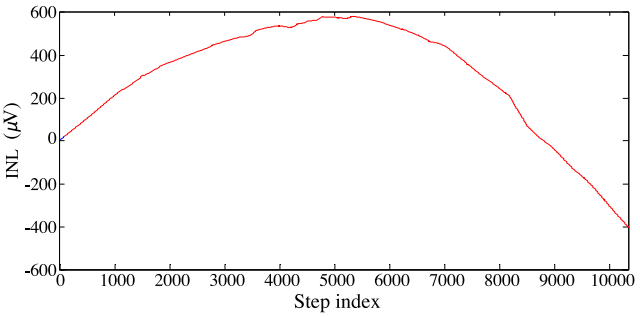


Fig. 7: INL of the generated ramp.

two consecutive steps and the slope of a linear fit to an ideal ramp that crosses through the middle points of the steps. The average slope error, that is, the average of slope errors per step over all steps, is computed to be −0.040%. In the same way, we can compute the INL of the generated ramp from the values in Fig. 6, defined as the difference between the actual position of the middle point of each step and its ideal position. The complete INL characteristic of the generated ramp is shown in Fig. 7. The maximum INL of the generated ramp is around 580 μV, that is, around 6 average steps.

Fig. 6 clearly shows a constant linear decrease of the ramp step size across the considered full-scale that

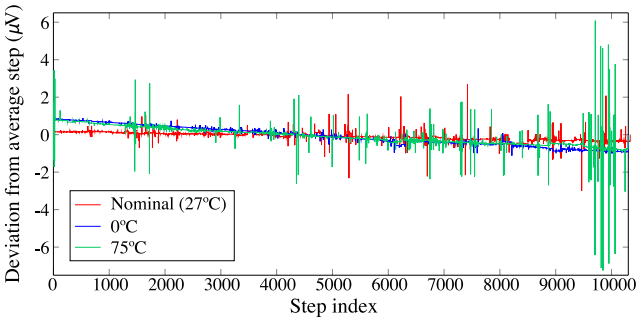


Fig. 8: Deviation of the magnitude of the ramp steps with respect to the average ramp step at different operation temperatures.

can be explained by the effect of the integrator leakage. Consequently, the INL curve in Fig. 7, obtained by integrating the DNL curve, shows a very characteristic parabolic shape. These results indicate that the main source of static non-linearity in the proposed ramp generator design comes from the integrator leakage and, to a lesser extent, from the residual integrator offset.

It is also worth noticing that the proposed measurement strategy takes advantage of the smooth shape of the INL curve and the well-contained evolution of the ramp step size. Since the proposed reduced-code linearity test technique only requires the measurement of the widths of a limited set of codes, the ramp stimulus is only required to be locally linear in the vicinity of the target codes, as long as the ramp step size is relatively constant and only a small fraction of the LSB.

In order to further validate the performance of the proposed ramp generator under different operation conditions, Fig. 8 shows the deviation of the step size of the generated ramp across the complete voltage range of the ramp for corner temperatures $T = 0$°C and $T = 75$°C and for the nominal temperature $T = 27$°C. As it can be observed, the impact of temperature variations in the linearity of the ramp is well controlled. The resulting

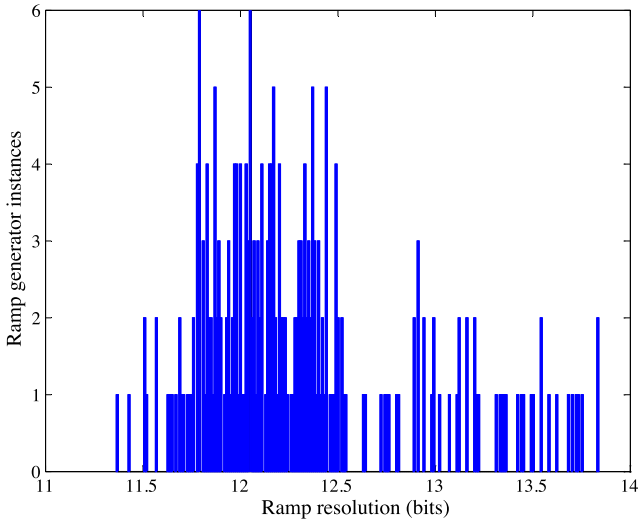


Fig. 9: Histogram of the resolution of the generated ramp obtained by Monte Carlo process and mismatch simulations.

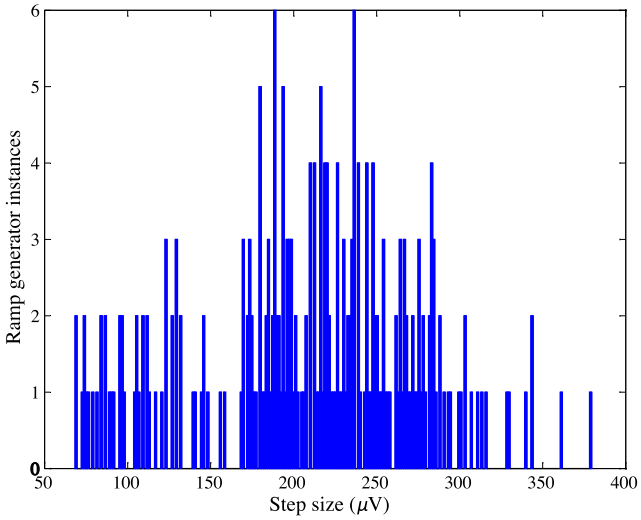


Fig. 10: Histogram of the step size of the generated ramp obtained by Monte Carlo process and mismatch simulations.

average step sizes are 96.9 μV and 97.1 μV for $T = 0$°C and $T = 75$°C, respectively. Compared to the 96.7 μV average step size for $T = 27$°C, the change of the magnitude of the average step size due to stressed temperature operation is below 0.5%.

In order to show the impact of process variations and mismatch on the performance of the proposed ramp generator, we carried out a set of Monte Carlo transistor-level electrical simulations of the complete system using the actual Process Design Kit (PDK) of the technology. To speed up the simulation process, during each Monte Carlo iteration we monitor at fixed time instants the step size of the generated ramp (which is relatively stable as shown in Fig. 8), and the iteration is stopped and skipped if the step size is small and well within the design goal. In this way, we bias the Monte Carlo simulation towards worst cases and we generate such worst cases with less computational effort.

Fig. 9 and Fig. 10 show the histograms of the ramp resolution and average step size, respectively, for 250 Monte Carlo runs. As it can be seen, the obtained resolution and step size are well contained in the range of 11.4-13.7 bits and 100-300 μV, respectively, which comply with the requirements of our target application.

Fig. 11 shows the histogram of the average ramp slope deviation for the 250 Monte Carlo runs. As it can be seen, this deviation is well centered around the -0.2% value and the observed worst case value close to -6% is still deemed very acceptable.

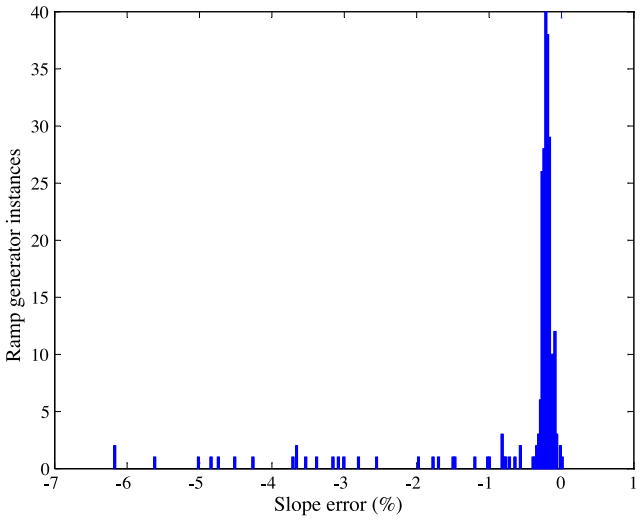


Fig. 11: Histogram of the average slope error of the generated ramp obtained by Monte Carlo process and mismatch simulation

5.2 Reduced-code linearity testing of a pipeline ADC using a discrete-time integrator-based servo-loop

To demonstrate the feasibility and performance of the proposed ramp generator in an actual test application, we employ the ramp generator to implement an on-chip servo-loop-based reduced-code linearity test technique for pipeline ADCs. The ADCUT is an 11-bit 2.5 bits/stage pipeline ADC IP provided by STMicroelectronics.

The complete test setup described in Fig. 5 has been modeled in Matlab. Realistic behavioral models have been developed for the ADC and ramp genera-

tor. The ADC model has been derived from the actual static characteristic of the ADC, which was measured in the lab using the standard histogram technique on dedicated bench-top equipement. On the other hand, the ramp stimuli have been directly captured from the transistor-level electrical simulations of the complete ramp generator. The BIST engine, digital counter, and word comparator blocks are digital circuits and, thereby, for simplicity, have been considered as ideal blocks in this work.

According to the reduced-code algorithm in [13], in order to characterize the complete static characteristic of the ADCUT we only need to measure the code widths around a reduced set of selected transitions. Specifically, we only need to measure the widths of 8 codes around the 6 transitions of the first stage, 6 codes around the 6 transitions of the second stage, 4 codes around the 6 transitions of the third stage, and 2 codes around the 6 transitions for the fourth and fifth stages. The interested reader is referred to [13] for a detailed description of the algorithm for relevant code selection. Only 132 out of 2046 codes of the ADCUT are measured, which represents about 6% of the total number of codes, resulting in a significant test time reduction.

Fig. 12 shows the estimated INL using the proposed BIST scheme. Each code is traversed r=50 times in the servo-loop configuration so as to average out noise effects. Fig. 12 also shows the actual INL values obtained from a traditional histogram test for the purpose of comparison, as well as the INL estimation error. As it can be seen, under nominal conditions the INL estimation error is well controlled in the range $[-0.5\text{LSB}, +0.5\text{LSB}]$.

In order to estimate the robustness of the proposed BIST to process variations and mismatch, we performed Monte Carlo transistor-level electrical simulation of the ramp generator with 250 runs, and we employed the test set up of Fig. 5 250 times, each time using a different ramp generator instance. Fig. 13 shows the histogram of the maximum INL estimation error in absolute values recorded for each run. As it can be seen, the INL estimation error is always below 1 LSB with an average absolute value around 0.5 LSB. Results in [13] show that INL estimation error using an ideal ramp, that is, the INL estimation error that is exclusively due to the reduced-code linearity test technique itself, is in the range $[-0.5\text{LSB}, +0.5\text{LSB}]$. According to our results in Fig. 13, in the worst-case scenario, the non-linearity of the proposed ramp generator design only contributes an additional 0.5 LSB to the INL estimation error introduced by the reduced-code linearity test technique.

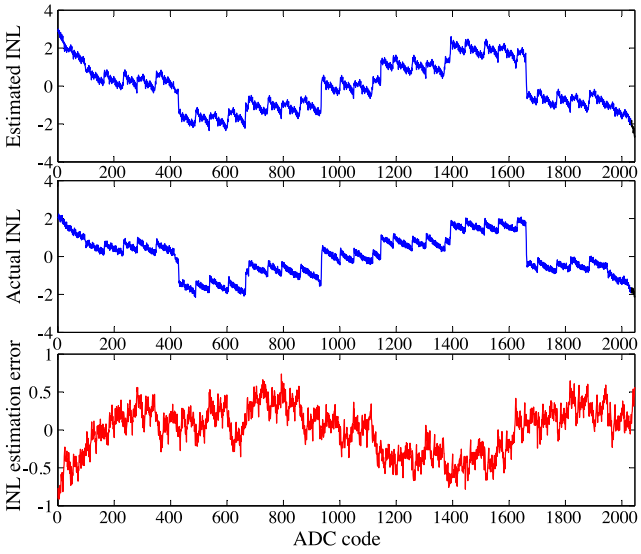


Fig. 12: Estimated INL obtained by BIST, actual INL obtained by standard histogram test, and INL estimation error.

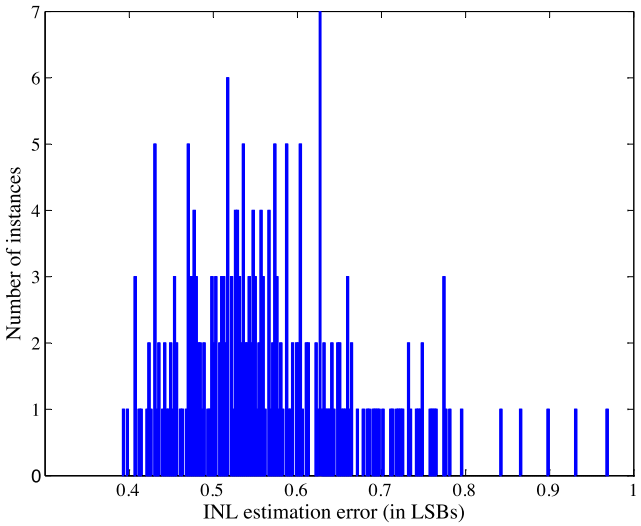


Fig. 13: Histogram of the maximum absolute INL estimation error obtained by the BIST by assuming different Monte Carlo instances of the ramp generator.

6 Conclusions

In this work, we have presented an efficient ramp generator for ADC static BIST applications. The proposed ramp generator is based on a discrete-time SC integrator whose input stage has been modified to produce a very small integration gain. The main non-idealities affecting the performance of the ramp generator have been comprehensively discussed, and design trade-offs to alleviate these effects have been explored. The complete ramp generator has been designed in a 65nm technology and its performance has been validated by

transistor-level electrical simulations. A nominal resolution of 13.3 bits in a 1V range has been demonstrated, while the resolution varies in the range 11.4-13.7 bits in the presence of process variations and mismatch.

As a case study application, the proposed ramp generator has been used to enable the on-chip implementation of a reduced-code linearity test technique for pipeline ADCs. The proposed BIST strategy is based on a discrete-time integrator-based servo-loop that employs the developed ramp generator to provide the test stimulus. The proposed test technique has been validated by realistic behavioral simulations using actual data from an 11-bit 2.5 bits/stage pipeline ADC IP provided by STMicroelectronics. Obtained results show that the combination of the proposed ramp generator and the reduced-code linearity test technique yields an accurate estimation of the static linearity characteristic of the ADCUT across the complete conversion range, while only measuring the widths of 6% of the total number of codes.

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