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Editorial

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JETTA Editorial Board held its annual meeting at Washington, D.C. on November 11, 2019. The following picture shows, left-to-right, Faith Pilacik (Editorial Assistant, Springer), Said Hamdioui, Patrick Girard, Mehdi Tahoori, Magdi Abadir, Chen-huan Chiang (TTTC Chair}, Steve Sunter, Sybille Hellebrand, Hans-Joachim Wunderlich, Hans Manhaeve, Krishnendu Chakrabarty, Haralampos Stratigopoulos, Stefano Di Carlo, Naghmeh Karimi, Erik Jan Marinissen, Cheng-Wen Wu, Charles Glaser (Editorial Director, Springer), Adit Singh, and Anita Lekhwani (Senior Editor, Springer). Also present at the meeting but missing from the picture is Rubin Parekhji. Krishnendu Chakrabarty ran the proceedings since personal commitments kept me away from the meeting.

The cover of *JETTA* carries a statement of our cooperation with the Test Technology Technical Council (TTTC) of the IEEE Computer Society. We recently announced the 2018 JETTA-TTTC Best Paper Award for the paper "Address Remapping Techniques for Enhancing Fabrication Yield of Embedded Memories," by Shyue-Kung Lu, Hao-Cheng Jheng, Hao-Wei Lin and Masaki Hashizume, that appeared in *Journal of Electronic Testing: Theory and Applications*, Volume 34, Number 4, pp. 435–446, August 2018. The next photograph shows Yervant Zorian (left), TTTC President and *JETTA* Editor, presenting the Award to Shyue-Kung Lu, who also represented his three other coauthors. The presentation occurred at a plenary session of the *International Test Conference* on November 14, 2019 in Washington, D.C., USA.

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This issue contains twelve articles including three *Letters*. The topics discussed are fault tolerance, FPGA testability, RF device aging, transceiver calibration, delay testing, hardware security, system test, and 3D-stacked device testing.

The first paper addresses faults caused by crosstalk, noise and transients in a wireless network on chip (WiNoC). A dynamic voltage and frequency scaling (DVFS) method here provides significant error avoidance with low power and area overheads. Contributors of this research are Ouyang, Wang, Hu and Liang from Hefei University of Technology, Hefei, China.

The second paper follows the theme of testable FPGA design for real time signal processing applications. The proposed methodology emphasizes fault localization and reconfiguration. Authors are Palchaudhuri and Dhar from Indian Institute of Technology, Kharagpur, India.

Contributors of the third paper are Yang from Tianjin University, Tianjin, China and Feng from Carleton University, Ottawa, ON, Canada. They train an artificial neural network to predict the age-related degradation in the performance of an RF device.

Our fourth paper comes from Moon, Choi, Keezer and Chatterjee of Georgia Institute of Technology, Atlanta, GA, USA. Their test hardware helps a conventional automatic test equipment (ATE) efficiently measure the time-domain reflectometry (TDR) and other calibration signals.

In the fifth paper, small delay defects (SDD) are analyzed by Hasib, Savaria and Thibeault from École de Technologie Supérieure, Montréal, Canada. The main idea of this research is to study how process-voltage-temperature (PVT) variations influence the testing of SDD. An interesting finding is that testing at higher voltage largely eliminates the dependence of the test result on PVT.

Next, two papers address hardware security. The sixth paper of this issue gives a procedure for finding tests for malicious hardware. Such hardware, known as Trojan, may have a signal called payload and a group of trigger signals. Detection becomes harder as the trigger group grows larger. The technique in this paper examines payload's input and output cones for signals that are most likely to be triggers. Contributors of this work are Sebt and Beitollahi from Iran University of Science and Technology, Tehran, Iran and Patooghy from University of Central Arkansas, Conway, AR, USA.

Continuing with the theme of security, the seventh paper presents a design of physical unclonable functions (PUF) using random variations of node capacitances within

differential gates. Deep learning attacks by artificial neural networks (ANN) then assess the level of security achieved. Contributors of this work are Yu and Wen from Old Dominion University, Norfolk, VA, USA.

The eighth paper is on system test generation. The technique represents the function as a directed graph in which testing must traverse all edges. Using various criteria, the paper finds that the solution of the Chinese Postman Problem (CPP) gives the best result. Authors are Mariano from National Institute for Space Research – INPE, SP, Brazil, de Souza and Endo from Federal Technological University – UTFPR, PR, Brazil, and Vijaykumar from Federal University of Sao Paulo – UNIFESP, SP, Brazil. They had presented an earlier version of this paper at the 20th *IEEE Latin-American Test Symposium* (LATS), Santiago, Chile, March 11–13, 2019.

The ninth paper examines the test access and test application problems specific to 3D-stacked devices. An FPGA solution provides an effective interface between the automatic test equipment (ATE) and the device under test (DUT). The improved test access and reorganization of test resources reduce the test time and the switching activity on DUT during test. Authors are Sun, Zhang, Jiang, Dworak and Manikas from Southern Methodist University, Dallas, TX, USA, Nepal from University of St. Thomas, Saint Paul, MN, USA, and Bahar from Brown University, Providence, RI, USA. They presented an earlier version of this work at the 28th *IEEE North Atlantic Test Workshop* (NATW), Essex, VT, USA, May 13–15, 2019.

Next, we have three *JETTA Letters*.

In the first *Letter*, Gorantla and Deepa from Government College of Technology, Coimbatore, India present several approximate arithmetic circuits for image processing. Judicious approximations in circuit design and some area overhead help achieve enhanced energy efficiency and error tolerance.

The second *Letter* gives a design for a latch with error tolerance in presence of single event upsets (SEU). The cost is six extra transistors over an original design of eight transistors. Authors are Dai, Wang, Chu and Liu from Hohai University, Changzhou, Jiangsu, China, Cai from China Institute of Atomic Energy, Beijing, China, and Yan from Jiangsu Jotry Electrical Technology Co. Ltd., Changzhou, Jiangsu, China.

In the third *Letter*, Zhou, Li and Zhao from Beijing Institute of Technology, Beijing, China study several designs of phase locked loops (PLL) for reduced phase noise and spur.

Completing Volume 35 of *JETTA*, we now look forward to another fruitful year in 2020.