Journal of Signal Processing Systems (2020) 92:1153–1154
https://doi.org/10.1007/s11265-020-01593-4

Guest Editorial Note: Special Issue on Applied Reconfigurable Computing

Georgios Keramidas[1] · Nikolaos Voros[2] · Michael Huebner[3] · Diana Goehringer[4]

Published online: 29 August 2020

1 Description of the Topic

Reconfigurable computing platforms offer increased performance gains and energy efficiency through coarse-grained and fine-grained parallelism coupled with their ability to implement custom functional, storage, and interconnect structures. The growth of the capacity of reconfigurable devices, such as FPGAs, has created a wealth of new research opportunities and intricate engineering challenges. Within the past decade, reconfigurable architectures have evolved from a uniform sea of programmable logic elements to fully reconfigurable systems-on-chip (SoCs) with integrate multipliers, memory elements, processors, and standard I/O interfaces. One of the foremost challenges facing reconfigurable application developers today is how to best exploit these novel and innovative resources to achieve the highest possible performance and energy efficiency; additional challenges include the design and implementation of next-generation architectures, along with languages, compilers, synthesis technologies, and physical design tools to enable highly productive design methodologies.

The purpose of this special issue is to provide an insight into current research and development in aspects related to reconfigurable computing. This special issue includes six papers that were presented in the 2018 edition of the International Symposium of Applied Reconfigurable Computing (May 2018 in Santorini, Greece). The six articles were appropriately selected (based on their quality) in order to cover various topics of the Symposium. The articles have undergone rigorous peer-review according to the journal's high standards.

2 Articles of this Special Section

The article "An FPGA-based Accelerated Optimization Algorithm for Real-Time Applications" studies and proposes an FPGA-based acceleration of a low-complexity optimization algorithm, namely Big Bang-Big Crunch (BB-BC). The proposed technique describes a novel, fully parameterized and pipelined FPGA design of the BB-BC algorithm and a parallel scheme which integrates several BB-BC engines to improve performance.

The article "VerCoLib: Fast and Versatile Communication for FPGAs via PCI Express" presents a highly configurable hardware interface that supports DMA-based connections to a host system as well as direct communication between multiple FPGAs. The proposed implementation offers unidirectional channels to connect FPGAs, allowing for precise adaptation to all kinds of use cases e.g., multiple channels to the same endpoint can be used to realize independent data transmissions.

The article "SDMPSoC: Software-defined MPSoC for FPGAs" proposes an automatic development environment for heterogeneous and FPGA-based MPSoCs. Based on an MPI program, a heterogeneous MPSoC for FPGAs consisting of an arbitrary number of MicroBlaze processors and hardware modules is generated. All hardware modules can be easily programmed in the MPI program and are synthesized using high-level synthesis.

The article "Towards Accelerated Genome Informatics on Parallel HPC Platforms: The ReneGENE-GI Perspective"

✉ Georgios Keramidas
gkeramidas@csd.auth.gr

Nikolaos Voros
voros@teiwest.gr

Michael Huebner
Michael.Huebner@ruhr-uni-bochum.de

Diana Goehringer
diana.goehringer@tu-dresden.de

[1] Aristotle University of Thessaloniki, Thessaloniki, Greece

[2] University of Peloponnese, Tripoli, Greece

[3] Brandenburg University of Technology, Cottbus, Germany

[4] Technische Universität Dresden, Dresden, Germany

presents ReneGENE-GI, an innovatively engineered Genome Informatics (GI) pipeline. The article details the performance analysis of ReneGENE-GI's Comparative Genomics Module (CGM), the compute intensive stage of the GI pipeline. ReneGENE-GI proposes a dedicated acceleration fraemworks by exploiting the inherent parallelism and scalability of the reconfigurable hardware at the level of micro and system architecture.

The article "Tackling Critical Challenges towards Efficient CyberPhysical Components & Services Interconnection: The ATLAS CPS Platform Approach" proposes a holistic end-to-end CPS architecture based on message passing communication technologies able to support the inherent complexity of respective deployments spanning several areas of applied industrial research and development. The proposed architecture aims to serve as a roadmap on how existing, prominent technologies from different domains can be effectively integrated and address all changes while be applied in diverse application demands.

Finally, the article "An Accelerator for Resolution Proof Checking based on FPGA and Hybrid Memory Cube Technology" presents an FPGA accelerator for checking resolution proofs, a popular proof format. The proposed accelerator exploits parallelism at the low level by implementing the basic resolution steps in hardware and at the high level by instantiating a number of parallel modules for proof checking.

Acknowledgments Several people contributed to this special issue. We would like to thank all the authors for their valuable contributions. Special thanks also to the researchers who contributed to the reviewing process. We hope that this special issue will serve as a valuable resource for the reconfigurable computing community.