Flexible and Reconfigurable Implementation of Link Adaptation Algorithms

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Abstract - Reconfigurable systems using FPGAs are of growing interest for the design and implementation of software defined radio transceivers. By reconfiguring a FPGA, its hardware resources can be reused and shared to provide multiple functionalities on a single device. This paper investigates power savings by means of partial reconfiguration for implementing two link adaptation algorithms. These algorithms provide variable performance in terms of spectral efficiency and hardware utilization at different average SNRs. In order to obtain the best tradeoff between i) spectral efficiency and ii) area and power consumption, we propose an efficient implementation that switches between the two algorithms by means of partial reconfiguration. Our experimental results show that our implementation provides a high spectral efficiency and, for certain SNR regions, reduces the hardware resources and thereby the power consumption.

Keywords—FPGA, Reconfiguration, Link Adaptation.

Abbreviations: BER: Bit Error Rate; CLB: Configurable Logic Block; DSP: Digital Signal Processor; E2R: End-to-End Reconfigurability; FPGA: Field Programmable Gate Array; HIPERLAN: High PERformance Local Area Network; LA: Link Adaptation; OFDM: Orthogonal Frequency Division Multiplexing; PR: Partial Reconfiguration; QAM: Quadrature Amplitude Modulation; RSSI: Received Signal Strength Indication; SAMPDA: Subcarrier based Adaptive Modulation and Power Distribution Algorithm; SDR: Software Defined Radio; SNR: Signal to Noise Ratio; SR: Software Radio; SRA: Simple Rate Adaptive algorithm

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1. Introduction

Current trends in wireless technology demand high spectral efficiency and Quality of Service (QoS) to serve the users with high data rates. Link Adaptation (LA) is one of the techniques to improve the spectral efficiency by compensating channel impairments on the wireless link [1]. It is a technique which adapts the transmission link by changing the transmission parameters through bit loading and power adaptation algorithms according to the channel conditions. Bit loading is performed in link adaptation by assigning appropriate modulation schemes for corresponding Signal to Noise Ratio (SNR) which is measured from current channel conditions. The LA algorithms utilized in this paper exploit the advantages of multi-carrier techniques such as Orthogonal Frequency Division Multiplexing (OFDM) which serves as the PHY layer for several standards like IEEE 802.11a and ETSI HIPERLAN/2 [2].

No single modulation scheme serves for all link conditions as real-time channels change continuously. LA aims at selecting an appropriate modulation scheme by measuring the link quality in terms of Received Signal Strength Indication (RSSI) and SNR [2]. Based on the parameters that are fed back to the transmitter, an appropriate modulation scheme for each sub-carrier is assigned. More specifically, the two algorithms used in this work are the Simple Rate Adaptive algorithm (SRA) and Sub-carrier based Adaptive Modulation and Power Distribution Algorithm (SAMPDA) which both improve the throughput [2], [3].

1.1 Flexibility Through Reconfiguration

Along with high QoS requirements, modern wireless devices demand more flexibility in terms of design and operation. By performing signal digitization closer to the antenna, more flexibility is obtained for implementing different baseband functionalities and transmitter/receiver algorithms in software. The ideal Software Radio (SR) [4] digitizes the signal right after the antenna which is impractical due to stringent requirements in analog-to-digital conversion, low noise amplification and high sampling rate requirements. The Software Defined Radio (SDR) is a realizable form of SR taking into account those practical limitations [5]. Therefore, SDR has the possibility to be a promising candidate in the development of future wireless devices which offers more flexible operation among multiple standards or services through End-to-End Reconfigurability (E2R) [6]. By performing reconfiguration, interoperability and E2R can be realized on the same hardware device.

For implementing SDR architectures, Field Programmable Gate Array (FPGA) is one of the suitable platforms, as it can perform dynamic reconfiguration. FPGAs can be reconfigured in two ways: complete and partial [7]. Complete reconfiguration deals with reconfiguring the full FPGA whereas by using Partial Reconfiguration (PR), it is possible to reconfigure part of the FPGA while maintaining operation of the rest of the device. Partial reconfiguration provides advantages like reduced power consumption and efficient use of available silicon area. Moreover, power consumption can be controlled by optimizing the algorithm design in terms of parallel processing solutions. At a lower level, many vendor specific power reduction techniques can be used during the implementation stage in the synthesis, map, and place-and-route processes [8].

Hence, partial reconfiguration appears to be suitable for employment in SDR transceivers where a particular functionality that requires a change is reprogrammed without modifying the remaining functionality. This offers both flexibility and also potential power savings as only the required hardware is active. In order to investigate the feasibility and performance of such an approach, we present the design, implementation and results analysis of applying dynamic PR for two LA algorithms which switch according to a decision algorithm. The decision algorithm selects the appropriate LA algorithm depending on the current channel conditions. This results in a flexible and efficient means of implementing both algorithms to achieve better spectral efficiency along with reduced hardware resource utilization, which in turn reduces the power consumption significantly.

The rest of this paper is organized as follows: Section 2 introduces and compares the two LA algorithms and motivates the need for employing partial reconfiguration. Section 3 presents the decision algorithm used for the reconfiguration. Section 4 discusses the simulation and implementation details of the PR. Section 5 describes the results in terms of spectral efficiency,

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power consumption, available sub-carriers, and flexibility. Finally, conclusions are presented in Section 6.

2. LA Algorithms and Motivation for Reconfiguration

In this section, the SRA and SAMPDA algorithms are described and compared in terms of spectral efficiency. Moreover, a reconfigurable implementation is motivated by comparing their performances and hardware utilizations. The numbers used in this comparison have been obtained in our previous work [3].

2.1 Link Adaptation Algorithm

The SRA algorithm is a bit loading algorithm where the sub-carriers are modulated with one of the schemes among 4QAM, 16QAM, 64QAM and 256QAM. First of all, a predefined threshold SNR is calculated for each modulation scheme to attain a target Bit Error Rate (BER). The SRA algorithm starts with equal power distribution for all sub-carriers. The received instantaneous SNR with equal power distribution is compared with a threshold SNR for selecting a modulation scheme for each sub-carrier. A higher modulation scheme is selected if the received SNR is higher than the corresponding threshold SNR. A zero modulation scheme is selected when the SNR of a sub-carrier is less than the threshold SNR of the 4QAM modulation scheme. When a sub-carrier is selected with zero rate, it is switched off from the transmission. The transmission power is redistributed among the other sub-carriers and the modulation scheme assignment process is repeated [2].

The SAMPDA algorithm builds upon a similar initial power distribution method as the SRA algorithm; however, the bit loading and power adaptation are different. A best sub-carrier is chosen based on the minimum power increment required for the next level of modulation scheme. If the needed power increment is less than the available power, the best sub-carrier is upgraded to the next higher modulation scheme. After re-distributing the power, the process is repeated until the available power is less than the transmission power [3].

2.2 Motivation for Investigating Partial Reconfiguration

In order to obtain the best tradeoff between spectral efficiency and area (and thus power consumption), we have to compare the two LA algorithms. The comparison in terms of theoretical spectral efficiency is presented in Figure 1 (at this point the reader should only consider the SRA and SAMPDA curves and disregard the PR curve). Besides this, the algorithms have been implemented on a Xilinx Virtex-4 SX35 FPGA; Table 1 shows the corresponding execution time and hardware resource utilization.

The spectral efficiency provided by the SRA and SAMPDA algorithms is almost equal for SNRs below 10 dB and above 40 dB, as shown in Figure 1. Between 10 and 40 dB, the SAMPDA algorithm performs better than the SRA algorithm. As shown in Table 1, the SRA algorithm utilizes less hardware resources than the SAMPDA algorithm (35% and 94% of the logic slices, respectively), but its execution time is larger (0.69ms and 0.29ms, respectively): although SAMPDA is more complex than SRA, it has a higher inherent level of parallelism (which requires more resources) and, at the same time, it requires less iterations for the allocation procedure, thus has a smaller execution time. By observing these two aspects, it appears that switching between the two LA algorithms, depending on the SNR conditions, can be used to achieve a good spectral efficiency while minimizing hardware resources and thus reducing power consumption.

This can be efficiently achieved by means of a partially reconfigurable FPGA: it is possible to easily switch between the two LA algorithms (the switching decision algorithm is discussed in section 3) and, moreover, only one algorithm is configured and active at a time, which reduces the amount of active hardware resources and thus reduces the power consumption.

In this paper we follow the Xilinx Virtex-4 partial reconfiguration procedures [9]. In order to perform the partial reconfiguration on the FPGA, the system is partitioned into two modules: static and dynamic. The partitioning into static and dynamic modules is a critical step in implementing a

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reconfigurable system. It is also possible to have a static module and multiple dynamic modules in a single partially reconfigurable system. The smaller the number of reconfiguration blocks (i.e. dynamic modules), the less complex the implementation. The size of the dynamic module is also an important aspect to be considered as it affects the reconfiguration time, i.e. the time needed to re-configure the dynamic module [9].

Deciding on the static and dynamic modules requires efficient design space exploration at the algorithmic level by identifying common blocks which can share the same hardware resources. In Xilinx FPGAs the communication between the static and dynamic modules is handled by Xilinx specific bus-macros [9]. As the data transfer through the bus-macros is limited, it is necessary to minimize the communication between the static and dynamic modules. In the current system, the partitioning is as shown in Figure 2. The static module consists of all the baseband processing blocks which are required all the time as well as the decision algorithm block. The dynamic module is configured with one of the two LA algorithms, based on the selection information provided by the decision algorithm.

3. Decision Algorithm

The decision algorithm is based on the following three selection performance metrics: spectral efficiency, execution time and number of available sub-carriers. All these performance metrics for SRA and SAMPDA algorithms vary in different average SNR ranges as shown in Figure 1, 4 and 5, respectively (at this point the reader should only consider the SRA and SAMPDA curves and disregard the PR curve). So, each performance metric, as a function of the average SNR, influences the selection of the appropriate algorithm. The decision algorithm allows the user to select between the performance metrics: choice 1 (*Ch1*) optimizes the spectral efficiency, whereas choice 2 (*Ch2*) optimizes both the execution time and number of available sub-carriers.

The decision algorithm selects the appropriate LA algorithm based on the average SNR of the sub-carriers for the selected performance metric. The choice of the algorithm and the value of the average SNR are sent to the corresponding dynamic module through the bus macros. The dynamic module also receives the individual SNRs of the sub-carriers through the bus-macros, which are calculated in the static module. With the two inputs, the bit loading is performed as explained in subsection 2.1.

Once the communication between the static and dynamic modules is designed, the designers can individually develop and implement the static and dynamic modules in parallel, which offers some flexibility in the design flow. The inputs to the algorithms in the dynamic module are the average and instantaneous SNRs of the sub-carriers. This also offers the flexibility to change either SRA or SAMPDA algorithms with other LA algorithms, without changing the whole system. It is also possible to optimize existing algorithms independently, and to update the dynamic module only.

In this work, an algorithmic optimization is done in order to reduce the execution time and power consumption. Each of the algorithms, when operated independently, takes the SNR of the individual sub-carriers and calculates the average SNR for every iterations i.e. while assigning the modulation scheme. In the current system model with partial reconfiguration, the decision algorithm itself calculates the average SNR. Hence, the average SNR calculation in the individual algorithms is omitted, which reduces the number of computations and power consumption for the selection of the algorithms. The limitations on the bus macro communication on current generation of FPGAs restrict algorithm optimizations to a certain degree. With more flexible bus macro communication, significant reduction in power, area and computational requirement of the dynamic module should be possible.

The specific conditions for reconfiguration based on SNR are shown in Figure 3. The background for the decision scheme is that in all the cases where SRA and SAMPDA give similar performance, SRA is selected because of its lower hardware resource utilization which results in reduced power consumption.

If the spectral efficiency (*Ch1*) is considered, then the SRA algorithm is selected when the SNR is in the region [1;10] dB or greater than 40 dB, while the SAMPDA algorithm is selected when the SNR is in the region [10;40] dB.

Similarly, when the optimization is needed in terms of execution time and/or available number

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of sub-carriers, the selection metric is chosen as *Ch2*. In this case, when the SNR is below 25 dB, SAMPDA algorithm is selected since it offers better performance. When the SNR exceeds 25 dB, the SRA algorithm is selected as is offers better or similar performance at lower resource utilization.

4. Simulation of the Switching Algorithm and Implementation of the PR

The switching algorithm and the LA algorithms are simulated with Matlab for an OFDM system considering 512 sub-carriers with a bandwidth of 5 MHz. The channel model considered is an SUI-4 (Stanford University Interim) model. The simulations are carried out up to 50 dB SNR with a frame duration of 1 ms for a target BER of 10^{-3}. The simulations are performed to observe the performance of the individual algorithms in terms of spectral efficiency, execution time and number of available sub-carriers. The results of the simulation considering the decision algorithm and the PR system are shown in Figures 1, 4 and 5 (the PR curves) and are compared with the performance of the individual algorithms (SRA and SAMPDA curves). By looking at these results, it is possible to conclude that the switching algorithm offers a good trade-off between spectral efficiency, execution time, number of sub-carriers and the channel conditions (SNR). Since this is a promising result, an actual implementation has been carried out.

The SRA and SAMPDA algorithms are implemented individually on a Xilinx Virtex-4 FPGA. The algorithms are coded in the Handel-C language [10] and compiled with AgilityDS (formerly Celoxica) DK Design Suite. Several possibilities of introducing parallelism have been studied to explore the area vs. execution time trade-off. As the area increases the execution time reduces and vice versa. The Handel-C codes are compiled to generate VHDL files which are synthesized and implemented using Xilinx' ISE tool to generate the bit-stream files which are used to configure the FPGA. These configuration files are stored in a memory external to the FPGA. Based on the decision algorithm selection, the corresponding LA algorithm is loaded and configured into the FPGA. Different power reduction options in synthesis, map, place-and-route steps are enabled in the tool. The resource utilization results are collected from Xilinx' ISE tool for the target FPGA.

In the partial reconfiguration process on the current generation of FPGAs [9], the area assigned for the dynamic module is fixed. So, the size of the dynamic module depends on the largest dynamic module. In the current system, SAMPDA occupies more area than SRA. When SRA is configured onto the FPGA, the remaining space assigned for the dynamic module is idle, which can lead to considerable power savings which is a great advantage for power limited systems. The results are discussed in the next section.

5. Results

The hardware resource utilization is an important parameter to be considered for assessing the performance of the implementation. The dynamic power consumption of the FPGA design depends on the resource utilization. Hence, reducing hardware resources causes a reduction in power consumption [9]. As seen in Table 1, the SRA and SAMPDA algorithms use 35% and 94% of the total number of slices, respectively. So, when SRA is used, the hardware utilization is about 63% lower as compared to SAMPDA. Based on the area utilization, the power consumption has been estimated by considering the power consumption of the individual logic slices of the FPGA. Four logic slices constitute a single CLB in Xilinx Virtex-4 FPGAs and one CLB consumes approximately 5.9 μW per MHz [8]. This is reflected in Table 1: the SRA algorithm consumes 7.9 mW/MHz whereas the SAMPDA algorithm consumes 21.3 mW/MHz. So the PR implementation enables power savings of up to 13.4 mW/MHz, in different SNR regions when the SRA algorithm is selected by the decision algorithm.

6. Conclusions

In this paper, the application of partial reconfiguration in performing link adaptation has been investigated. Two algorithms have been compared in terms of spectral efficiency, execution time,

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number of sub-carriers, and hardware resource utilization. In order to obtain the best tradeoff between those parameters a switching decision algorithm has been devised. Matlab simulations have shown that this algorithm can provide a good tradeoff. Moreover, a partially reconfigurable FPGA implementation has been evaluated. By selecting the appropriate link adaptation algorithm according to the current link conditions, power consumption can be reduced without degrading the performance in terms of spectral efficiency and number of sub-carriers.

Based on this work, it can be concluded that partial reconfiguration paves the way for designing and implementing flexible and efficient elements of communication systems. However, it is still necessary to perform efficient design space exploration at different levels (such as algorithmic and architectural) of the design and implementation processes and to take into account the vendors' specific architectural, tooling and procedural constraints for partial reconfiguration.

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Figures:

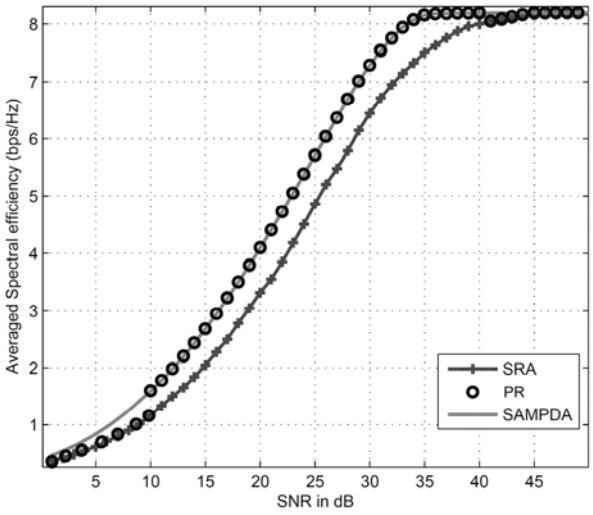

Fig. 1. Comparison of SRA, SAMPDA and PR system interms of spectral efficiency.

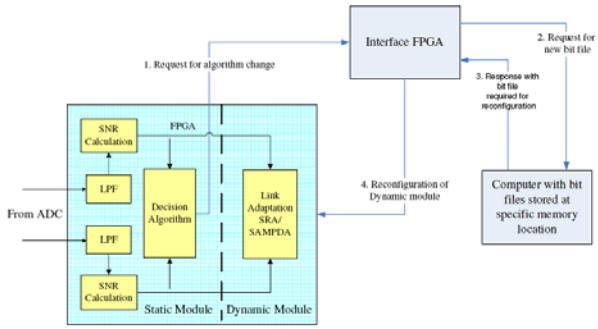

Fig 2: Partitioning of the system on the FPGA for partial reconfiguration.

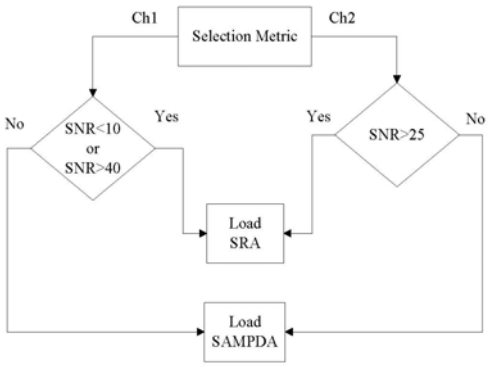

Fig. 3: Decision algorithm for selecting the appropriate LA algorithm, where Ch1 optimizes the spectral efficiency and Ch2 optimizes the available number of sub-carriers.

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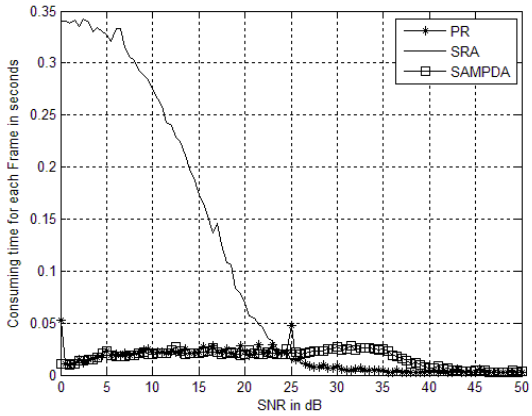

Fig. 4: Comparison for SRA, SAMPDA and PR algorithms in terms of execution time.

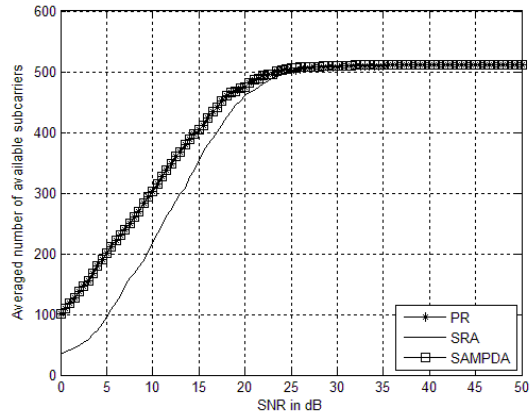

Fig. 5: Comparison for SRA, SAMPDA and PR algorithm in terms of number of available sub-carriers.

Table 1: Implementation details on Xilinx Virtex-4 FPGA

Algorithm	Resource Utilization (% of 15360 slices)	Execution time [ms]	Power consumption Estimate [mW/MHz]
SRA	35%	0.69	7.9
SAMPDA	94%	0.29	21.3

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