Low-Power SRAM Cell and Array Structure in Aerospace Applications: Single-Event Upset Impact Analysis

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Abstract

One of the most critical functions of a computer is memory, as it would be impossible for it to function efficiently without it. The main memory of a computer is known as Random Access Memory (RAM). It stores operating system software, applications, and other data for the central processor unit (CPU) to perform operations swiftly and efficiently. Unfortunately, traditional static RAM (SRAMs) in aerospace applications suffers from high soft error issues such as Single Event Upset (SEU). To overcome the soft error problems, many Radiation-Hardened-Based Designs (RHBD) and Radiation-Hardened-Polar Designs (RHPD) have been developed, such as 12T We-Quatro, twelve-transistor (12T) Dice SRAM cells, and so on. However, they consume more total and static power, as well as have more delay and area. In this article, an RHPD and RHBD 12T SRAM cell is proposed to reduce power dissipation and area overhead. Compared to RHPD, the RHBD 12T SRAM cell devours less total and static power, and RHPD cells have less delay. The proposed SRAM cell is implemented in the 32 x 32 array architecture. The power consumption of a 32 x 32 SRAM array with a 12T RHBD SRAM cell is 1.33mW, which is 10.1% less than a 32 x 32 SRAM array with a 12T RHPD SRAM array is 4.23mW. Cadence virtuoso 6.1.5 at 45 nm Generic Process Design Kit (GPDK) technology file is used to simulate the comparative analysis for the SRAM cell.

1 Introduction

The usage of electronic devices and integrated circuits have increased in recent years because of technological advances [1]. The advancement of Complementary Metal Oxide Semiconductor (CMOS) process technology results in a smaller semiconductor system [22]. SRAM is the basic building block of most electronic devices, providing maximum performance and low power consumption. SEU, caused by radiation particles, makes it impossible for hardware devices to operate reliably in high-radiation conditions like space [23]. Fig. 1 explains problems of SEU occur. SEU in SRAM, in general, is a significant source of concern. Many radiation-hardened SRAM bit-cells have been proposed to solve this issue. For SRAM designs in aerospace applications, the soft error rate, power consumption, size, and delay are the most critical metrics to consider. In addition, SRAM cells take up much space in the device on the chip [24-27].

In recent years, several RHBD cells have been demonstrated to provide radiation fault-free cache memory, including the 12T Dice, 12T We-Quatro, and 14T cell [21]. Two latch pairs employed effective feedback to obtain the original value of a 12T RHBD Dice in the cell. Two access transistors are added to a 10T-Quatro cell to achieve strong writ ability in a 12T We-Quatro cell [3]. The above-mentioned RHBD cells, such as Dice, We-Quatro, and boosted-Quatro, require more power when going slower. The above-mentioned RHBD cells, such as Dice, We-Quatro, and boosted-Quatro, use more power when travelling slower. The 10T RHBD SRAM cell was intended to overcome a problem with a big area and high power consumption [15]. However, it has the disadvantage of having a high rate of write loss. As a result, creating an RHBD cell with a higher frequency combination of all parameters is a challenge. A new

radiation-hardened [4] 12T SRAM cell has been proposed to achieve low power dissipation, high write speed, and higher frequency.

Aside from RHBD cells, RHPD is offered, which is based on the polarity upset mechanism of NMOS transistors' single-event transient voltage [6-8]. A 12T RHPD SRAM cell [5] is also employed to boost the reliability and speed of space applications. The parasitic bipolar amplification of the PMOS transistor is higher than that of the NMOS transistor. In IC's, a charge-sharing effect between NMOS transistors within the circuit occurs, making the heavy-ion strike's distortion more severe. As a result, by adopting multi NMOS transistor designs to lessen the charge-sharing effect inside the circuit, the circuit's SEU dependability can be boosted even further [10-12]. Using more NMOS transistors and a lower transistor size will have great radiation-hardened capabilities and good write ability [14]. In addition, it has a lower write failure probability than other SRAM cells, including Dice, We-Quatro, and 14T SRAM cells.

This paper is mainly structured as follows: Chapter 2 describes the existing design and in Chapter 3 describes the proposed method, and Chapter 4 discuss the 32 x 32 SRAM Array. Chapter 5 describes the performance and analysis, and Chapter 6 includes the conclusion.

2 Conventional Rhbd Sram Cells

2.1 10T SRAM Cell

The DICE, We-Quatro cells are discussed in [2, 3, and 9]. Due to the significant latency of the 10T cell, the schematic of a 10T SRAM cell in 45 nm CMOS technology indicates imminent write failure for high frequency (1 GHz) and 1V supply voltage is shown in figure 2.

The simulated response of the 10T-SRAM cell is shown in figure 3. According to the response, the 10T cell has a write failure at 1 GHz. Due to the SEU effect, the output node "B" is unable to complete flip due to the "N2" s weak pull-up strength. Therefore, when the voltage at the output node "A" is dropped, the transistor "N4" is turned "OFF," leading the transistors "P1" and "P6" to switch "ON," flipping the output node "B" to VDD and creating the 10T cell's writ ability issue [4 and16].

2.2 DICE SRAM Cell

Figure 4 shows a schematic representation of the DICE SRAM cell. It's one of the RHBD cells utilized in radiation sensitivity testing. It took 12T to develop a DICE Cell [2], which comprises of two interlocked latch pairs that employ positive feedback to revert to the original value, at the cost of its massive scale, power consumption, speed, and noise margin. "A, B, C, and D" are the labels for the four output nodes. When "A" equals 0, "C" equals 0, and "B" equals 1, "D" equals 1. The value recorded in the output node "B" ('1) is automatically flipped to '0' as node "B" is exposed to radiation. The P3 is completely reliant on node "B," which has been temporarily turned "OFF". The N5's gate, on the other hand, is connected to both node "B" and node "N2". As a result, the reduced voltage at node "B" has little influence on nodes "A & C". Finally, P2 and N7 aid in the recovery of the "B" and "C" disruptions.

2.3 WE-QUATRO SRAM Cell

The WE-QUATRO SRAM Cell [3, 9] is depicted schematically in Figure 5. It's also one of the RHBD cells that's employed in radiation sensitivity testing. This circuit contains 12 transistors. On the other hand, We-Quatro uses four access transistors to link 'B' and 'C' to BL and 'A' and 'D' to BLB using four access transistors. In this approach, four storage nodes are accessed at the same time during the write operation.

3 Proposed Rhbd And Rhpd Sram Cell

3.1 12T RHBD SRAM Cell

As shown in Fig. 6, the suggested cell has twelve transistors. Because the write failure rate of the 10T SRAM cell is greater [4, 18]. Two more transistors, N3 and N4, have been added to the 10T cell in the proposed cell to prevent write failure. There are twelve transistors in the We-Quatro and Dice cells, with four PMOSs (P1–P4) and eight NMOSs (N1–N8). It consumes more power because it has more NMOSs and because the design configuration allows all the transistors to be active during reading and writing mode. The power and area expenses have been reduced due to smaller transistors (all transistors are the same size except P3 and P4 (2.0)) and more PMOS. The write speed and write Static Noise Margin (SNM) have risen as more N3, and N4 access transistors have been added. The higher hold stability is related to the larger scale of P3, P4, and the transistors' connection.

During the Hold State, the logic '0' is applied to WL. Because WL = '0,' all-access transistors N1–N4 will be "OFF" in this case. As a result, bit lines will be separated from the stored value at the latch's output node, and the output will remain unchanged. While the logic signal is active high ('1'), the circuit is similarly connected from the bit lines to WL. This is referred to as active mode [17]. The pre-charge circuit gives high voltage to both the BL = '1' and BLB = '1' during the read operation. There is no BL voltage discharge if the proposed cell has a high value [19-20].

The BLB voltage will be discharged, and the stored output will be lowered because both bit lines are coupled to the sense amplifier (SCSA), which supplies the digital output. For example, assume you wish to write '1' in a cell that is now set to '0', and you want BL = '1' and BLB = '0'. When WL = '1', transistors N1–N4 will be "ON," transistors N6, P2, P4, P5 will be "ON," and transistors P1, N5, P3, P6 will be "OFF," causing the cell's store output to move from '0' to '1'. As a result, the write operation is quick and painless. The ideal function of the proposed cell is depicted in Figure 7.

3.2 12T RHPB SRAM Cell

Figure 8 depicts the planned RHPD-12T memory cell. The RHPD-12T cell [5] is made up of two PMOS transistors and ten nMOS transistors. Pull-up transistors (N1, N2, P1, and P2) have W/L values of 80/45 nm, whereas drive transistors (N3, N4, N5, and N6) have W/L values of 280/45 nm. The access

transistors are four extra nMOS transistors N7–N10 (W/L = 140/45 nm) with a conventional word line connecting their gates (WL). Thus, it contains two fewer PMOS transistors and four more NMOS transistors than the RHBD design.

When WL is set to low (“0”), the cell is in the hold mode, and four access nMOS transistors are in the cutoff state. Two complementary signals are stored in each of the circuit’s four storage nodes in this mode (Q, QB, S0, and S1). All access transistors are turned on when WL is set to “1”. During the reading process, one of the bit lines will discharge across the circuit, resulting in a voltage difference between the two-bit lines. The SCSA sensing amplifier can detect voltage differences and convert them to readable digital signals. During a written procedure, bit lines will write the matching data to the four storage nodes.

The transient response of the 12T-RHPD SRAM Cell is shown in figure 9. Assume the stored value is logic "1," that is, A="1," B="0". During the reading process, the voltages of the two-bit lines are raised to high voltage “1” during the pre-charge stage. When WL is high (WL= “1”), the four access NMOS transistors and the four internal storage nodes are turned ON for the read operation. The voltage of BL stays “1,” while the voltage of BLB is lowered due to N3 and N6 discharge. For the write operation, the bit lines BL and BLN must be “1” and “0” respectively, assuming the data “1” is written. When the voltage of WL is high, the write operation is performed. Transistors N1, N3, and N6 are turned on, while P1 is turned OFF, and the Q node data is stored as “1,” indicating that data “1” may be successfully written into the proposed RHPD-12T memory cell.

4 Sram Array Structure

A write driver circuit, a pre-charge circuit, a sensing amplifier, and a row/column decoder are all part of a 32X32 SRAM array. An SRAM cell can store a single bit of binary data [28-30]. SRAM cells are organized in horizontal rows and vertical columns in an array.

In array architecture, word lines and bit lines are 2XN rows and 2XM columns, respectively. Therefore, the array’s average number of memory cells is 2(N+M) and thus 32 rows, and 32 columns are in 32 x 32 SRAM Array [13]. For quick read and write operations, each column has its write driver circuit and sense amplifier. Because of the differential writing and sensing technique, this architecture allows for simple read and write operations. For 45nm technology, the proposed 12T SRAM RHBD and RHPD cells are implemented in 32 x 32 SRAM array architecture for different voltages. Figure 10 depicts the SRAM series as a block diagram.

4.1 Address Decoder

A row decoder is another name for an address decoder. Because there are five address lines, the row decoder utilized is a 5:32 decoder. The use of a 32X32 array necessitates the use of 32-word lines, which the 5:32 decoder provides. Because the entire row is selected when any one of the address lines is selected, the matching word line rises high. The row decoder is responsible for this. The suggested address decoder is shown in figure 11.

4.2 Write Driver Circuit

The peripheral device utilized to implement the 32X32 KB array depicted in figure 12 is the write driver. The write driver circuit is employed during read operation, and read operation is started once the Write Enable (WE) is set to high. Data is then written in the form of voltage, accessed during reading operation via the sensing amplifier.

4.3 Precharge Circuit

A precharge circuit is employed when the circuit is idle and does not conduct any of the read or write activities depicted in figure 13. It is utilized to charge the bit-line, making the sense amplifier's job of sensing the voltage during read operations easier. These circuits can be essential for low power consumption because writing requires more power than reading operations. After all, it has more circuitry. Write driver circuits enter the picture during a write operation, and Write Enable (WE) gets high, while data is also written into it, increasing the requirement for more and more power.

4.4 Sense Amplifier

The sense amplifier's principal function is to measure the voltage difference between the two-bit lines and, as the name implies, to amplify that difference, i.e. to boost the weak signal. The use of sense amplifiers in an array is due to the discharge of one of the bit lines during a read operation, which requires boosting. Instead of employing a traditional Differential Sense Amplifier, the proposed sense amplifiers are 1) current latch sense amplifiers and 2) Self-Correcting Sense Amplifiers.

4.4.1 Current latch sense amplifier

Figure 14 shows a schematic representation of the CLSA structure. To produce a latch, the inverters on each branch (P1-N0 and P2-N1) were cross-coupled. N2 and N3 get input from the two bit-lines on their gate, while N4 is a sensing transistor until NMOS is "ON". The gate to source voltage of the two input transistors differs because one of the two-bit lines on the memory cell provides a lower voltage than the other. As a result, distinct currents pass through the two transistors, causing one of the output nodes (OA or OB) to discharge more slowly than the other. Finally, positive feedback is provided by the inverters' cross-coupling, which latches the slower discharging output node to VDD and the other node to GND.

4.4.2 Self Correcting Sense Amplifier

Figure 15 shows a schematic representation of the SCSA structure. PMOS transistors (P3 and P4) and NMOS transistors make up the two cross-coupled inverters (N4 and N5). Because they are connected to bit-line (BL) and complementary bit-line (BLB) at their respective gates, the NMOS transistors N0 and N3 are sensing transistors. The pre-charging modules P2 and P5 charge the output nodes OUT and OUT B to VDD until sensing. The Offset Direction Determining signal (ODD) is kept at logic heavy simultaneously,

causing the nodes preQ1 and preQ2 to be dragged to earth (GND). The inverters (PO and N11) provide rail-to-rail voltage fluctuations (P7 and N8). Until sensing, the last offset path outputs, Q1 and Q2, are held at GND by an INV1 and INV2 inverter.

5 Performance And Analysis

This section covers the proposed design's and the 32 x 32 array architecture and its building blocks performance and analysis in power, area, delay, process corner analysis, and SNM by using cadence EDA tool at 45nm technology.

5.1 Power Consumption and Delay analysis

Table 5.1
Performance and Parameter Analysis of Various SRAM Designs

Various SRAM Cells/Parameters	Total Power (µW)	Static Power (pW)	Write Delay (pS)	Read Delay (pS)	Area (μm^2)	HSNM (mV)	RSNM (mV)	WSNM (mV)
12T-RHBD SRAM Cell	0.931	21.3	11.668	83.21	4.29	361	151	198
12T-RHPD SRAM Cell	1.894	24.12	10.543	76.48	5.385	275	130	145
We-Quatro SRAM Cell	2.035	32.35	17.20	70.56	4.212	242	160	175
Dice SRAM Cell	1.36	28.15	16.43	63.25	4.507	198	175	224

The 12T RHBD SRAM cell decreases power dissipation and write delay in SRAM-based cache memory. The power, delay, and area of the SRAM cells under consideration are compared in Table 5.1. The overall power loss of the cell is calculated using the average power losses in the write, read, and hold modes. In read and write mode (WL = '1), it dissipates dynamic power, while in hold mode (WL = '0'), it dissipates static power. Table 5.1 demonstrates that the 12T RHBD cell outperforms the We-Quatro and Dice and 12T RHPD cells in terms of power, and that the 12T RHBD cell has less write latency than the 12T RHBD cell.

Table 5.2
Power consumption of Different Sense Amplifier

Sense Amplifier	Supply Voltage(V)	Power(µW)
Differential sense Amplifier	1V	42.89
Current latch sense amplifier	1V	39.79
Self-Correcting sense amplifier	1V	37.79

Table 5.2 shows that a self-correcting sense amplifier produces (37.79 μW)) less power consumption compared to propose Current latch sense amplifier and conventional differential sense amplifier.

Table 5.3 shows how various supply voltages are applied and implemented in 45nm technology for the 32X32 array and the average power consumption of the 32 x 32 array for the proposed SRAM cells. For example, a 32 x 32 SRAM array with a 12T RHBD SRAM cell consumes 1.1 mV for a supply voltage of 1V, which is 10.1% less than a 32X32 SRAM array with a 12T RHPD SRAM array, which consumes 3.2 mV.

Table 5.3
Power consumption of 32 x 32 SRAM Array

Supply Voltage (v)	12T-RHBD SRAM (mV)	12T-RHPD SRAM (mV)
1	1.1	3.2
1.1	1.3	3.4
1.2	1.42	3.7
1.3	1.7	4.1

Both SRAM cells are processed under the process corner analysis to simulate a circuit or device in worst-case and normal conditions. The average power consumption of process corner analysis of proposed SRAM cells is shown in figure 16. The process corner analysis for proposed SRAM cells applied for cell supply voltage is 1V. Compared to both SRAM cells, the RHBD cell's power for FF, FS, and TT process has reduced power consumption by 56.16%, 60.17%, and 30.30%. On the other hand, when compared to both SRAM cells, the RHBD cell's power SF and SS process are increased by 10.14% and 15.40%, respectively.

5.2 Area Comparison

The area of 12T RHBD and RHPD SRAM cells is compared in Table 5.1. The planned 12T cells are seen in figures 17 and 18. The size of transistors (P3, P4) in the RHBD cell is (2.0) times that of P1 and P2 transistors and area, as shown in Fig. 6. Access transistors (N7–N10) have dimensions of 140/45 nm, while RHPD (N1, N2, P1, and P2) and drive transistors (N3, N4, N5, and N6) have dimensions of 80/45 and 280 nm/45 nm, respectively. The 12T Dice cell's transistors are of the same size. Many of the We-Quatro cell's pull-down transistors (N5, N6, N7, and N8) are twice the size of all other transistors.

5.3 Stability Comparison

The primary measurement is used to determine the cell's stability is the SNM. The cell can withstand most significant DC voltage without interfering with the SNM output. The butterfly curve is the method for computing SNM that is most commonly employed. SNM is stimulated for 1V in both proposed SRAM cells, and Table 5.1 shows that the proposed 12T RHBD SRAM has a better HSNM than the We-Quatro and Dice cell and 12T RHPD SRAM due to larger P3, P4, and more extended feedback. The WSNM outperforms the We-Quatro but falls short of the Dice cell, which can be improved by increasing access transistor size. The read noise margin is determined by the strength of the pull-down and driver

transistors (RSNM). Because the proposed cell contains PMOS (P1 and P2), it produces less RSNM than other cells.

Based on simulation and analysis of the speed of the above four memory cells, power consumption, and SEU immune capabilities, the proposed RHBD-12T cell is more acceptable in general.

6 Conclusion

SRAM cells with excellent reliability and speed, such as the proposed RHBD and RHPD-12T. In terms of single-event upset prevention, circuit output at high frequency and low power supply voltage, the suggested SRAM cells outperform DICE and We-Quatro radiation-hardened memory cells. Based on the layout design, the 12T RHBD cell has a lower cell area than the 12T Dice, We-Quatro, and RHPD cells. The suggested 12T SRAM cell absorbs 51.56% less total power dissipation, 27.88% less static power dissipation, and 18.78% less static power dissipation than the 12T We-Quatro and 12T Dice cells. The write speed of the RHBD cell is 18.37%, which is 14.54% faster than the write speeds of the We-Quatro (12T), Dice (12T), and RHPD (12T). The RHBD cell's HSNM is increased by 32.96% and 77.56%, respectively, compared to We-Quatro and Dice. The RHBD cell's WSNM is enhanced by 11.6% and decreased by 12.7%, respectively, compared to the We-Quatro and Dice cells. In comparison to the We-Quatro and Dice cells, the proposed cell has a lower and similar RSNM. A 32X32 SRAM array with a 12T RHBD SRAM cell consumes 1.1 mV of power, 97.67% less than a 32X32 SRAM array with a 12T RHPD SRAM array, which consumes 3.2 mV at a supply voltage of 1V. As a result, the suggested SRAM cell provides a reasonable balance of strength, stability, delay, and area under high radiation circumstances at high frequencies, making it a desirable choice for aerospace applications.

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Conflicts of interest/Competing interests

The authors whose names are listed immediately certify that they have NO affiliations with or involvement in any organization or entity with any financial interest or non-financial interest in the subject matter or materials discussed in this manuscript.

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Not Applicable

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Not Applicable

Authors' contributions –

All authors are equally contributed

Ethics approval -

Agreed

Consent to participate –

Yes

Consent for publication -

Yes

DATA AVAILABILITY STATEMENT

Data sharing is not applicable to this article as no datasets were generated or analyzed during the current work.

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Figures

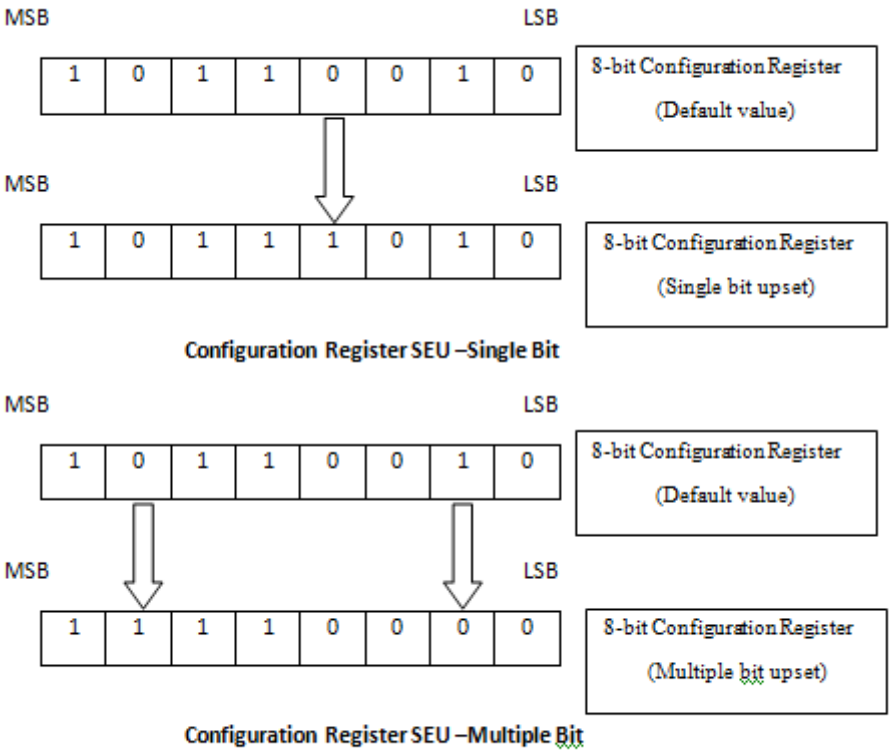

Figure 1

Single Event Upset

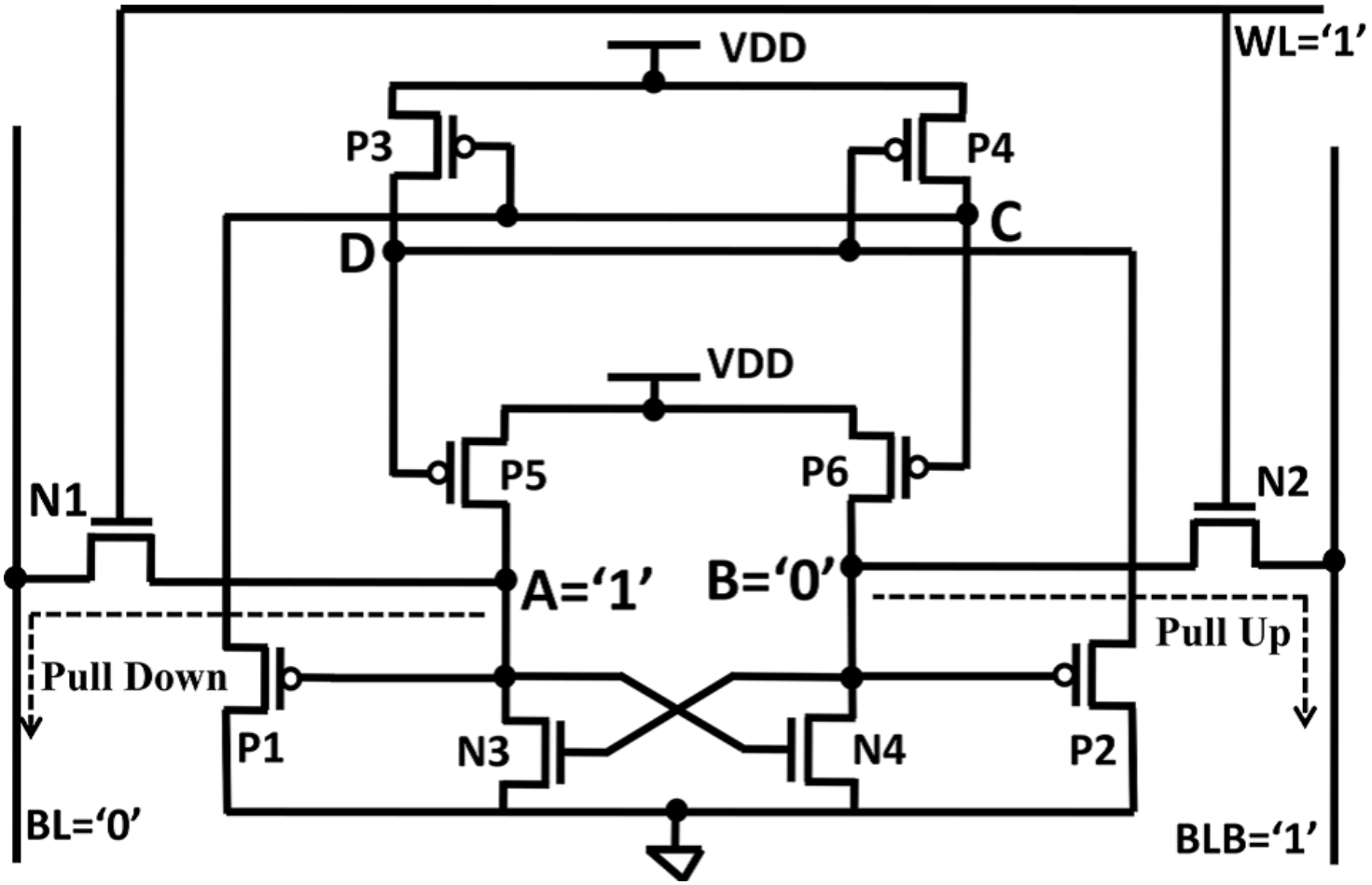

Figure 2

Schematic Diagram of 10T SRAM Cell

Figure 3

Simulation Response of 10T SRAM Cell

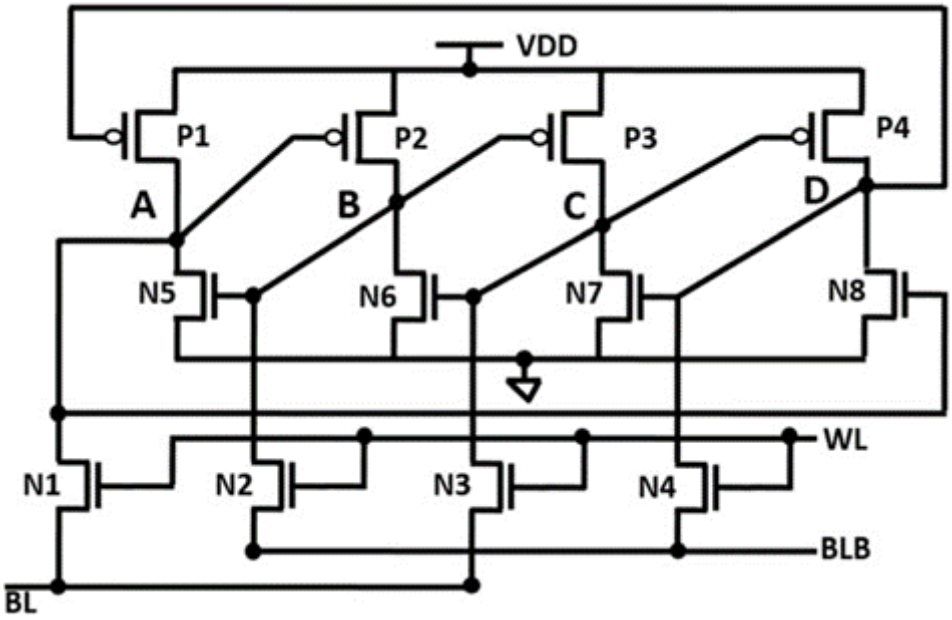

Figure 4

Schematic Diagram of DICE SRAM cell

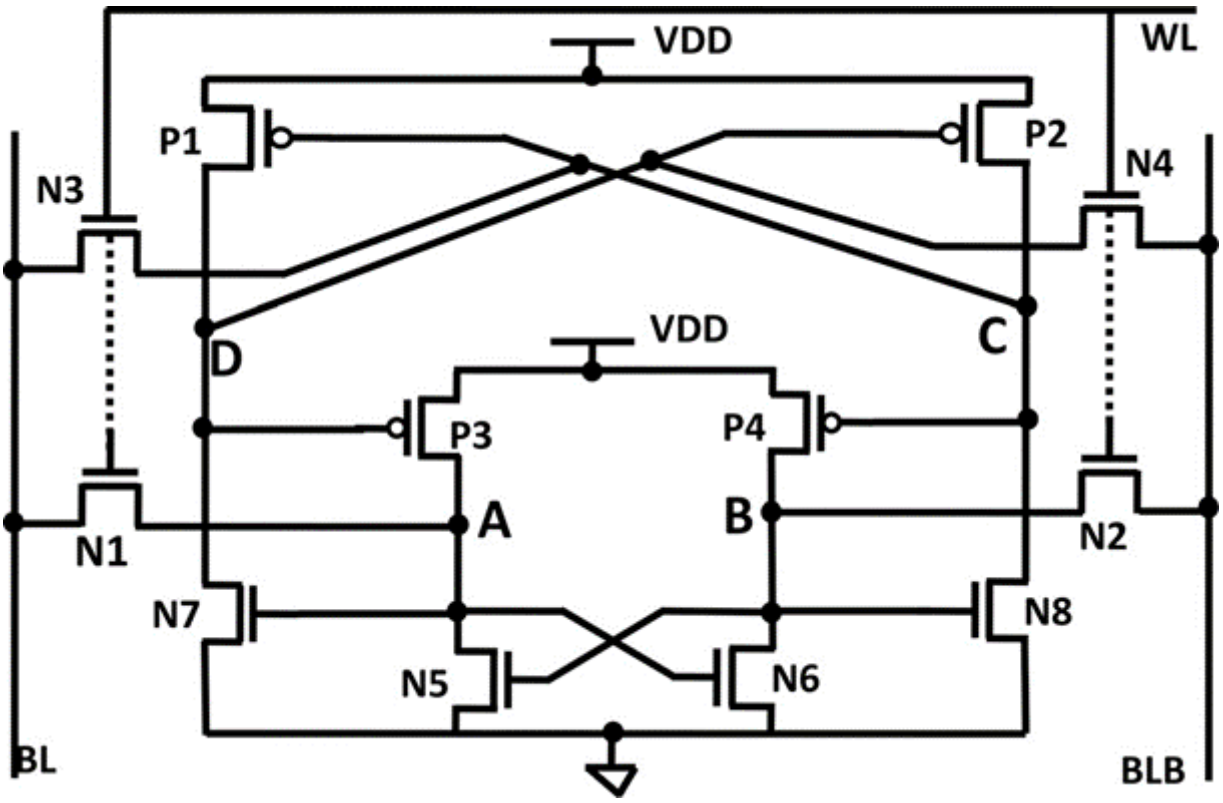

Figure 5

Schematic Diagram of WE-QUATRO SRAM cell

Figure 6

12T Representation of RHBD SRAM Cell

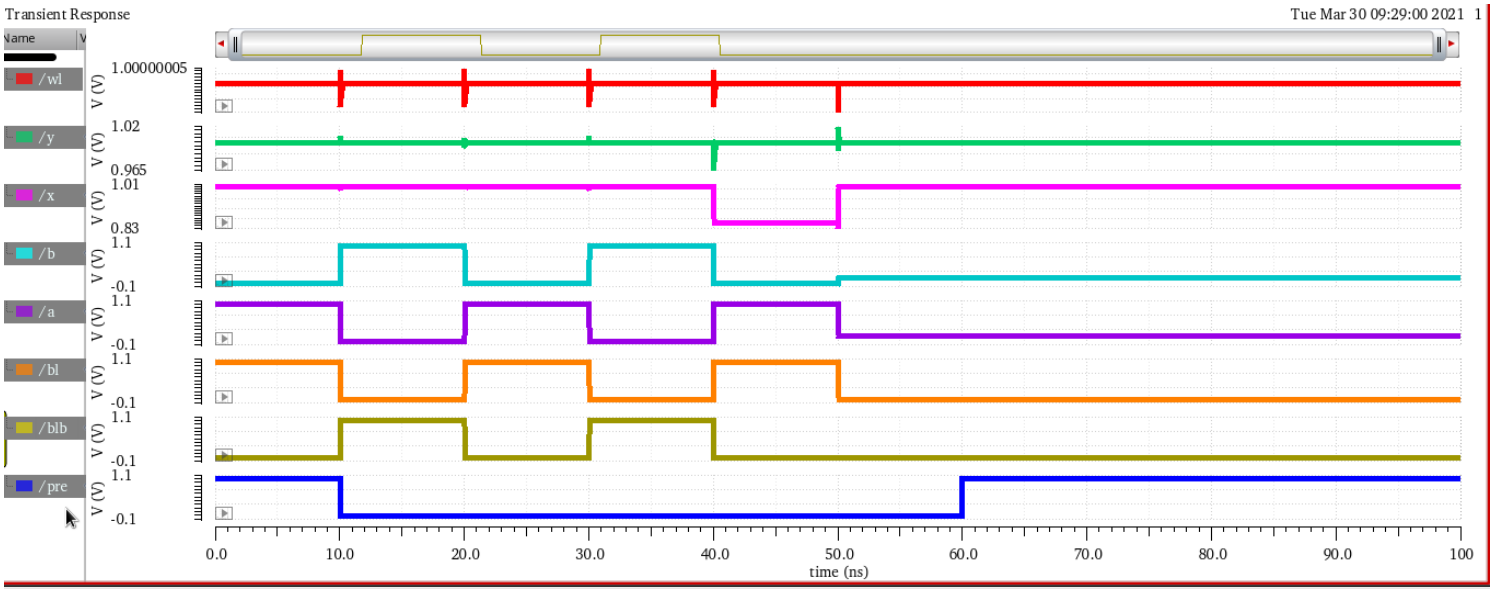

Figure 7

Transient response 12T RHBD SRAM Cell

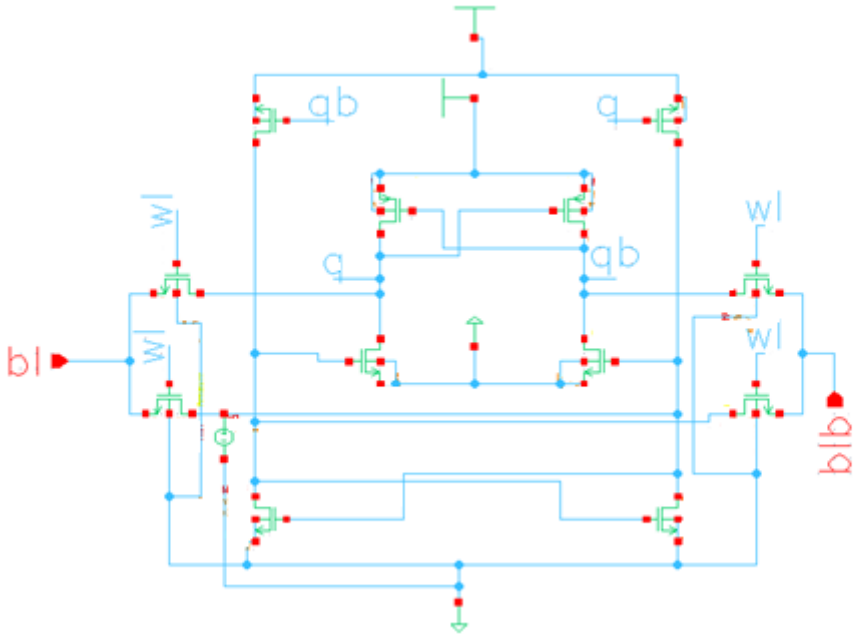

Figure 8

Schematic Diagram of RHPD-12T SRAM cell

Figure 9

Transient Response for 12T-RHPD SRAM Cell

Figure 10

Design of 32X32 SRAM Array

Figure 11

Representation of Address Decoder

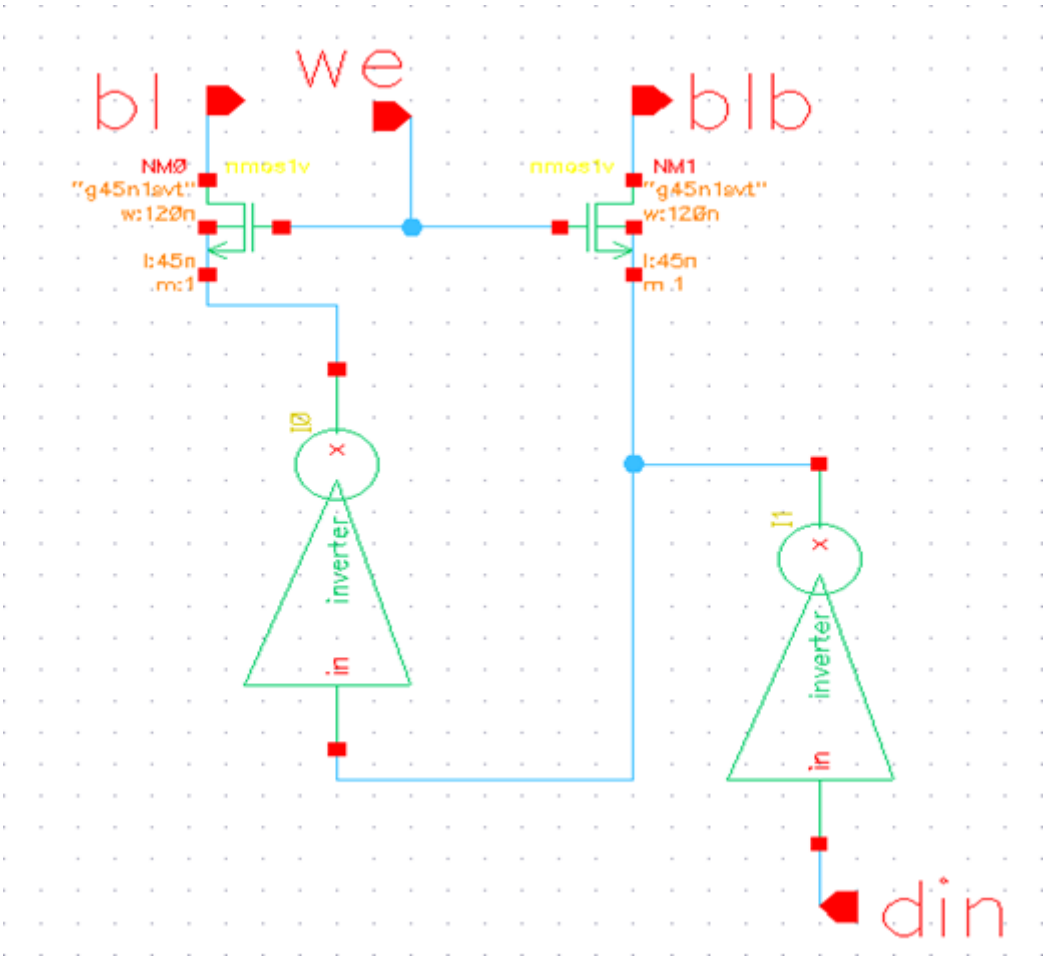

Figure 12

Schematic Diagram of Write Driver Circuit

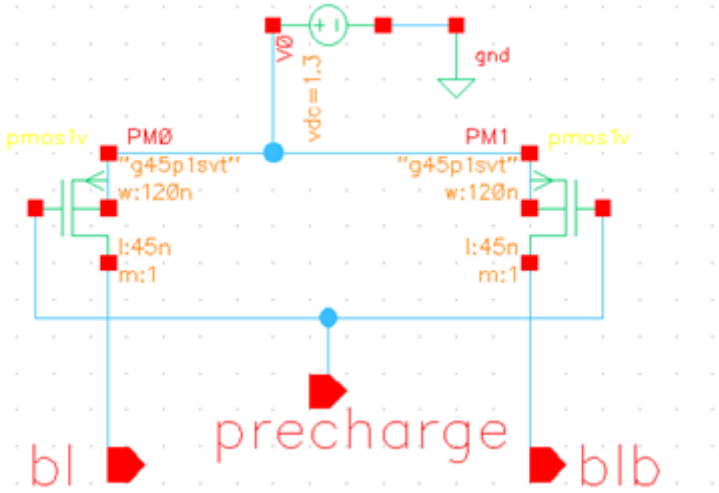

Figure 13

Schematic Diagram of Precharge Circuit

Figure 14

Schematic Diagram of CLSA

Figure 15

Schematic Diagram of SCSA

Figure 16

Process Corner Analysis of Proposed SRAM Cells

Figure 17

Layout for the 12T RHBD

Figure 18

RHPD SRAM Cells