Thermal-Aware Floorplanner for 3D IC, including TSVs, Liquid Microchannels and Thermal Domains Optimization

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Abstract

3D stacked technology has emerged as an effective mechanism to overcome physical limits and communication delays found in 2D integration. However, 3D technology also presents several drawbacks that prevent its smooth application. Two of the major concerns are heat reduction and power density distribution. In our work, we propose a novel 3D thermal-aware floorplanner that includes: (1) an effective thermal-aware process with 3 different evolutionary algorithms that aim to solve the soft computing problem of optimizing the placement of functional units and through silicon vias, as well as the smooth inclusion of active cooling systems and new design strategies,(2) an approximated thermal model inside the optimization loop, (3) an optimizer for active cooling (liquid channels), and (4) a novel technique based on air channel placement designed to isolate thermal domains have been also proposed. The experimental work is conducted for a realistic many-core single-chip architecture based on the Niagara design. Results show promising improvements of the thermal and reliability metrics, and also show optimal scaling capabilities to target future-trend many-core systems.

Keywords: 3D architecture, Thermal-aware floorplan, Air channels, Through silicon vias, Evolutionary algorithms

Glossary

AC Air Channel. 4, 14, 16–19, 26–28

DVFS Dynamic Voltage and Frequency Scaling. 2

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FU Functional Unit. 2–5, 9–15, 17–19, 21, 23, 25–28

IC Integrated Circuit. 2–5, 12, 14, 15, 27, 28

LC Liquid Channels. 3, 4, 14, 15, 17–19, 23, 24, 26–28

MFA Multi-objective Floorplanning Algorithm. 5, 6, 9–19, 21, 23, 24, 26–28

MOEA Multi-Objective Evolutionary Algorithm. 9–11

PCB Printed Circuit Board. 3, 8

RC Resistance-Capacitance. 7, 8

TSV Through Silicon Via. 2, 4, 5, 8, 9, 13–15, 17–19, 21, 23, 25, 28

1. Introduction

The process of continuous scaling over the past decades has led to important improvements in size and performance of electronic products, but it has also led to several challenges such as communication problems and temperature management.

The shift to the many-core architectures has been driven by the advances in semiconductor technologies. Besides, the increase in power dissipation has been tailored by dynamic techniques like Dynamic Voltage and Frequency Scaling (DVFS) [1], using several clock domains [2] or task migration policies [3]. These techniques, however, may also impact negatively the performance of the system. Design-time approaches like the one proposed in this paper are able to mitigate the effect of high temperatures and, also, are compatible with any other existing dynamic technique applied to maintain or even increase the performance of the system.

One important mechanism to overcome physical limits in Integrated Circuit (IC) design underlies on the design of multi-level ICs using advanced processes. These techniques boost the concept of three dimensional integrated circuits (3D ICs). 3D designs improve the performance of the system by reducing interconnect delays and increasing the density of the logic. Through Silicon Vias (TSVs) connect multiple layers of the stack reducing distances between Functional Units (FUs), hence decreasing the communication delay.

This fabrication technology also allows the integration of multiple and disparate technologies, such as radio frequency and mixed signal components, with traditional computing technologies.

However, 3D integration exacerbates the problem of temperature in the chip, specially temperature in inner layers. These thermal problems are increasingly affecting the performance and the reliability of electronic systems. [4] reported that over 50% of electronic product failures are caused by thermal issues and the presence of hotspots. Increasing the temperature decreases lifetime of the chip exponentially. Furthermore, higher temperature can cause slower devices, can increase leakage current, and can reduce the performance due to the impact in the metal resistivity.

Considering these facts, it is desired to keep the components and the chip structure as cool as possible for maximum reliability. However, the absolute temperature of the chip is not the only factor that affects performance; moreover, the thermal gradients that appear on the chip surface degrade the system reliability through the promotion of dangerous electro-migrations [5].

One way in which hardware designers have tried to address the thermal problem is with the use of thermal-aware floorplanners such as [6] (that proposed a thermal-driven floorplanning algorithm for 3D ICs) or [7] (where the authors implemented a multi-objective floorplanning algorithm for 2D and 3D ICs, combining linear programming and simulated annealing). Some other authors have also considered the placement of thermal vias in these 3D stacks to optimize the thermal profile of ICs [8]. The careful placement of active modules in a 3D stack can optimize the wire length that connects FUs by reducing the communication delays, and can also provide a homogeneous temperature distribution across the chip. Apart from static approaches of thermal optimization, dynamic techniques are required to manage the high power densities found in these architectures. While the conventional air cooling has proved to be insufficient for 3D-ICs, the interlayer micro-channel liquid cooling provides a better option to address this problem. Some works like [9] and [10] have focused in thermal modeling with active cooling. These works have studied the effect of allocating liquid channels between active layers and their cooling effect.

Some of the goals in the design of 3D stacks are to achieve a reduction in area and also to decrease the length of the interconnections, that would be translated into improved data transfer times and power consumption. Figure 1 summarizes our proposed concept of a 3D-IC architecture. Based on [11], the 3D stack is built over a Printed Circuit Board (PCB), which is considered to be adiabatic. Then, several layers are stacked, as can be seen in Figure 1. Every layer of the stack is composed of silicon and silicon dioxide. Liquid Channelss (LCs) is used as an active cooling system. These channels are placed in the silicon dioxide just over the active layers. Liquid channels absorb heat produced by FUs with a high power density, reducing



Figure 1: 3D architectural concept

the temperature of inner layers. LCs contain a coolant (generally water) that is pumped into the chip. In this paper we also propose a novel architectural set-up based on isolation channels or Air Channels (ACs). Air channels are etched in silicon and filled with low pressure air. Since heat spread is mainly diffusive, air channels prevent cold areas to be affected by the power dissipated in other regions of the chip, creating temperature domains or regions. The use of air channels has the major purpose of isolating thermal regions. This could seem counter intuitive as the heat flow from hotter modules could not be dissipated by the cooler ones. However, the idea behind this is the optimization of the active cooling mechanism (liquid channels), whose placement, number and required cooling energy are benefited by the air channels. More in detail:

- Since the chip is split in several independent regions, the thermal distribution of every domain can be defined attending to design constraints. In this way, it is easier to obtain a homogeneous distribution, or a pattern of alternate warm and cold regions, that help on achieving a more controlled thermal profile in the design phase.
- If high temperatures are located in certain regions, dissipation mechanisms can be applied in those areas where the thermal problems are exacerbated, minimizing technological costs and optimizing the cooling properties of the different techniques.

All this architectural diversity encourages the research on the design of optimization algorithms to place automatically FUs, TSVs, as well as liquid and air channels, minimizing maximum temperature and total wire length. The efficient management of all these input variables, and the multiple optimization criteria given by several objectives that have to be accomplished at the same time, requires innovative algorithms capable of evaluating all these parameters and returning the best set of solutions. In the case of 3D IC design, incremental optimization is a promising way to handle multi-objective optimization with complicated

Functional Units	Air Channels	TSVs	Liquid Channels
Input: Processors, memories, crossbars, set of connections between components, max. chip dimensions, etc. Algorithms: MFAFU or MFAFU	Possible inputs: Processors, memories, crossbars, set of connections between components, max. chip dimensions, etc. MFAFU output MFAFU output Algorithm: MFAac	Possible inputs: • MFAFU output • MFAFU output • MFAAC output • Any feasible design Algorithm: • MFATSV	Possible inputs: • Any feasible design • MFAFU output • MFAFU* output • MFAAC output • MFATSV output Algorithm: • MFALC

Figure 2: 3D design flow

constraints and to facilitate the design reuse technology. Many works have been published with this approach, however, none took into account thermal-aware floorplanning. Most multi-objective floorplanning algorithms in the literature are developed using Genetic Algorithms or Simulated Annealing, where the main problem relies on the formulation of the representation. Common representations for the floorplanning problem are polish notation [12], combined bucket array [6] and O-tree [13]. Most of these representations do not perform well in our scenario because they were initially developed to reduce area, whereas our problem is based on minimizing temperature. To this end, we extend in this paper our previous algorithm for floorplanning optimization named Multi-objective Floorplanning Algorithm (MFA) [14], in which we formulated a multi-objective optimization problem for 3D thermal aware floorplanning that is able to reduce peak temperature, eliminate hotspots, and hence decrease reliability risks related to temperature. MFA allows the incremental placement of FUs and TSVs.

In this paper, we will denote this algorithm with MFA_{FU}. From our previous work in [14], as Figure 2 introduces, we have enhanced the TSVs placement developing the new MFA_{FU*} that slightly extends MFA_{FU} to obtain solutions where at least one TSV configuration can be reached. We have also developed two new evolutionary algorithms. These algorithms solve the integration of active cooling systems within the 3D IC using liquid channels by optimizing their placement in those areas where the temperature is higher. The second new algorithm can manage the optimization of FU and TSV in the 3D IC design with air channels, taking into account new placement restrictions in the model. Results show that the inclusion of isolation channels creates temperature regions, decreasing the energy overhead imposed by the active cooling system.

This paper makes major contributions in the area of thermal optimization in 3D-integrated circuits. As compared with previous approaches, the work presented here achieves a practical and effective solution in the field of interest, outperforming the results obtained by these works. This paper also extends our previous

work presented in [14] with the following major upgrades:

- The proposal of a novel structure, called air isolation channels, as an effective mechanism for thermal isolation in 3D chips.
- The development of the required thermal models for these structures that enable their control by the optimization algorithm.
- The extension of the MFA algorithm presented in [14] with two new evolutionary algorithms, to consider the new design constraints and technologies, achieving better results in terms of thermal profile and fabrication costs.

The rest of the paper is structured as follows: Section 2 describes both the thermal model and current implementation of MFA. Then, Section 3 continues with an explanation of the proposed optimizer. The experimental set-up used for our scenario is then described in Section 4 and finally, results and conclusions are presented in Sections 5 and 6, respectively.

2. Thermal model

The equation governing heat diffusion via thermal conduction in a 3D stack is [15]:

$$\rho c \frac{\partial T\left(\vec{r},t\right)}{\partial t} = \nabla \left(k(\vec{r})\nabla T(\vec{r},t)\right) + p(\vec{r},t)$$
(1)

subject to the boundary condition

$$k(\vec{r},t)\frac{\partial T(\vec{r},t)}{\partial n_i} + h_i T(\vec{r},t) = f_i(\vec{r},t)$$
(2)

Regarding Equation 1, ρ is the material density, c is the mass heat capacity, $T(\vec{r}, t)$ and $k(\vec{r})$ are the temperature and thermal conductivity of the material at position \vec{r} and time t, and $p(\vec{r}, t)$ is the power density of the heat source. With respect to Equation 2, n_i is the outward direction normal to the boundary surface i, h_i is the heat transfer coefficient and f_i is an arbitrary function at the surface i.

Numerical thermal analysis can be accomplished by applying a seven points finite difference discretization method to Equation 1, which decomposes the 3D stack into numerous rectangular parallelepipeds of non-uniform sizes and shapes if necessary. In this way, each element has a power dissipation, temperature, thermal capacitance and thermal resistance to adjacent elements, which interact via heat diffusion. The discretized equation at an inner point of a grid element is:

$$\rho c V \frac{T_{i,j,l}^{q+1} - T_{i,j,l}^{q}}{\Delta t} = -2(R_{x} + R_{y} + R_{z})T_{i,j,l}^{q} + R_{x}T_{i-1,j,l}^{q} + R_{x}T_{i+1,j,l}^{q} + R_{y}T_{i,j-1,l}^{q} + R_{y}T_{i,j+1,l}^{q} + R_{z}T_{i,j,l-1}^{q} + R_{z}T_{i,j-1}^{q} + R_{z}T_{i,j-1}^{q} + R_{z}T_{i,j-1}^{q} + R_{z}T_{i,j-1}^{q} + R_{z}T_{i,j-1}^{q} + R_{z}T_{i,j-1}^{q} + R_{z}T_{i,j-$$

where *i*, *j* and *l* are discrete offsets along the *x*, *y* and *z* axes, Δt is the discretization step in time *t*, Δx , Δy and Δz are discretization steps along the *x*, *y* and *z* axes, and $V = \Delta x \Delta y \Delta z$. Finally, R_x , R_y and R_z are the thermal conductivities between adjacent elements, defined as follows: $R_x = k \frac{\Delta y \Delta z}{\Delta x}$, $R_y = k \frac{\Delta x \Delta y}{\Delta y}$, and $R_z = k \frac{\Delta x \Delta y}{\Delta z}$.

For a 3D stack with N discretized elements, equation 3 can be summarized as follows:

$$\mathbf{C}\frac{dT(t)}{dt} + \mathbf{R}T(t) = Pu(t) \tag{4}$$

where the thermal capacitance matrix **C** is an $N \times N$ diagonal matrix, the thermal conductivity matrix **R** is an $N \times N$ sparse matrix, T(t) and P are $N \times 1$ temperature and power vectors, and u(t) is the unit step function.



Figure 3: Material cells: (a) Diffusive cell (silicon, silicon dioxide, air) and (b) Liquid cell.

Equation (4) can be characterized by a 3D Resistance-Capacitance (RC) model as the one presented in [16]. Voltage differences are analogous to temperature differences, and the electrical resistance is analogous to thermal resistance. The thermal modeling of the stack in Figure 1 can be performed splitting the chip into small cubic unitary cells.

295 W/(mK)
-0.491 W/(mK ²)
1.38 W/(mK)
1.628 x 10 ⁶ J/m ³ K
4.180 x 10 ⁶ J/m ³ K
1.73 x 10 ⁶ J/m ³ K
0.03 W/(mK)
372 W/(mK)
3.45 x 10 ⁶ J/m ³ K
2.4 x 10 ⁻ 3 W/(mK)
$1 \ge 10^4 \text{ J/}m^3 \text{K}$
4.184 x 10 ⁶ J/m ³ K
0.58 W/(mK)

Table 1: Thermal properties of materials.

Silicon and silicon dioxide cells are modeled with six thermal resistances and one thermal capacitance as it can be seen in Figure 3(a). Four of these resistances connect each cell to its lateral neighbors (those on the same layer), while the two remaining resistances connect the cell with the upper and bottom cell, respectively. The capacitance represents the heat storage inside the cell.

Air channels also have a diffusive behavior. Despite the fact air is a fluid, the dimensions of the cavity and the absence of forced convection methods, make the fluid to behave as a diffusive material. We have considered channels fabricated and filled with low pressure air, which decreases thermal conductivity, making isolation much more efficient.

Liquid channels are electrically modeled as it can be seen in Figure 3(b). This difference with the diffusive cell comes because, in cells circulating a coolant, the mechanism that dominates the heat transfer is the forced convection. This mechanism can be translated into our RC model using two voltage controlled current sources, as it is profusely covered in [17].

Heat diffusion to the surrounding environment is also considered by the RC model. This diffusion occurs in the edge of the chip and in the top layer. Different chip packages and heat sinks can be integrated in Equation (4) by tuning the capacitance and resistance parameters of the model. As the PCB base is considered to be adiabatic, no heat transfer occurs in the bottom direction of the first layer.

The interface material that exists in between two silicon layers, used as a glue, is modeled as an epoxy layer, a pure resistant material. The existence of TSVs is considered in the model, also as a resistance element.

All these cell types are integrated in Equation (4), which is solved using an iterative method (Forward

Stack width	12000 µm
Stack length	10500 µm
Cell size (lxw)	300x300 µm
TSV cell size (lxw)	300x300 µm
Liquid channel width	300 µm
SiO ₂ height	50 µm
Si height	150 μm
Epoxy height	25 µm

Table 2: Geometric properties of the stack.

Euler) to validate the results given by our 3D floorplanner. The main thermal properties of the material and dimensions used in the model are listed in Table 1 and 2.

3. Design Flow: Multi-objective Floorplanning Algorithm

MFA was first proposed by David Cuesta *et al.* [14]. This algorithm performs an incremental floorplanning divided in two phases. First, FUs are placed by running MFA_{FU}. Secondly, MFA_{TSV} is executed, placing TSVs. These two processes are independent. Thus, MFA_{FU} tends to obtain floorplans where the insertion of TSVs is not possible. In this section we describe all the algorithms implied in the design flow shown in Figure 2, including these two sub-algorithms for self-content purposes. We also improve MFA_{FU} to reach feasible solutions for the insertion of TSVs.

3.1. MFA_{FU}

MFA_{FU} is a Multi-Objective Evolutionary Algorithm (MOEA) based on NSGA-II [18]. The foorplanner manages coded solutions that are gradually improved in the evolutionary process to provide configurations optimized both in performance and thermal response for the target architecture. To this end, MFA_{FU} simultaneously minimizes the following three objectives:

- *F*₁: Number of topological constraints violated (overlapping between different blocks, or components out of the borders of the chip).
- F_2 : Wire length, approximated as the Manhattan distance between interconnected blocks C:

$$F_2 = \sum_{i,j \in \mathbb{C}: i < j} |x_i - x_j| + |y_i - y_j| + |z_i - z_j|$$
(5)

, where (x_i, y_i, z_j) are the coordinates of FU *i*.

• F_3 : Maximum temperature of the chip. The computation of this objective depends on the chosen thermal model. In the case of MFA_{FU}, the contribution to the maximum temperature of two FUs *i*, *j* is simplified as the cross product of their power densities p_i , p_j divided by the corresponding euclidean distance. Thus, having *n* FUs, F_3 is defined as:

$$F_3 = \sum_{i < j \in 1...n} \frac{p_i \cdot p_j}{\sqrt{(x_i - x_j)^2 + (y_i - y_j)^2 + (z_i - z_j)^2}}$$
(6)

By minimizing F_3 the algorithm will try to place hottest blocks as far as possible. This process reduces maximum temperature, as it is demonstrated in [14].

 MFA_{FU} can be classified as a hybrid foorplanning approach because the decoding heuristic implements an incremental foorplanning inspired in constructive techniques, while the MOEA on top of the heuristic is essentially iterative.



Figure 4: MFA_{FU} A chromosome representing a solution of a platform with 4 cores, C_i , and 4 memories, M_i , (a), as well as crossover operation (b) and the two ways of mutation operator; swapping (up) and rotation of a FU (down) (c) operators.

We use a permutation encoding [19], in which every chromosome is a string of records representing the different FUs of the target architecture. These records gather information relative to a FU, namely label, width, and length. Managing the width and length of the blocks allows to perform rotations, granting further degrees of freedom to the optimization process. Additional characteristics of the FUs such as power densities, connections, etc., must be managed by the algorithm. However, this information does not need to be codified in the chromosomes as it is common to all the individuals. Figure 4(a) depicts the representation of a chromosome used in MFA_{FU}. The example shows a candidate solution (individual) of a platform composed of 8 FUs: 4 cores $C_i(i = 1, 2, 3, 4)$ and 4 memories $M_i(i = 1, 2, 3, 4)$. The order $C_3, M_2, M_4, C_1, M_1, C_4, M_3, C_2$ determines the placement sequence. Thus, C_3 will be placed first, followed by M_2, M_4 and so on.

All the chromosomes must have size n, where n is the number of FUs to be placed. Therefore, the cardinality of the considered solution space is n!. The operators designed according to the representation are depicted in Figure 4 and briefly described below:

- *Selection:* The selection operator implements a binary tournament strategy. To this end, random couples of individuals are formed and the best solution of each pair is selected for crossover.
- *Crossover:* A cycle crossover is used to produce the offspring, this operator must take into account that all the components must appear once and only once in the chromosome (see Figure 4(b)).
- *Mutation:* The mutation of the solutions is performed in two ways. The first one consists in swapping the position of two blocks in the chromosome, resulting in a change of the placement sequence of the mutated individual. The effect of the second is the rotation of a FU (see Figure 4(c)).

Algorithm 1 shows the implementation of MFA_{FU}. As Figure 2 indicates, the initial population is built from a list of components to be placed in the floorplan, along with their dimensions and interconnectivity. Each chromosome is defined just as a random sequence of these components (see Figure 4(a)). A heuristic is in charge of the placement of the different elements of the architecture (decoding of the solutions). The heuristic performs an incremental floorplanning in which the components are sequentially placed in the 3D stack following the order implied by the solution encoding. In fact, as the exhaustive heuristic alone is capable of obtaining well performing solutions, the MOEA is designed to obtain the optimal order of the components given the placement heuristic. In this heuristic, every block *i* is placed considering all the topological constraints, the wire length, and the maximum temperature of the chip with respect to all the previously placed blocks j : j < i, named as (F_1^i, F_2^i, F_3^i) . The best location for each block is selected depending on whether the block is a relative heat sink or a heat source. For a heat source (like a core, for example) the best position is the one with lowest F_3^i to ensure an even thermal distribution. If the block is a heat sink (like a memory) the best position is the one with lowest wire length F_2^i . With this procedure, the Algorithm 1 MFA_{FU}

Require: G is the number of generations. N is the population size. function main() $P = \text{initialize}() \{P \text{ is the first random population}\}$ evaluate(*P*) {*P* is evaluated} for g = 1 to G do $\hat{P} = \emptyset$ {New empty population} for n = 1 to N/2 do $\hat{P}_s = \text{select}(P)$ {Select two individuals,} $\hat{P}_c = \text{crossover}(\hat{P}_s) \{\text{perform crossover } \dots\}$ \hat{P}_m = mutation(\hat{P}_c) {and mutation} $\hat{P} = \hat{P} \cup \hat{P_m}$ end for $evaluate(\hat{P})$ $P = P \cup \hat{P}$ reduce(P) {Standard NSGA-II reduction mechanism} end for function evaluate(P) for all $I \in P$ do for i = 1 to n do $B_i \leftarrow I_i$ {The i-th gene in individual $I(I_i)$ represents the i-th block/functional unit (B_i) to be placed in the current 3D candidate design} $f_i^* \leftarrow \infty, x_i^* \leftarrow 0, y_i^* \leftarrow 0, z_i^* \leftarrow 0$ $\{0 \le l_i \le L, 0 \le w_i \le W \text{ and } 0 \le h_i \le H \text{ are the length, width and height of block } i, respectively}\}$ for all $(x_i \in [0..L - l_i], y_i \in [0..W - w_i], z_i \in [0..H - h_i])$ do $F_1^i \leftarrow$ checkTopologyConstraints(x_i, y_i, z_i, i) {Number of topology constraints violated with the previous i-1 blocks already placed} if $F_1^i = 0$ then $\dot{F}_2^i \leftarrow \text{manhattan}(x_i, y_i, z_i, i)$ {This function computes wire length according to Manhattan distances between connected blocks in the range [1..*i*]} $F_{2}^{i} \leftarrow \text{computeTemp}(x_{i}, y_{i}, z_{i}, i) \{\text{Compute (6) with } i < j \in 1..i\}$ $\mathbf{if}^{'}B_{i}$ is a core then $f_i \leftarrow F_3^i$ else $f_i \leftarrow F_2^i$ end if if $f_i < f_i^*$ then $\begin{array}{c} f_i^* \leftarrow f_i \\ x_i^* \leftarrow x_i, y_i^* \leftarrow y_i, z_i^* \leftarrow z_i \end{array}$ end if end if end for $B_i \leftarrow (x_i^*, y_i^*, z_i^*)$ {Assign best coordinates to each block} end for $F_1 \leftarrow$ checkTopologyConstraints() {Number of topology constraints violated in the current 3D IC} $F_2 \leftarrow \text{manhattan}() \{\text{Total wire length}\}$ $F_3 \leftarrow \text{computeTemp}() \{\text{Compute (6)}\}$ $I \leftarrow (F_1, F_2, F_3)$ {Assign multi-objective values to each individual} end for

authors try to ensure a correct thermal optimization. This approach is highly reasonable in terms of thermal profile, since large 3D stacks with more than 48 cores reach prohibitive temperatures (more than 400 K, as can be seen in [14]). Thus, every block is fixed in the remaining position (x_i, y_i, z_i) . Once the placement

has finalized, the obtained configuration is evaluated according to the three defined objectives (F_1, F_2, F_3) . In order to help the algorithm to find feasible solutions, the multiobjective function can be transformed to $(F_1, (1 + F_1) \cdot F_2, (1 + F_1) \cdot F_3)$. Although the first objective can be removed in this case, we keep it to easly check if the algorithm is not able to find feasible solutions.

3.2. TSV Optimization: MFA_{TSV}

As aforementioned, this algorithm is responsible of the placement of TSVs to allow vertical communications. As in MFA_{FU}, MFA_{TSV} is based on NSGA-II. In the original version of MFA, this algorithm is the step executed immediately after MFA_{FU}. Since TSVs insertion is not checked in the first algorithm, it could happen that MFA_{TSV} did not find a feasible distribution of TSVs. To solve this issue, we improve MFA_{FU} in the next subsection. In the following, we describe the MFA_{TSV} algorithm.

Technologically, and due to fabrication process constraints, TSVs can only be built from one specific layer to any other. In this regard, MFA_{TSV} considers the top layer as the initial one.



Figure 5: TSV Chromosome description.

To encode a solution, MFA_{TSV} examines the remaining free cells in the MFA_{FU} resultant stack. Then, MFA_{TSV} builds an array of x-y coordinates where TSVs can be drilled, as the array of coordinates in Figure 5 shows. Given a 3D IC with *N* layers, a first region of this array contains the coordinates where a TSVs between layers *Top* and 1 can be built; a second region in the same array contains the coordinates where TSVs between layers *Top* and 2 can be built, and so forth. Next, a 0-1 chromosome of length equal to the array of coordinates is created. If a gene contains a 1, a TSV is inserted in the corresponding (x,y) position, between the layers that belong to the corresponding region. In this way, Figure 5 encodes 7 TSVs in four layers (N = 4): 1 TSV drilled between layers 4 and 1, 2 TSVs between layers 4 and 2, and 4 TSVs between layers 4 and 3. As a result, the initial population is a set of binary chromosomes randomly generated. The corresponding (x,y) coordinates are stored in a separate array of coordinates.

Algorithm 2 MFA_{TSV}

Require: *I* is the current individual to be evaluated (see Figure 5). *C* is the set of connections in the floorplan. function evaluate(I) $F_4 \leftarrow \sum_{i=1..N} I_i$ {Number of TSVs.} $F_5 \leftarrow \overline{0}$ for all $(B_i, B_j) \in C$ do $dz \leftarrow |z_i - z_j|$ if dz = 0 then $d \leftarrow \text{manhattan}(x_i, y_i, x_j, y_i)$ {Manhattan distance between blocks *i* and *j*} $F_5 \leftarrow F_5 + d$ else $d \leftarrow \text{findBestTsv}(I, i, j)$ {This functions takes all the candidate TSVs in I and compute the Manhattan distance in the path block $i \rightarrow \text{TSV} \rightarrow \text{block } j$. At the end, it returns the best distance} $F_5 \leftarrow F_5 + d$ end if end for $I \leftarrow (F_4, F_5)$ {Assign multi-objective values to this individual}

Algorithm 2 shows a pseudocode for MFA_{TSV}. This algorithm returns a set of solutions, considering the number of TSVs F_4 and the new total wire length F_5 . This set constitutes a Pareto front approximation, and the designer will have the chance to select the best solution in terms of economic cost and wire length reduction, considering that a minimum number of TSVs must be included in the design in order to fulfill the communication constraints. The minimum number of TSVs is calculated attending to the communication bandwidth needs of cores. We have calculated the data that is transferred by an FM modulation/demodulation application as the one explained in [3]. The minimum number of TSVs is given by the technological parameters of the TSVs and the volume of data to transfer [20].

3.3. MFA_{FU*}

In this Section, we slightly modify MFA_{FU} to obtain solutions where at least one TSV configuration can be reached by MFA_{TSV}. To this end, we present Algorithm 3. We only show the evaluation function because the main function is identical to MFA_{FU}. The modification is performed including the *R* matrix. *R* contains all the free cells in the 3D stack. Thus, given a floorplan, it is quite easy to check if a TSV can be drilled to connect two blocks placed at different layers. If this is not possible, F_2^i is set to infinity.

In the following subsections we present two new subalgorithms of MFA, named MFA_{LC} and MFA_{AC} . MFA_{LC} has been developed to place liquid channels in the 3D IC. MFA_{AC} has been designed to divide the 3D stack into regions isolated by air channels. It is worth noting that the following two algorithms receive as input the resultant 3D IC obtained either by MFA_{FU} or $MFA_{FU*}+MFA_{TSV}$, as Figure 2 shows.

Algorithm 3 MFA_{FU*}

Require: G is the number of generations. N is the population size. **function** evaluate(*P*) for all $I \in P$ do $R \leftarrow 1$ {Matrix $L \times W \times H$ with free cells in the 3D-IC, i.e., where FUs can be placed} for i = 1 to n do $B_i \leftarrow I_i$ {The i-th gene in individual $I(I_i)$ represents the i-th block (B_i) to be placed in the current 3D candidate design} $f_i^* \leftarrow \infty, \, x_i^* \leftarrow 0, y_i^* \leftarrow 0, z_i^* \leftarrow 0$ for all $(x_i \in [0..L - l_i], y_i \in [0..W - w_i], z_i \in [0..H - h_i])$ do $F_1^i \leftarrow$ checkTopologyConstraints (x_i, y_i, z_i, i) {Number of topology constraints violated with the previous i-1 blocks already placed} if $F_1^i = 0$ then $F_2^i \leftarrow \text{manhattan}(x_i, y_i, z_i, i, R)$ {This function computes wire length according to Manhattan distances between connected blocks in the range [1..i]. It also asserts that a TSV can be created if two blocks are placed on different layers (it is easily computed using R)} $F_3^i \leftarrow \text{computeTemp}(x_i, y_i, z_i, i) \{\text{Compute (6) with } i < j \in 1..i\}$ if B_i is a core then $f_i \leftarrow F_3^i$ else $f_i \leftarrow F_2^i$ end if if $f_i < f_i^*$ then $\begin{array}{c} f_i^* \leftarrow f_i \\ x_i^* \leftarrow x_i, y_i^* \leftarrow y_i, z_i^* \leftarrow z_i \end{array}$ end if end if end for $B_i \leftarrow (x_i^*, y_i^*, z_i^*)$ {Assign best coordinates to each block} update (\hat{R}, B_i) end for $F_1 \leftarrow$ checkTopologyConstraints() {Number of topology constraints violated in the current 3D IC} $F_2 \leftarrow \text{manhattan}()$ {Total wire length} $F_3 \leftarrow \text{computeTemp}() \{\text{Compute (6)}\}$ $I \leftarrow (F_1, F_2, F_3)$ {Assign multi-objective values to each individual} end for

3.4. Liquid Channel Optimization: MFALC

Once the 3D IC has been thermally optimized placing FUs or TSVs, we run our accurate thermal model in Equation (4) to evaluate the temperatures in the chip, computing the temperature matrix T. TSVs have been already incorporated into this equation as a set of cells disposed vertically in the 3D IC. The temperature values and the floorplan information are the inputs to our proposed liquid channel optimizer, shown in Algorithm 4.

Since liquid channels are placed right above FUs, the only topological constraint is the possible collision between liquid channels and TSVs. As was done for the placement of TSVs, a set of available (x, z) coordinates is built. The initial population is also a random set of binary chromosomes indicating the presence or not of a liquid channel at a given position. The evaluation function of MFA_{LC} takes into account the



Figure 6: Regression for evaluation function in liquid channels optimization

cooling effect of a liquid channel. In order to evaluate this cooling effect, several thermal simulations were conducted. Liquid channels are able to reduce temperature not only in the active cells under the channel, but also in their neighbors. This reduction follows a logarithmic tendency with the chip temperature that can be seen in Figure 6. Introducing these data in the evaluation of our proposed evolutionary algorithm, we can find optimized solutions.

The optimization of the number of microchannels in the design is a major constraint from the point of view of technological and operating costs. Adding liquid microchannels in the design implies not only fabrication costs but also additional energy for the pumping system, as shown in [21].

3.5. Air Isolation Placement Optimization: MFA_{AC}

Our proposal of creating thermal domains in a chip is a revolutionary method to keep heat concentrated in certain areas preventing, with air isolation channels, heat spread from hot to cold regions. If this design technique is combined with the deployment of liquid channels, better results in terms of energy saving and fabrication cost are obtained.

Since the thermal conductivity of air is lower than the silicon, the channels can create thermal domains isolating regions with high temperatures from other areas of the 3D stack. With this set up a more homogeneous thermal distribution is obtained with a reduced investment in any other active cooling mechanisms.

Algorithm 4 MFA_{LC}

Require: *I* is the current individual to be evaluated. *T* is the set of temperatures obtained with the thermal model.

function evaluate(I) $F_6 \leftarrow \sum_{i=1..N} I_i$ {Number of liquid channels.} $F_7 \leftarrow 0$ $\hat{T} \leftarrow T$ for all $I_i \in I$ do if $I_i = 1$ then $(x_i, z_i) \leftarrow I_i$ {Every gene is referred to a concrete (x_i, z_i) , where z_i is the current layer for the i-th channel and x_i its x coordinate} for $y_i = 0$ to W - 1 do $\hat{T}(x_i, y_i, z_i) = 342.46 ln(\hat{T}(x_i, y_i, z_i)) - 1664.4$ $\hat{T}(x_i - 1, y_i, z_i) = 321.28 ln(\hat{T}(x_i - 1, y_i, z_i)) - 1541.5$ $\hat{T}(x_i - 2, y_i, z_i) = 293.60 ln(\hat{T}(x_i - 2, y_i, z_i)) - 1380.8$ $\hat{T}(x_i+1,y_i,z_i) = 321.28 ln(\hat{T}(x_i+1,y_i,z_i)) - 1541.5$ $\hat{T}(x_i + 2, y_i, z_i) = 293.60 ln(\hat{T}(x_i + 2, y_i, z_i)) - 1380.8$ end for end if end for $F_7 = \sum_{x_i,y_i,z_i} \hat{T}((x_i,y_i,z_i))$ $I \leftarrow (F_6, F_7)$ {Assign multi-objective values to this individual}

The creation of thermal domains implies a reduction in the number of liquid microchannels and consequently a reduction in fabrication and working costs.

When the chip is isolated by air channels, the optimization placement process is guided. This process works like the one described before, but restricting certain areas of the chip to chosen FUs accordingly to their power consumption. Hot areas would be composed of FUs that have a high power density. On the other hand, elements with a lower power consumption will be placed, all together, in cold regions.

The considered algorithm is the same that the one described in Algorithms 1 or 3, but different topological constraints are included in the checkTopologyConstraints function. Obviously, neither FUs nor TSVs can occupy cells previously designed as air channels. The initial population is generated as in MFA_{FU} or MFA_{FU*}. However, as Figure 2 shows, feasible solutions obtained with these two algorithms could be incorporated as a starting point for the MFA_{AC} optimization process.

The definition of the topology is given by the designer and hence, is an input to the optimization system as shown in Figure 2. After that, it is the designer who specifies where isolating air channels should be routed.

4. Experimental set-up

Niagara2 and Niagara3 architectures are the base of our tests. This distribution has been modified to include 48 SPARC cores. These 48 cores have been distributed in four layers, composed of 8-core original

Niagara2 in layers one and two and 16-core original Niagara3 in layers three and four. This scenario will be used in the following for all the optimizations and simulations and also to compare different optimization strategies.

The floorplan has also been modified in order to include an increased number of cores which are placed in several layers of the 3D stack. Since MFA can place a variable number of cores in every layer, the power consumption of the crossbar is scaled accordingly to the number of cores found in every layer and their required bandwidth. The inter-layer communication is resolved with a set of TSVs that route the communication signals from one layer to another.

Worst case scenario has been set for power consumption. In our two realistic floorplans, power consumption is set to 84W and 139W for Niagara2 and Niagara3 respectively [22].

As has been shown in section 3, MFA_{FU*} will place the FUs that compose the 3D multi-processor architecture to minimize the temperature parameters. The area is set from the beginning of the optimization, and the original distribution of components defines the area of the optimization. The thermal results obtained by our floorplanner will be compared with the stacks composed by the two original layers, based on Niagara 2 and Niagara 3, presented in Figure 7. These two layers are disposed in order to build a 48 core system. Niagara2 is placed in first and second layer, and Niagara3 is used for layers 3 and 4. The cores (C), memories (L2), shared memories (L2B) and crossbar (Crossbar) are disposed in 4 layers.

Our experimental work will be focused on the analysis of the thermal optimization achieved by the floorplanner and the additional temperature reduction by the liquid cooling system. Additional modifications have been conducted. We have created two isolated thermal domains including air channels in the active layers. These channels isolate an area of the chip creating "hot islands" that will be then cooled with liquid channels. These air channels are placed at 5400μ m for layers 1 and 3 from the left side of the chip, and the same distance for layers 2 and 4 from the right side. Heat sources will be placed by the floorplanner in these areas, whereas FUs with lower power density will be placed in the warm region.

On the other hand, MFAs are configured with different parameters. Both MFA_{FU*} and MFA_{AC} are configured with a population of one hundred individuals and number of generations equal to the number of FUs, which prevents the algorithm from stacking in a local optimum. In both algorithms, crossover probability is set to 0.90 and the mutation probability is set to 1/number of FUs as recommended in [18].

 MFA_{TSV} and MFA_{LC} are configured with a maximum population of one hundred individuals, and a maximum number of 250 generations. The probability of mutation is set depending on the number of variables; in this particular case, it is the inverse of the number of available points to insert TSVs or liquid



Figure 7: Original floorplans [14]

channels, respectively. Then, we set a single point crossover with a probability of 0.90 and the tournament selection method, following the guidelines given in [18].

5. Results

This section presents the thermal results obtained in the scenarios described in Section 4. All the thermal values have been calculated using the thermal model described in section 2. All the designs presented in this section have been computed with MFA_{FU*}, MFA_{AC}, MFA_{TSV} and MFA_{LC}.

In addition to maximum temperature (in *K*) and total wirelength (in cells, each cell has 300μ m), we also include thermal gradient as a measure of reliability. Maximum temperature and wire length are presented as absolute values, thermal gradient is averaged among the layers.

Figure 8 depicts the thermal distribution of our baseline scenario, where all the cores are labeled as C{id}, memories as $L2_{id}$, shared memories as $L2_B$ {id}, and Crossbars as Crossbar{id}, where *id* is an identifier. As can be seen in the figure, hot areas appear, specially in first and second layers because they cannot dissipate heat as easy as top layers do.

5.1. Functional units and TSV placement: MFA_{FU*} + MFA_{TSV}

Figure 9 shows the non-dominated solutions obtained by both MFA_{FU*} and MFA_{TSV} . Figure 9(a) shows the resultant non-dominated front obtained by MFA_{FU*} . It is worth noting that the wire length is not realistic in the sense than the Manhattan distance has been also applied vertically, without adding TSVs yet. One of these non-dominated solutions must be selected by the system designer in order to apply both MFA_{TSV} and MFA_{LC} algorithms. In our case, we have selected the one with the lowest temperature, as illustrated in







Figure 8: Thermal maps of the original 48-core system [14]



Figure 9: (a) Set of non-dominated solutions obtained with MFA_{FU*} and the floorplan selected to be used in MFA_{TSV} and MFA_{TSV} . (b) Set of non-dominated solutions reached by MFA_{TSV} with the previous selected floorplan

Algorithm	Max.Temp. (K)	Grad. (K)	Wirelength (Cells)
Baseline Stack (Ø)	399	89	1012
MFA _{FU*}	362	43	-
$\dots + MFA_{TSV}$	362	43	1459

Table 3: Thermal and wire length comparison for the placement of FUs and TSVs

Figure 9(a). Figure 9(b) shows the non-dominated solutions obtained by MFA_{TSV} with the number of TSVs and chip wire length. The designer whill have to choose which solution is more convenient in every case, depending on the economic cost and technological issues. In out case, we have selected the point (11, 1459), since it fulfills the bandwith requirements for this particular scenario [14].

Finally, Figure 10 depicts the thermal maps of the solution selected in (MFA_{FU*} and MFA_{TSV}). Black spots in the figures show the position of the TSVs. As can be seen in the Table 3, we achieve a reduction of 38 K in maximum temperature when compared with the original scenario.

Table 3 compares the metrics obtained by the original 3D floorplan with the one that has been optimized with $MFA_{FU*}+MFA_{TSV}$. It is worth noting that the wiring of both the Niagara2 and Niagara3 architectures is isolated by layer in our baseline stack (no vertical communication occurs), highly optimized by the 2d floorplanner, and thus impossible to improve. For this reason, the total wire length has not been improved by our proposal. In the same manner, the wire length computed by MFA_{FU*} (912 cells) is not included in Table 3 because it is not realistic, i.e., the Manhattan distance cannot be applied between different layers in a realistic design.



Figure 10: Thermal maps of the optimized 48-core system. Black spots show the position of the TSVs.



Figure 11: (a) Set of non-dominated solutions obtained with MFA_{LC} over the baseline stack. (b) Set of non-dominated solutions reached by MFA_{LC} over the floorplan selected in MFA_{FU*}

As can be seen, our proposal is able to reduce chip temperature up to 37 K. However, as Table 3 shows, since we are connecting FUs in different layers the performance is worse than in the baseline 3D stack, even when including TSVs. However, if we compute the total wirelength using wire bonding as the inter-layer communication mechanism we could reach up to 2680 cells in wire length. This proves the convenience of using TSVs as the most promising solution to take advantage of 3D integration technology.

5.2. Liquid microchannel optimization: MFALC

The high temperatures reached in the baseline stack can be managed including liquid micro channels, as an effective way to decrease temperature in inner layers. In this scenario, 32 liquid channels were placed. To this end, we executed MFA_{LC} with $F_6 \leq 32$, obtaining the set of non-dominated solutions depicted in Figure 11. MFA_{LC} placed liquid channels in both the baseline stack and the optimized floorplan given by MFA_{FU*} + MFA_{TSV}. Obviously, the configuration with more liquid channels obtained the lowest temperature.

The optimized liquid channel placement thermogram can be seen in Figure 12 for the baseline stack. As can be seen in the Figure, hot areas have disappeared because channels can cool down the heat produced by the cores. The comparison results of placing channels following a homogeneous distribution (8 channels/layer), and optimizing their position using MFA_{LC} can be seen in table 4. The homogeneous distribution of liquid channels is able to reduce the temperature throughout the chip, however, optimizing channel placement improves maximum temperature and gradients.

Finding an optimal distribution for liquid channels improves not only thermal metrics, but also fabrication costs, because wider channels can be built to replace two or more thinner ones, also reducing pumping



Figure 12: Thermal maps of the original system with 32 optimized liquid channels. Arrowheads show the location of each channel.

LC Algorithm	Max.Temp. (K)	Grad. (K)	Wirelength (Cells)
Baseline Stack (Ø)	399	89	1012
Homogeneous (Ø)	348	46	1012
MFA _{LC}	341	38	1012

Table 4: Homogeneous and optimized liquid channels in the original distribution.



Figure 13: Thermal maps of the optimized system with 32 optimized liquid channels. Black spots show the position of the TSVs. Arrowheads show the location of each channel.

energy. The optimization of the placement of liquid channels achieves very good results, but these thermal results can be enhanced adding several optimizations such as FUs placement.

Let us now examine the placement of liquid channels over the optimized floorplan. As was previously commented, liquid placement optimizer evaluates not only hot areas but also TSVs location, because liquid channels cannot go through TSVs. In Figure 13 it can be seen that once the liquid channels are deployed, there are no longer hot areas. Optimizing both the placement of FUs, and the placement of liquid microchannels, we have achieved a reduction of 57 K in maximum temperature, 33 K in mean temperature and 66 K in the gradient when compared with the original scenario.

Table 5 shows data for the optimized placement of FUs, and the effect of adding 32 liquid channels following a homogeneous and optimized placement. Placing channels in an optimal way improves now every thermal metric. Including liquid channels does not change the wirelength since the routing is invariant.

LC Algorithm	Max.Temp. (K)	Grad. (K)	Wirelength (Cells)	
$MFA_{FU*} + \emptyset$	362	43	1459	
MFA _{FU*} + homogeneous placement	339	26	1459	
$MFA_{FU*} + MFA_{LC}$	335	24	1459	

Table 5: Homogeneous and optimized 32 liquid channels in the optimized distribution.

5.3. Air channel isolation: MFA_{AC}

One of the main contributions of this work is adding air channels to isolate thermal domains in the chip. This isolation makes the cooling process much easier, because liquid channels can be placed in those areas where the temperature is higher, reducing the number of deployed liquid microchannels to achieve the same thermal profile. This reduction in the number of microchannels implies a reduction in fabrication costs and in the energy designated for the pumping system.



Figure 14: Floorplan distribution with air isolation (MFAAC). * symbols limit the location of the air channel.

As was explained in section 4 a hot region and a warm region are created. Figure 14 presents the floorplan in the non-dominated front obtained by MFA_{AC} with the lowest temperature and without liquid channels, where * symbols represent the existence of an air channel. In this regard, Figure 15, shows the same scenario but after inserting 20 liquid channels with MFA_{LC} . As can be seen in Figure 14, the floorplanner has located



Figure 15: Resultant floorplan with air isolation and 20 liquid channels ($MFA_{AC} + MFA_{LC}$) * symbols limit the location of the air channel. Arrowheads show the position of liquid channels.

FUs with a high power consumption in hot regions (left side for layers 1 and 3; right side for layers 2 and 4) and FUs with lower power densities in warm regions. Once the placement has been done, liquid channels can be deployed in the 3D IC (see Figure 15). Most of the optimized channels are placed in hot regions but some of them are located with heat sinks units in order to obtain a homogeneous thermal distribution.

Table 6 shows the results when FUs have been placed in isolated areas, and liquid channels have also been optimized to decrease the temperature in the stack. With this approach, using MFA_{LC} , we can save the placement of 12 liquid channels, but still obtaining the same thermal results that were achieved with 32.

Floorplanner	LC placement	# of channels	Max.Temp. (K)	Grad. (K)
MFA _{AC}	-	0	377	61
MFA _{FU*}	Homogeneous	32	335	24
MFA _{AC}	MFA _{LC}	20	335	27

Table 6: Comparison between optimized floorplan with and without air channel isolation plus liquid microchannels (MFAAC + MFALC).

These results are shown in Figure 15 and Tables 5 and 6. These results have a very important impact in terms of technological costs and fabrication issues, and also a cost in the pumping energy required to drive liquid through the channels. Since some FUs are separated by the air channels, there is a small overhead in the wirelength. This overhead is compensated by the thermal benefits and the saving in the number of liquid channels and, according to [21], 5W of operating energy for the pumping system.

The reader could miss a comparison with other techniques. We certainly tried to compare our implementations of MFA_{FU*} + MFA_{TSV}, MFA_{LC} and MFA_{AC} with other state-of-the-art floorplanning algorithms. However, the most well known implementations in the literature using representations like Combined Bucket and 2D Array (CBA), Double-Tree and Sequence (DTS), Sequence Pair (SP) or Generalized Polish Expression (GPE) do not perform the placement of TSVs, LCs or ACs, unless TSVs and LCs are explicitly included as new passive elements in the algorithm. This would require a significant modification in MFA_{FU}, avoiding the use of MFA_{TSV} and MFA_{LC}. In this regard, a comparative study between CBA, DTS, SP, GPE and MFA_{FU} has been recently published in [23], obviously avoiding the placement of TSVs, LCs or ACs. Because of the different nature of CBA, DTS and SP, which are single-objective algorithms and GPE and MFA_{FU}, which are multi-objective algorithms, two sets of experiments were performed in [23]. In the first set of experiments, the multi-objective function of GPE and MFA_{FU} was transformed into three separate optimizations minimizing temperature, wire length and a weighted sum of both objectives, respectively. Results showed that starting in the same conditions, i.e., starting with random initial values, only CBA and MFA_{FU} reached feasible solutions. In all these cases MFA_{FU} obtained the best range of temperatures and wire length. Only when CBA, DTS, SP and GPE started with initial feasible solutions outperformed the wire length obtained by MFA_{FU}. In the second set of experiments, in a multi-objective optimization, GPE was not able to find a set of feasible solutions, whereas MFA_{FU} found a non-dominated set in all the experiments. Comparing these results with an execution of GPE with a set of initial feasible solutions, MFA_{FU} reached excellent temperatures but sacrificing wire length.

6. Conclusions

This work proposes a novel and an effective optimization process that combines three different evolutionary algorithms to enhance our previous and related work in the field. In this sense, our algorithms are capable of optimizing the placement of functional units and TSVs, taking into account their thermal contribution to the entire 3D stack. The optimization in the placement reduces thermal metrics in 3D IC. The complete floorplanner is demonstrated to achieve excellent results when placing FUs and TSVs. These results are widely improved by adding other design solutions such as the use of active cooling, using liquid channels whose locations have been also optimized with our proposed evolutionary algorithms. The floorplanner interfaces with an accurate thermal model, which calculates the results in the minimization of thermal and reliability parameters.

Experimental results have been obtained for a realistic many-core single-chip, resembling Niagara floorplan.

The addition of air channels to isolate thermal domains in the chip is an important contribution presented in this paper. The isolation helps on the cooling process, because our liquid channels can be placed in those areas with higher temperatures. This strategy reduces the number of deployed liquid microchannels to achieve the same thermal profile. This reduction directly impacts on fabrication costs and on the energy designated for the pumping system. In other words, the creation of hot regions using air channels inside the chip has resulted in an improvement of the thermal parameters, saving technological and energy costs.

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