Circuit Walks in Integral Polyhedra

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Abstract. Circuits play a fundamental role in the theory of linear programming due to their intimate connection to algorithms of combinatorial optimization and the efficiency of the simplex method. We are interested in better understanding the properties of circuit walks in integral polyhedra. In this paper, we introduce a hierarchy for integral polyhedra based on different types of behavior exhibited by their circuit walks. Many problems in combinatorial optimization fall into the most interesting categories of this hierarchy – steps of circuit walks only stop at integer points, at vertices, or follow actual edges. We classify several classical families of polyhedra within the hierarchy, including 0/1-polytopes, polyhedra defined by totally unimodular matrices, and more specifically matroid polytopes, transportation polytopes, and partition polytopes. Finally, we prove three characterizations of the simple polytopes that appear in the bottom level of the hierarchy where all circuit walks are edge walks, showing that such polytopes constitute a generalization of simplices and parallelotopes.

Keywords: edge walks, circuit walks, diameter, linear programming, integer programming, total unimodularity

MSC: 52B05, 90C05, 90C08, 90C10

1 Introduction

The search for a polynomial pivot rule for the simplex method is one of the fundamental open questions in linear programming. It motivates the studies of the combinatorial and circuit diameters of polyhedra. The *combinatorial diameter* of a polyhedron refers to the maximum number of steps needed to connect any pair of vertices by an edge walk. It is a lower bound on the best-case performance of the simplex method – in particular, a family of *n*-dimensional polyhedra with f facets whose diameter is super-polynomial in f and n would disprove the existence of a polynomial pivot rule for the simplex algorithm. While this is a classical field of study, there remain many open questions.

One of the attempts to gain a better understanding of the behavior of edge walks is the study of *circuit walks* and the associated *circuit diameters*. These generalize the concept of walking along the edges of a polyhedron to walking along its *circuits*. Whereas the famous Hirsch Conjecture is false in general [20,25], the analogous *Circuit Diameter Conjecture* [8], which asks whether the circuit diameter of a polyhedron is bounded by f - n, remains open [11,26].

We introduce some notation [8,9]: Given a polyhedron $P = \{\mathbf{x} \in \mathbb{R}^n : A\mathbf{x} = \mathbf{b}, B\mathbf{x} \leq \mathbf{d}\},$ the set of circuits of P, denoted $\mathcal{C}(A, B)$, consists of those $\mathbf{g} \in \ker(A) \setminus \{\mathbf{0}\}$ normalized to coprime integer components for which $B\mathbf{g}$ is support-minimal over the set $\{B\mathbf{x} : \mathbf{x} \in$ $\ker(A) \setminus \{\mathbf{0}\}$. Circuits also appear as *elementary vectors* in the literature [24]. It can be shown that the set of circuits consists of all potential edge directions of P as the right-hand side vectors **b** and **d** vary [17]. Note that $\mathcal{C}(A, B)$ is dependent on the representation of a polyhedron. When a polyhedron is not given through an \mathcal{H} -representation, we assume that its set of circuits corresponds to that of a minimal representation; i.e., that each constraint appears as a facet.

The directions of $\mathcal{C}(A, B)$ can be used to traverse P via a *circuit walk*:

Definition 1 (Circuit Walk). Let $P = {\mathbf{x} \in \mathbb{R}^n : A\mathbf{x} = \mathbf{b}, B\mathbf{x} \leq \mathbf{d}}$ be a polyhedron. For two vertices $\mathbf{v}^{(1)}, \mathbf{v}^{(2)}$ of P, we call a sequence $\mathbf{v}^{(1)} = \mathbf{y}^{(0)}, \dots, \mathbf{y}^{(k)} = \mathbf{v}^{(2)}$ a circuit walk of length k if for $i = 0, \dots, k - 1$ we have:

1. $\mathbf{y}^{(i)} \in P$, 2. $\mathbf{y}^{(i+1)} = \mathbf{y}^{(i)} + \alpha_i \mathbf{g}^{(i)}$ for some $\mathbf{g}^{(i)} \in \mathcal{C}(A, B)$ and $\alpha_i > 0$, and 3. $\mathbf{y}^{(i)} + \alpha \mathbf{g}^{(i)}$ is infeasible for all $\alpha > \alpha_i$.

If $\mathbf{y}^{(i)}$ is a vertex of P for i = 0, ..., k, we call the circuit walk a **vertex walk**. If $\mathbf{y}^{(i)}$ has integer components for i = 0, ..., k, we call the circuit walk **integral** (and **non-integral** otherwise).

Informally, circuit walks travel from an initial vertex to a terminating vertex by following circuit directions and taking steps of maximal length. In particular, these steps may go through the interior of P.

Further, as a generalization of the edge directions, C(A, B) provides an optimality certificate for any linear program over P [17]. Thus, there are many settings in mathematical programming in which algorithms construct circuit walks by taking augmenting steps along circuits [1,2,3,13,15,16,18]. For example, the computation of an improving circuit direction is a viable approach for dealing with highly degenerate vertices in the simplex method [16]. Additionally, an augmentation scheme along so-called greedy circuit directions takes only polynomially many steps [13,18]. The challenge here lies in finding a greedy circuit direction – it is open whether this can be done in polynomial time. However, it is possible to efficiently compute circuits for a steepest-descent augmentation scheme [13], which terminates in at most |C(A, B)| steps and runs in strongly polynomial time for polyhedra defined by totally unimodular matrices [12].

We are interested in the behavior of circuit walks constructed by such algorithms. We are especially interested in circuit walks within *integral polyhedra* – those polyhedra whose vertices have integer coordinates – due to the intimate relationship between circuits and methods from combinatorial optimization [5,7,10,19]: Many algorithms for classical problems from combinatorial optimization, such as transportation or network flow problems, can be interpreted as circuit walks in the underlying polyhedra. For example, in the context of a minimum-cost flow problem, circuits correspond to directed cycles in the associated network. It follows that the minimum mean cycle-canceling algorithm serves as an efficient implementation of the steepest-descent circuit augmentation scheme [13,16]. Graph-theoretic interpretations of circuits can also be used to prove bounds on the circuit diameter of classical polyhedra such as matching polytopes and the traveling salesman polytope [19].

By definition, a circuit walk in an integral polyhedron begins and ends at vertices. In general, however, the intermediate steps of the walk need not travel along edges, terminate at vertices, or even visit integral points. In this paper, we therefore define a hierarchy of integral polyhedra based on which of these various behaviors appear in a polyhedron. We contrast our approach with that of [6] in which different relaxations of Definition 1 (such

as circuit walks that do not take maximal steps or that may even leave the polyhedron) are used to define a hierarchy of circuit diameters. Our main results regarding the proposed hierarchy are presented in Section 2.

Outline

First, in Section 2.1 we formally define the hierarchy and show that all of its levels are distinct (Theorem 1). We also relate the hierarchy to an important challenge in the study of circuit diameters: all circuit walks in a polyhedron are vertex walks if and only if all of its circuit walks are reversible (Theorem 2). Short proofs are provided in Section 3.

Next, in Section 2.2 we discuss the relationship between the hierarchy and two wellknown families of integral polyhedra: 0/1-polytopes and those defined by totally unimodular matrices (or *TU polyhedra*). We show that circuit walks in general 0/1-polytopes can exhibit any behavior. However, we prove that all circuit walks in TU polyhedra are integral (Theorem 3), which implies that all circuit walks in TU 0/1-polytopes are vertex walks (Corollary 1). We classify examples of these polyhedra within the hierarchy (Theorem 4): matroid polytopes, transportation polyhedra, and so-called *bounded-size* and *fixed-size* partition polytopes. These results, which include a characterization of the edges and circuits of the bounded-size partition polytope, are proven in Sections 4 and 5.

Finally, in Section 2.3 we provide several characterizations of the simple polytopes in which all circuit walks are necessarily edge walks (Theorems 5 to 7). We show that such polytopes constitute a highly-symmetric generalization of the simplex and the *n*-parallelotope which we call the (n, d)-parallelotope. Proofs for these results are given in Section 6.

2 Results

2.1 A Hierarchy of Integral Polyhedra

We begin with the introduction of a hierarchy for integral polyhedra based on the behavior of their circuit walks. In particular, we classify a polyhedron according to the types of intermediate points which are reachable via circuit walks. See Figure 2 for a visualization of the hierarchy.

The levels of the hierarchy are successively more restrictive. At the top, least-restrictive level of the hierarchy are integral polyhedra with general circuit walk (GCW) behavior – namely, their circuit walks may be non-integral. Below this are ICW polyhedra: integral polyhedra in which all circuit walks are necessarily integral. This is followed by VCW polyhedra: integral polyhedra in which all circuit walks are vertex walks. The bottom, most-restrictive level consists of ECW polyhedra in which the only circuit walks are edge walks. Low-dimensional examples of polyhedra from each level of the hierarchy are given in Figure 1. The behaviors of the circuit walks in these polyhedra yield our first result, formally proven in Section 3.1.

Theorem 1. All integral polyhedra fall into the hierarchy based on circuit walk behavior depicted in Figure 2. The four levels of the hierarchy – GCW, ICW, VCW, and ECW polyhedra – are distinct.

The location of a polyhedron within this hierarchy has strong implications on the behavior of a circuit augmentation scheme when applied to the polyhedron. The middle levels



(a) A GCW polyhedron with a nonintegral circuit walk.



(c) A VCW polyhedron in which all circuit walks are vertex walks.



(b) An ICW polyhedron in which all circuit walks are integral.



(d) An ECW polyhedron in which all circuit walks are edge walks.

Fig. 1: Two-dimensional examples of polyhedra from each level of the hierarchy.

of the hierarchy ensure that the algorithm will only visit either integral points or vertices of the polyhedron. At the bottom level, any circuit augmentation scheme is necessarily some variation of the simplex method.

We can also connect this hierarchy to one of the biggest challenges in the study of circuit diameters: Unlike edge walks, circuit walks are not necessarily reversible [8]. For example, reversing the walks depicted in Figures 1a and 1b does not yield maximal circuit walks. However, as depicted in Figure 2 and proven in Section 3.2, the hierarchy characterizes the polyhedra in which all circuit walks are reversible:

Theorem 2. All circuit walks in a polyhedron are reversible if and only if all circuit walks in the polyhedron are vertex walks.



Fig. 2: A hierarchy for integral polyhedra based on the behavior of their circuit walks. The VCW level is equivalent to the polyhedra in which all circuit walks are reversible.

2.2 0/1-polytopes and Totally Unimodular Matrices

Next, we discuss how two important families of polyhedra from combinatorial optimization relate to the hierarchy: 0/1-polytopes and TU polyhedra.

0/1-polytopes are widely studied due to their relationship to classical combinatorial optimization problems involving binary decisions. Their combinatorial diameter satisfies the Hirsch Conjecture [22] and hence also the Circuit Diameter Conjecture.

We note that in general, circuit walks in 0/1-polytopes need not be integral. Consider the example in Figure 3. The edge direction (1, 1, 0) is a circuit. However, when taking a step in this direction starting at the vertex (0, 0, 0), we reach the non-integral midpoint $(\frac{1}{2}, \frac{1}{2}, 0)$ of an edge.

There are important classes of 0/1-polytopes from combinatorial optimization which also exhibit GCW behavior. For example, *matroid polytopes* are a family of 0/1-polytopes in which circuit walks need not be integral. Given a matroid M with ground set E and rank function f, the matroid polytope P(f) associated with M is the convex hull of the incidence vectors $\mathbf{x} \in \{0, 1\}^E$ of the independent sets of M. We use a common inequality representation [28] to describe the possible behaviors of the circuit walks in P(f) in Section 5.1.

Another important class of integral polyhedra are those defined by totally unimodular matrices – which we call TU polyhedra. These polyhedra are guaranteed to be integral for any integral right-hand side, and are extensively studied due to appearing in transportation, assignment, and network flow problems. Their combinatorial (and circuit) diameter is polynomially bounded [4,14] and linear programming over them is efficient [27].

We show that all TU polyhedra are in fact ICW. This suggests that any algorithm which traverses such a polyhedron via a circuit walk has a combinatorial interpretation.

Theorem 3. Let $P = \{\mathbf{x} \in \mathbb{R}^n : A\mathbf{x} = \mathbf{b}, B\mathbf{x} \leq \mathbf{d}\}$ be an integral polyhedron whose constraint matrix $\binom{A}{B}$ is totally unimodular. Then all circuit walks in P are integral.

We provide a proof of Theorem 3 in Section 4, but we see another good way to prove the claim from a careful extension of Proposition 3.3 in [23]. The merit of our approach is that it provides a generalization to polyhedra in any representation and requires only basic linear algebra.

Note that total unimodularity is not a necessary condition for the ICW property. This can be observed in the polyhedra from Figures 1b and 1c, which can be represented via non-TU constraint matrices. Additionally, total unimodularity is not a sufficient condition for the VCW property. For instance, the *transportation polytope*, whose circuits are characterized



Fig. 3: A 0/1-polytope in \mathbb{R}^3 with non-integral circuit walks.

in [7], can have many non-vertex circuit walks. We discuss the behavior of these walks in Section 5.2.

However, by combining Theorem 3 with the fact that all integral points in 0/1-polytopes are vertices, we immediately see that all 0/1-polytopes defined by TU matrices are VCW.

Corollary 1. Let $P = {\mathbf{x} \in \mathbb{R}^n : A\mathbf{x} = \mathbf{b}, B\mathbf{x} \leq \mathbf{d}}$ be an integral polyhedron whose constraint matrix $\binom{A}{B}$ is totally unimodular. If P is a 0/1-polytope, then all circuit walks in P are vertex walks.

One example of such a polytope is the bounded-size partition polytope $PP(\kappa^{\pm})$, which is associated with the partitioning of a set of n items into k clusters $C_1, ..., C_k$ where each cluster C_i has an upper bound κ_i^+ and a lower bound κ_i^- on its size. The vertices of $PP(\kappa^{\pm})$ correspond to all feasible clusterings. In Section 5.3, we characterize the edges and the circuits of this polytope. It then follows that although both circuit walks and edge walks in $PP(\kappa^{\pm})$ travel from vertex to vertex (and hence from clustering to clustering), the circuit walks exhibit a more general behavior.

On the other hand, the related fixed-size partition polytope $PP(\kappa)$ is a TU 0/1-polytope associated with the partitioning of a set of n items into k clusters $C_1, ..., C_k$ where the size of cluster C_i is fixed at κ_i [5]. In Section 5.4, we show that, unlike the bounded-size partition polytope, all circuit walks in $PP(\kappa)$ are in fact edge walks.

The examples from this section together imply an additional result. Namely, as proven in Section 5, there exist well-known polyhedra from combinatorial optimization in each level of the hierarchy from Section 2.1.

Theorem 4. There exist specific examples of integral polyhedra from combinatorial optimization in each of the four distinct levels of the hierarchy based on circuit walk behavior. In particular:

- a) There exist matroid polytopes which are GCW but not ICW.
- b) There exist transportation polytopes which are ICW but not VCW.
- c) There exist bounded-size partition polytopes which are VCW but not ECW.
- d) All fixed-size partition polytopes are ECW.

A visualization of the results from this section (along with the results from the upcoming Section 2.3) in terms of the hierarchy is given in Figure 4.



Fig. 4: The results of Sections 2.2 and 2.3 in terms of the hierarchy from Section 2.1. The left-hand side shows where well-known families of polyhedra belong in the hierarchy, and the right-hand side gives specific examples from combinatorial optimization for each level.

2.3 ECW Polyhedra

In this section we characterize the simple polytopes at the bottom level of the hierarchy in which all circuit walks are edge walks. Our characterizations are quite restrictive and have strong implications on the degenerate polytopes in the category as well. But surprisingly, non-trivial examples of (degenerate) polyhedra from this category do appear in practice. We provide an example – the *fixed-size partition polytope* – at the end of the section.

An *n*-dimensional polyhedron is said to be *simple* – or *non-degenerate* – if each vertex belongs to exactly *n* facets. On the other hand, a *degenerate* polyhedron contains a vertex belonging to more than *n* facets. Simple polyhedra are of interest in the study of diameters as it suffices to only consider this class of polyhedra to bound the combinatorial diameter of any *n*-dimensional polyhedron with a fixed number of facets [20]. While much harder to prove, the same holds for circuit diameters [11].

The structure of simple polyhedra offers several useful characterizations of ECW polytopes. Our main result is that the only simple polytopes exhibiting this behavior are intimately related to the highly-structured simplex and parallelotope.

Our first important tool is what we call elementary cones. Consider a full-dimensional polyhedron $P = \{\mathbf{x} \in \mathbb{R}^n : B\mathbf{x} \leq \mathbf{d}\}$ and the hyperplane arrangement in \mathbb{R}^n consisting of the hyperplanes $B_i\mathbf{x} = 0$ for each row B_i of B. These hyperplanes each contain the origin and partition \mathbb{R}^n into *n*-dimensional polyhedral cones with disjoint interiors. We call this arrangement of hyperplanes the elementary arrangement of P and refer to the inclusion-minimal *n*-dimensional cones in the arrangement as the elementary cones of P.

It is not difficult to see that elementary cones are generated by circuits (Lemma 5). We use this fact to give a first characterization of simple ECW polytopes: the inner cones of all vertices must be elementary cones. Recall that given a vertex \mathbf{v} of a polyhedron P, the inner cone $I(\mathbf{v})$ of \mathbf{v} is the cone consisting of all feasible directions at \mathbf{v} with respect to P.

Theorem 5 (Elementary Cone Condition). Let $P = {\mathbf{x} \in \mathbb{R}^n : B\mathbf{x} \leq \mathbf{d}}$ be a fulldimensional, simple polytope. All circuit walks in P are edge walks if and only if for each vertex $\mathbf{v} \in P$, the inner cone $I(\mathbf{v})$ is an elementary cone of P.

Next, we prove that all polytopes satisfying this *elementary cone condition* are highly symmetric: the inner cones of vertices that do not share a facet are opposites of each other. By imposing that this property transfers to vertices belonging to a common face (and stating it with respect to the affine hull of the face), we obtain a second characterization. Given a pair of vertices \mathbf{u}, \mathbf{v} of a polyhedron P, we let P^{uv} denote the inclusion-minimal face of P containing \mathbf{u} and \mathbf{v} and let $I^{uv}(\mathbf{u}), I^{uv}(\mathbf{v})$ denote the inner cones of \mathbf{u}, \mathbf{v} with respect to P^{uv} .

Theorem 6 (Symmetric Inner Cone Condition). Let P be a simple polytope given by a minimal representation. All circuit walks in P are edge walks if and only if $I^{uv}(\mathbf{u}) = -I^{uv}(\mathbf{v})$ for all pairs of vertices \mathbf{u}, \mathbf{v} in P.

Naturally, the symmetric inner cone condition of Theorem 6 is only satisfied by quite symmetric polyhedra. One such example is the *parallelotope* of dimension n, also called the n-parallelotope: a vertex-transitive polytope with n pairs of parallel, opposite facets and 2^n vertices. Equivalently, an n-parallelotope is a zonotope generated by a set of n linearly independent vectors in general position, which correspond to its edge directions. We show that the only other polytopes satisfying the symmetric inner cone condition constitute a generalization of the n-parallelotope which we call the (n, d)-parallelotope.



Fig. 5: Examples of (n, d)-parallelotopes in \mathbb{R}^3 . From left to right: The (3, 1)-parallelotope (the 3-simplex), the (3, 2)-parallelotope, and the (3, 3)-parallelotope (the 3-parallelotope). The (3, 2)-parallelotope is the only simple ECW polytope in \mathbb{R}^3 that is not a simplex or parallelotope.

Definition 2 ((n, d)-parallelotope). Given $d \in \{1, ..., n\}$, an (n, d)-parallelotope is an *n*-dimensional polytope with n + d facets which satisfies the symmetric inner cone condition and in which each vertex belongs to a d-parallelotope face.

Note that an (n, n)-parallelotope is simply an *n*-parallelotope and an (n, 1)-parallelotope is an *n*-simplex. Other instances of (n, d)-parallelotopes, such as the (3, 2)-parallelotope pictured in Figure 5, are highly symmetric hybrids of the simplex and the parallelotope. We show that all (n, d)-parallelotopes are ECW (Lemma 9), which yields a final characterization.

Theorem 7. Let P be an n-dimensional, simple polytope given by a minimal representation. All circuit walks in P are edge walks if and only if P is an (n, d)-parallelotope.

The proofs of Theorems 5 to 7 and the related Lemmas 5 to 9 in Section 6 provide further insight into the structure of (n, d)-parallelotopes.

We comment on the two restrictions in our characterization: we only treat bounded and simple polytopes. Since circuit walks are defined to start and terminate at a vertex, a circuit walk in an unbounded polyhedron will never use a circuit direction from the recession cone. However, the facets of the recession cone may still intersect with facets from the "bounded part" of the polyhedron to introduce new circuits to be used in a circuit walk.

Additionally, the analysis of the inner cones in a degenerate ECW polyhedron becomes significantly more challenging. Opposite inner cones need not completely mirror each other as in Theorem 6 – instead the edge directions of one inner cone could be a superset or subset of the directions of its opposite. Some of our results readily transfer to degenerate polytopes – for example, all two-dimensional faces of (degenerate) ECW polytopes must be either triangles or parallelograms. Despite this restrictive property, such polytopes do appear in practice. As stated in Theorem 4, one example is the (highly) degenerate fixed-size partition polytope (Section 5.4).

An extension of our characterization of simple ECW polytopes to all ECW polyhedra is a natural but challenging next step for the presented line of research.

3 Proofs for Theorems 1 and 2

3.1 Proof of Theorem 1

We prove Theorem 1, which states that the levels in the hierarchy for integral polyhedra based on circuit walk behavior – as depicted in Figure 2 – are distinct. Although the result

also follows from the more detailed Theorem 4, we provide a short proof here using lowdimensional examples.

Proof (of Theorem 1). Recall the two-dimensional integral polyhedra from Figure 1, and assume a minimal algebraic representation for each polyhedron. This implies that we can characterize the set of circuits for each polyhedron based on its geometric properties; in particular, for two-dimensional polyhedra, all circuits appear as edge directions. It follows that the set of circuits for the examples in Figures 1a to 1c is $\{\pm(1,0),\pm(0,1),\pm(1,1),\pm(1,-1)\}$.

Consider first Figure 1a. Clearly, taking a maximal step in the circuit direction (1, -1) from the point $\mathbf{y}^{(0)}$ leads to the non-integral point $\mathbf{y}^{(1)}$. Therefore, the polyhedron is GCW but not ICW.

In Figure 1b, it is not difficult to observe via complete enumeration that, starting at any vertex in the polyhedron and taking maximal steps along circuit directions, all reachable points are indeed integral. However, some of these points – such as $\mathbf{y}^{(1)}$, $\mathbf{y}^{(2)}$, and $\mathbf{y}^{(4)}$ – need not be vertices. Hence the polyhedron is ICW but not VCW.

Similarly, in Figure 1c, only vertices are reachable from any starting vertex via maximal circuit steps. However, some of these steps – such as that from $\mathbf{y}^{(0)}$ to $\mathbf{y}^{(1)}$ – need not travel along edges. Thus, the polyhedron is VCW but not ECW.

Finally, assuming a minimal representation, the only circuits of the polyhedron in Figure 1d are $\{\pm(1,0)\pm(0,1)\}$. It is then clear that, starting at any vertex, the only feasible circuit steps must travel along edges. Hence, the polyhedron is ECW.

3.2 Proof of Theorem 2

We prove Theorem 2, which states that all circuit walks in a polyhedron are reversible if and only if all of its circuit walks are vertex walks.

Proof (of Theorem 2). First, let P be a polyhedron in which all circuit walks are vertex walks and suppose there exists a circuit walk $\mathbf{v}^{(1)} = \mathbf{y}^{(0)}, \mathbf{y}^{(1)}, ..., \mathbf{y}^{(k)} = \mathbf{v}^{(2)}$ in P that is not reversible. Then the reversed walk $\mathbf{y}^{(k)}, ..., \mathbf{y}^{(1)}$ must not be maximal. In particular, let i denote an index such that the step from $\mathbf{y}^{(i)}$ to $\mathbf{y}^{(i-1)}$ is not maximal. Thus, taking a maximal step from $\mathbf{y}^{(i)}$ along the direction $\mathbf{y}^{(i-1)} - \mathbf{y}^{(i)}$ leads to some point $\mathbf{z} \neq \mathbf{y}^{(i-1)}$ in P. However, this implies that $\mathbf{y}^{(i-1)}$ can be expressed as a convex combination of \mathbf{z} and $\mathbf{y}^{(i)}$, contradicting the fact that $\mathbf{y}^{(i-1)}$ is a vertex of P.

Conversely, let P be a polyhedron which contains a circuit walk $\mathbf{v}^{(1)} = \mathbf{y}^{(0)}, \mathbf{y}^{(1)}, ..., \mathbf{y}^{(k)} = \mathbf{v}^{(2)}$ that is not a vertex walk. Then some step $\mathbf{y}^{(i)}$ of the walk belongs to the strict interior of a face F of P with dimension greater than zero. Since P is pointed, there exists a vertex \mathbf{u} in F. Furthermore, there exists a walk $\mathbf{y}^{(i)} = \mathbf{z}^{(0)}, \mathbf{z}^{(1)}, ..., \mathbf{z}^{(t)} = \mathbf{u}$ in F which uses only edge directions of F and takes maximal steps. Hence, $\mathbf{v}^{(1)} = \mathbf{y}^{(0)}, ..., \mathbf{y}^{(i)} = \mathbf{z}^{(0)}, \mathbf{z}^{(1)}, ..., \mathbf{z}^{(t)} = \mathbf{u}$ is a circuit walk in P. This circuit walk is not reversible since $\mathbf{y}^{(i)}$ belongs to the strict interior of F and the circuit direction immediately following $\mathbf{y}^{(i)}$ on the walk is an edge direction of F.

4 Proof of Theorem 3

The fact that TU polyhedra are ICW is not surprising since such a polyhedron has integral vertices for any integral right-hand side. We present a complete proof for a general integral

polyhedron of the form $P = \{\mathbf{x} \in \mathbb{R}^n : A\mathbf{x} = \mathbf{b}, B\mathbf{x} \leq \mathbf{d}\}$. We note that this result can be obtained in various ways – in particular, it can be achieved by solving a linear program over a certain one-dimensional TU polyhedron. However, the upcoming Lemmas 1 and 2 follow from basic linear algebra and have additional useful implications [12]. We also refer the reader to the intimately related and well-presented results surrounding Proposition 3.3 in [23], which apply to polyhedra in standard form.

We begin with an important property of circuits which is used in [12] and can be derived from Proposition 1 in [19]. A short proof is included for the sake of completeness.

Lemma 1 ([12,19]). Let $P = \{\mathbf{x} \in \mathbb{R}^n : A\mathbf{x} = \mathbf{b}, B\mathbf{x} \leq \mathbf{d}\}$ be a pointed polyhedron, let $\mathbf{g} \in \ker(A)$ with coprime integer components be given, and let B' denote the maximal row-submatrix of B such that $B'\mathbf{g} = \mathbf{0}$. Then \mathbf{g} is a circuit of P if and only if rank $\binom{A}{B'} = n - 1$.

Proof. Suppose first that **g** is a circuit of *P*. Since *P* is pointed, rank $\binom{A}{B'} \leq n-1$. If rank $\binom{A}{B'} < n-1$, there exist rows of *B* which can be added to *B'* to form a row-submatrix *B''* of *B* with rank $\binom{A}{B''} = n-1$. However, ker $\binom{A}{B''}$ is then generated by some **y** with $\operatorname{supp}(B\mathbf{y}) \subseteq \operatorname{supp}(B\mathbf{g})$, contradicting the fact that **g** is a circuit.

Conversely, if rank $\binom{A}{B'} = n - 1$ then ker $\binom{A}{B'}$ is generated by **g**. Hence, any $\mathbf{y} \in \text{ker}(A) \setminus \{\mathbf{0}\}$ satisfying $\text{supp}(B\mathbf{y}) \subseteq \text{supp}(B\mathbf{g})$ is a scalar multiple of **g**, implying that **g** is a circuit.

This property yields the following lemma, which generalizes Proposition 3.3 in [23] by relating the components of a circuit \mathbf{g} and the corresponding vector $B\mathbf{g}$ to the maximum absolute subdeterminant of the constraint matrices.

Lemma 2 ([23]). Let $P = \{\mathbf{x} \in \mathbb{R}^n : A\mathbf{x} = \mathbf{b}, B\mathbf{x} \leq \mathbf{d}\}$ be a polyhedron and let $\mathbf{g} \in \mathcal{C}(A, B)$ be a circuit of P. Then $\max_i |\mathbf{g}_i| \leq \Delta(M)$ and $\max_i |(B\mathbf{g})_i| \leq \Delta(M)$, where $M := \begin{pmatrix} A \\ B \end{pmatrix}$ and $\Delta(M)$ denotes the maximum absolute value of a subdeterminant of M.

Proof. Let B' denote the maximal row-submatrix of B such that $B'\mathbf{g} = \mathbf{0}$. By Lemma 1, rank $\binom{A}{B'} = n - 1$. Consider the kernel of the matrix

$$M_{B'} = \begin{pmatrix} A & \mathbf{0} \\ B' & \mathbf{0} \\ B & -I \end{pmatrix}$$

Any $(\mathbf{x}, \mathbf{y})^T \in \ker(M_{B'})$ must satisfy $\mathbf{y} = B\mathbf{x}$ in addition to $A\mathbf{x} = \mathbf{0}$ and $B'\mathbf{x} = \mathbf{0}$. Since \mathbf{g} generates $\ker\begin{pmatrix}A\\B'\end{pmatrix}$, it follows that $\ker(M_{B'})$ is one-dimensional and generated by $(\mathbf{g}, B\mathbf{g})^T$. Cramer's rule then yields

$$\max_{i} \left| (\mathbf{g}, B\mathbf{g})_{i}^{T} \right| \leq \Delta \begin{pmatrix} A & \mathbf{0} \\ B' & \mathbf{0} \\ B & -I \end{pmatrix} = \Delta(M).$$

As a corollary to Lemma 2, if $\binom{A}{B}$ is totally unimodular then any circuit $\mathbf{g} \in \mathcal{C}(A, B)$ satisfies $\mathbf{g} \in \{0, 1, -1\}^n$ and $B\mathbf{g} \in \{0, 1, -1\}^m$. Theorem 3 now follows directly.

Theorem 3 Let $P = \{\mathbf{x} \in \mathbb{R}^n : A\mathbf{x} = \mathbf{b}, B\mathbf{x} \leq \mathbf{d}\}$ be an integral polyhedron whose constraint matrix $\binom{A}{B}$ is totally unimodular. Then all circuit walks in P are integral.

Proof. We may assume that the right-hand side vectors **b** and **d** are integral, for otherwise either P would be empty or the components of **d** could be rounded up without changing the polyhedron. Let **x** be any integral point in P and let $\mathbf{g} \in C(A, B)$ be a feasible circuit direction at **x**. For any strict inequality $(B\mathbf{x})_i < \mathbf{d}_i$ at **x**, we must have $(B\mathbf{x})_i \leq \mathbf{d}_i - 1$ since B and **d** are integral. Applying a step with step size $\alpha = 1$ in the circuit direction \mathbf{g} , it follows by Lemma 2 that $(B(\mathbf{x} + \mathbf{g}))_i = (B\mathbf{x})_i + (B\mathbf{g})_i \leq (B\mathbf{x})_i + 1 \leq \mathbf{d}_i$. Continuing in this direction until an inequality becomes strict, we see that the stopping point $\mathbf{x} + \alpha \mathbf{g}$ must be integral with integral step size α .

5 Proof of Theorem 4

In this section we prove Theorem 4, which states that there exist well-known examples of integral polyhedra in each of the four layers of the hierarchy based on circuit walk behavior. Namely, we show that there are matroid polytopes which are GCW but not ICW (Section 5.1), that there are transportion polytopes which are ICW but not VCW (Section 5.2), that there are bounded-size partition polytopes which are VCW but not ECW (Section 5.3), and that all fixed-size partition polytopes are ECW (Section 5.4).

5.1 Matroid Polytopes

For a matroid M with ground set E and rank function f, the matroid polytope P(f) associated with M can be represented as:

$$P(f) = \left\{ \mathbf{x} \in \mathbb{R}^E : \mathbf{x} \ge \mathbf{0}, \ \sum_{e \in S} \mathbf{x}_e \le f(S) \ \forall S \subseteq E \right\}.$$

The vertices of P(f) consist of all $\mathbf{x} \in \{0, 1\}^E$ that are incidence vectors of the independent sets of M. Two vertices are adjacent if and only if they differ in exactly one coordinate or they differ in exactly two coordinates while satisfying a certain quite technical ordering relation [28].

We examine the behavior of circuit walks in P(f). The matrix B in the system $B\mathbf{x} \leq \mathbf{d}$ defining P(f) consists of the identity matrix and a submatrix corresponding to the constraints of the form $\sum_{e \in S} \mathbf{x}_e \leq f(S)$. A vector $\mathbf{g} \in \mathbb{R}^E \setminus \{\mathbf{0}\}$ with coprime integer components is a circuit of P(f) when $B\mathbf{g}$ is support-minimal over $\{B\mathbf{x} : \mathbf{x} \in \mathbb{R}^E \setminus \{\mathbf{0}\}\}$. Note that each positive and negative unit vector is therefore a circuit of P(f). Any circuit walk in P(f)that exclusively uses these directions is an edge walk and can be interpreted as individually adding/removing elements from an independent set of M. Additionally, the difference of any two unit vectors is a circuit of P(f). Combinatorially, these circuits correspond to swapping out some element of an independent set of M for another. A circuit walk which exclusively uses these directions can traverse edges of P(f) when the adjacency conditions of [28] are satisfied, but it is possible that the walk is only a vertex walk and not an edge walk.

Furthermore, a circuit walk in P(f) may be non-integral. Since P(f) is a 0/1-polytope, only circuits from $\{0, 1, -1\}^E$ can be used in an integral circuit walk. However, P(f) has many circuits outside this domain. For instance, if $\{1, 2, 3, 4\} \subseteq E$, consider the vector $\mathbf{g} \in \mathbb{R}^E$ where:

$$\mathbf{g}_e = \begin{cases} 2 & \text{if } e = 1 \\ -1 & \text{if } e \in \{2, 3, 4\} \\ 0 & \text{otherwise.} \end{cases}$$

To see that **g** is a circuit, note that for any $S \subsetneq E$ containing $\{1\}$ and some 2-set of $\{2,3,4\}$, we have $\sum_{e \in S} \mathbf{g}_e = 0$. However, for any nonzero $\mathbf{y} \in \mathbb{R}^E$ whose support is strictly contained in the support of **g**, it can be shown that $\sum_{e \in S} \mathbf{y}_e \neq 0$ for some such subset S. Therefore, **g** is indeed a circuit of P(f). If $I := \{2,3,4\}$ is an independent set of M, then taking a step in the direction of **g** starting at the corresponding vertex \mathbf{v}_I of P(f) leads to a non-integral point in P(f). In fact, for any rank function f, if $|E| \ge 4$ and if M contains any independent set with size at least three, then a non-integral circuit walk can be constructed in P(f).

5.2 Transportation Polytopes

Given a set of m suppliers and n customers where $\mathbf{u} \in \mathbb{Z}_+^m$ gives the supply of each supplier and $\mathbf{v} \in \mathbb{Z}_+^n$ gives the demand of each customer, the corresponding *transportation polytope* P consists of all $\mathbf{y} \in \mathbb{R}^{mn}$ that describe feasible commodity flow assignments from suppliers to customers:

$$\sum_{j=1}^{n} y_{ij} = u_i, \quad i = 1, ..., m$$
$$\sum_{i=1}^{m} y_{ij} = v_j, \quad j = 1, ..., n$$
$$y_{ij} \ge 0, \quad i = 1, ..., m, \ j = 1, ..., n.$$

Given a feasible flow assignment $\mathbf{y} \in P$, the support graph $B(\mathbf{y})$ of \mathbf{y} is the bipartite graph with partite sets corresponding to the suppliers and customers in which there exists an edge with weight y_{ij} between supplier *i* and customer *j* if and only if $y_{ij} > 0$. It can be shown that any $\mathbf{y} \in P$ is a vertex of *P* if and only if $B(\mathbf{y})$ is acyclic. Further, two vertices are adjacent if and only if the union of the corresponding support graphs contains exactly one cycle [21].

It follows that the circuits of P consist of all simple cyclical exchanges of flow among the suppliers and customers [7]. Specifically, $\mathbf{g} \in \mathbb{R}^{mn}$ is a circuit of P if and only if the support of \mathbf{g} corresponds to a cycle in the complete bipartite graph $K_{m,n}$ whose edges alternately correspond to components 1 and -1 of \mathbf{g} . Hence, for any $\mathbf{y} \in P$, applying a step in a feasible circuit direction from \mathbf{y} corresponds to reducing weight along every other edge of some cycle of $K_{m,n}$ while simultaneously increasing weight along the remaining edges of the cycle. The step terminates once the weight of an edge in $B(\mathbf{y})$ is reduced to 0.

Since the constraint matrix of P is totally unimodular, we know by Theorem 3 that all circuit walks in P are integral. However, it need not hold that all circuit walks are vertex walks. Equivalently, if \mathbf{x} is a vertex of P and \mathbf{y} is reached by a maximal circuit step from \mathbf{x} , then although $B(\mathbf{x})$ is acyclic, it need not hold that $B(\mathbf{y})$ is acyclic.

As an example, consider the transportation problem with suppliers s_1, s_2, s_3 and customers c_1, c_2, c_3 , where $\mathbf{u} = \mathbf{v} = (1, 2, 2)^T$. Then

$$\mathbf{x} = (x_{11}, x_{12}, x_{13}, x_{21}, x_{22}, x_{23}, x_{31}, x_{32}, x_{33})^T = (0, 1, 0, 1, 0, 1, 0, 1, 1)^T$$

is a vertex of P and $\mathbf{g} = (1, -1, 0, -1, 1, 0, 0, 0, 0)^T$ is a circuit. However, after applying a step in the direction of \mathbf{g} from \mathbf{x} we reach a solution whose support graph is cyclic, and thus not a vertex. See Figure 6.



Fig. 6: A circuit step in a transportation polytope that does not lead to a vertex.

5.3 Bounded-size Partition Polytopes

Similar to the partition polytopes for fixed-size clusterings introduced in [5], the boundedsize partition polytope $PP(\kappa^{\pm})$ is associated with the partitioning of a set $X = \{x_1, ..., x_n\}$ of items into clusters $C_1, ..., C_k$, where each cluster C_i must satisfy $\kappa_i^- \leq |C_i| \leq \kappa_i^+$ given $\kappa_i^-, \kappa_i^+ \in \mathbb{Z}_+$. For i = 1, ..., k and j = 1, ..., n, let y_{ij} be a binary variable indicating whether or not item x_j is assigned to cluster C_i . Then $PP(\kappa^{\pm})$ is the 0/1-polytope defined by the following system of constraints:

$$\sum_{i=1}^{k} y_{ij} = 1 \qquad j = 1, ..., n$$
$$\sum_{j=1}^{n} y_{ij} \ge \kappa_i^- \qquad i = 1, ..., k$$
$$\sum_{j=1}^{n} y_{ij} \le \kappa_i^+ \qquad i = 1, ..., k$$
$$y_{ij} \ge 0 \qquad i = 1, ..., k, \ j = 1, ..., n.$$

We note that this polytope is an instance of the bounded-shape partition polytope described in [10] if X is the standard basis of \mathbb{R}^n .

As the constraint matrix defining the polytope is totally unimodular and the right-hand sides are integral, the vertices of $PP(\kappa^{\pm})$ consist of those $\mathbf{y} \in \{0,1\}^{kn}$ corresponding to feasible clustering assignments. As in [5] and [10], given two such assignments $\mathbf{y}^1, \mathbf{y}^2$, define the *clustering difference graph* $CDG(\mathbf{y}^1, \mathbf{y}^2)$ from \mathbf{y}^1 to \mathbf{y}^2 to be the directed graph with nodes $c_1, ..., c_k$ where an edge (c_i, c_ℓ) with label x_j is included if and only if $\mathbf{y}_{ij}^1 = \mathbf{y}_{\ell j}^2 = 1$ with $i \neq \ell$. Thus, the edges of $CDG(\mathbf{y}^1, \mathbf{y}^2)$ give all single-item transfers necessary in order to transform the clustering assignment of \mathbf{y}^1 into that of \mathbf{y}^2 . An example of a simple CDGis given in Figure 7.

A necessary condition for vertices $\mathbf{y}^1, \mathbf{y}^2$ of $PP(\kappa^{\pm})$ to share an edge is that $CDG(\mathbf{y}^1, \mathbf{y}^2)$ is either a directed path or a directed cycle [10]. Here, we use clustering difference graphs to provide a full characterization of both the edges and the circuits of $PP(\kappa^{\pm})$.

To do so, given a pair of clustering assignments $\mathbf{y}^1, \mathbf{y}^2$, let $C^1 = (C_1^1, ..., C_k^1)$ be the clustering of X associated with \mathbf{y}^1 and let $C^2 = (C_1^2, ..., C_k^2)$ be the clustering associated with \mathbf{y}^2 . We say that a node c_i of $CDG(\mathbf{y}^1, \mathbf{y}^2)$ is free if $\kappa_i^- < |C_i^1| < \kappa_i^+$. Hence C_i^1 may



Fig. 7: A depiction of the clustering difference graph $CDG(\mathbf{y}^1, \mathbf{y}^2)$ when \mathbf{y}^1 corresponds to the clustering $C^1 = (\{x_1\}, \{x_2\}, \{x_3\}, \{x_4\}, \{x_5\}, \{x_6\})$ and \mathbf{y}^2 corresponds to $C^2 = (\{x_4\}, \{x_1\}, \{x_2\}, \{x_3\}, \{x_6\}, \{x_5\})$. The edges of $CDG(\mathbf{y}^1, \mathbf{y}^2)$ describe the individual transfers needed to change C^1 into C^2 .

receive or give away some item of X and its size constraints will still be satisfied. Similarly, we say that c_i is saturated if $\kappa_i^- < |C_i^1| = \kappa_i^+$, that c_i is depleted if $\kappa_i^- = |C_i^1| < \kappa_i^+$, and that c_i is fixed if $\kappa_i^- = |C_i^1| = \kappa_i^+$. Finally, we say that a directed graph D is a valid CDG at \mathbf{y}^1 if there exists a vertex $\mathbf{y}^i \in PP(\kappa^{\pm})$ such that $D = CDG(\mathbf{y}^1, \mathbf{y}^i)$. The following lemma characterizes the edges of $PP(\kappa^{\pm})$.

Lemma 3. Let $\mathbf{y}^1, \mathbf{y}^2$ be a pair of vertices in $PP(\kappa^{\pm})$. Then \mathbf{y}^1 and \mathbf{y}^2 share an edge in $PP(\kappa^{\pm})$ if and only if $CDG(\mathbf{y}^1, \mathbf{y}^2)$ cannot be non-trivially decomposed into valid CDGs at \mathbf{y}^1 . Equivalently, \mathbf{y}^1 and \mathbf{y}^2 share an edge if and only if $CDG(\mathbf{y}^1, \mathbf{y}^2)$ is a single edge, a single directed path in which no interior vertices are free, or a single directed cycle in which at most one vertex is free.

Proof. For the forward direction, assume that \mathbf{y}^1 and \mathbf{y}^2 are joined by an edge in $PP(\kappa^{\pm})$ and suppose for the purpose of contradiction that $CDG(\mathbf{y}^1, \mathbf{y}^2)$ can be decomposed into valid CDGs at \mathbf{y}^1 : $CDG(\mathbf{y}^1, \mathbf{y}^3), ..., CDG(\mathbf{y}^1, \mathbf{y}^\ell)$. Since \mathbf{y}^1 and \mathbf{y}^2 share an edge, there exists a vector $f \in \mathbb{R}^{kn}$ such that $f^T\mathbf{y}^1 = f^T\mathbf{y}^2$ but $f^T\mathbf{v} > f^T\mathbf{y}^1$ for any other vertex \mathbf{v} of $PP(\kappa^{\pm})$. Specifically, it must hold that $f^T\mathbf{y}^i > f^T\mathbf{y}^1$ for $i = 3, ..., \ell$. However, note that the clustering of \mathbf{y}^2 can be derived from that of \mathbf{y}^1 by independent

However, note that the clustering of \mathbf{y}^2 can be derived from that of \mathbf{y}^1 by independent applications of the transfers given by each $CDG(\mathbf{y}^1, \mathbf{y}^i)$. In other words, we have $\mathbf{y}^2 - \mathbf{y}^1 = (\mathbf{y}^3 - \mathbf{y}^1) + \cdots + (\mathbf{y}^{\ell} - \mathbf{y}^1)$. Thus

$$f^{T}(\mathbf{y}^{2} - \mathbf{y}^{1}) = f^{T}(\mathbf{y}^{3} - \mathbf{y}^{1}) + \dots + f^{T}(\mathbf{y}^{\ell} - \mathbf{y}^{1}) > 0 + \dots + 0 = 0,$$

a contradiction.

Conversely, assume that $CDG(\mathbf{y}^1, \mathbf{y}^2)$ cannot be decomposed in such a manner. See Figure 8 for examples of possible structures for $CDG(\mathbf{y}^1, \mathbf{y}^2)$ and their implications. Note that if $CDG(\mathbf{y}^1, \mathbf{y}^2)$ were anything other than a single path or cycle, it could be decomposed into two valid CDGs at \mathbf{y}^1 by isolating a directed cycle or a maximal path from the remainder of the graph. Further, if $CDG(\mathbf{y}^1, \mathbf{y}^2)$ were a directed path with a free interior vertex c_i , it could be decomposed into two valid CDGs at \mathbf{y}^1 by splitting the graph at c_i (Figure 8a). Similarly, if $CDG(\mathbf{y}^1, \mathbf{y}^2)$ were a directed cycle with at least two free vertices, we could split $CDG(\mathbf{y}^1, \mathbf{y}^2)$ into two directed paths at these vertices in order to form two valid CDGs at \mathbf{y}^1 (Figure 8c). Hence, $CDG(\mathbf{y}^1, \mathbf{y}^2)$ must meet the specifications of the lemma (as in Figures 8b and 8d).

To show that $\mathbf{y}^1 = (\mathbf{y}_{11}^1, ..., \mathbf{y}_{kn}^1)^T$ and $\mathbf{y}^2 = (\mathbf{y}_{11}^2, ..., \mathbf{y}_{kn}^2)^T$ are joined by an edge in $PP(\kappa^{\pm})$, it suffices to find a vector $f \in \mathbb{R}^{kn}$ such that $f^T \mathbf{y}^1 = f^T \mathbf{y}^2 < f^T \mathbf{v}$ for any other



(a) A case where $CDG(\mathbf{y}^1, \mathbf{y}^2)$ can be decomposed by splitting the directed path at the free vertex c_3 . Hence, \mathbf{y}^1 and \mathbf{y}^2 do not share an edge in $PP(\kappa^{\pm})$.





(b) A case where $CDG(\mathbf{y}^1, \mathbf{y}^2)$ cannot be decomposed into valid CDGs – any decomposition contains a directed c_i, c_j -path in which either c_i is depleted/fixed or c_j is saturated/fixed. Thus, \mathbf{y}^1 and \mathbf{y}^2 share an edge in $PP(\kappa^{\pm})$.



(c) A case where $CDG(\mathbf{y}^1, \mathbf{y}^2)$ can be decomposed by splitting the cycle at the free vertices c_1 and c_3 . So \mathbf{y}^1 and \mathbf{y}^2 must not share an edge in $PP(\kappa^{\pm})$.

(d) A case where $CDG(\mathbf{y}^1, \mathbf{y}^2)$ cannot be decomposed into valid CDGs by the same reasoning as in Figure 8b. So \mathbf{y}^1 and \mathbf{y}^2 share an edge in $PP(\kappa^{\pm})$.

Fig. 8: Structures for $CDG(\mathbf{y}^1, \mathbf{y}^2)$ that can and cannot be decomposed into valid CDG_s .

vertex $\mathbf{v} \in PP(\kappa^{\pm})$. Define such a vector $f = (f_{11}, ..., f_{kn})^T$ by setting

 $f_{ij} = \begin{cases} 0 & \text{if } x_j \in C_i^1 \cap C_i^2 \\ 0 & \text{if } c_i \text{ is fixed, free, or an endpoint, and } x_j \text{ is incident to } c_i \text{ in } CDG(\mathbf{y}^1, \mathbf{y}^2) \\ -1 & \text{if } c_i \text{ is a saturated non-endpoint, and } x_j \text{ is incident to } c_i \text{ in } CDG(\mathbf{y}^1, \mathbf{y}^2) \\ 1 & \text{if } c_i \text{ is a depleted non-endpoint, and } x_j \text{ is incident to } c_i \text{ in } CDG(\mathbf{y}^1, \mathbf{y}^2) \\ 2n & \text{otherwise.} \end{cases}$

Hence, if α denotes the number of non-endpoint saturated vertices in the path or cycle of $CDG(\mathbf{y}^1, \mathbf{y}^2)$ and β denotes the number of non-endpoint depleted vertices in this component, we have $f^T \mathbf{y}^1 = f^T \mathbf{y}^2 = \beta - \alpha$.

Let \mathbf{v} be any other vertex of $PP(\kappa^{\pm})$ and let $C^v = (C_1^v, ..., C_k^v)$ denote its corresponding clustering. If $CDG(\mathbf{y}^1, \mathbf{v})$ contains any edge (c_i, c_j) not found in $CDG(\mathbf{y}^1, \mathbf{y}^2)$, then if x_ℓ is the label of this edge, we have $f_{j\ell} = 2n$ and $\mathbf{v}_{j\ell} = 1$. Thus, since \mathbf{v} has exactly n nonzero components, we obtain $f^T \mathbf{v} > n \ge f^T \mathbf{y}^1$.

Therefore, we may assume that $CDG(\mathbf{y}^1, \mathbf{v})$ is a subgraph of $CDG(\mathbf{y}^1, \mathbf{y}^2)$. Given that \mathbf{v} is not equal to \mathbf{y}^1 or \mathbf{y}^2 , it follows that $CDG(\mathbf{y}^1, \mathbf{v})$ is a nontrivial proper subgraph of $CDG(\mathbf{y}^1, \mathbf{y}^2)$ and hence must be a collection of disjoint directed paths. Assume first that $CDG(\mathbf{y}^1, \mathbf{v})$ is a single directed c_i, c_j -path for some pair of vertices c_i, c_j . Then either c_i is a saturated non-endpoint of $CDG(\mathbf{y}^1, \mathbf{y}^2)$ or c_j is a depleted non-endpoint of $CDG(\mathbf{y}^1, \mathbf{y}^2)$. In the former case, note that since $|C_i^v| < |C_i^1|$, we have $f^T \mathbf{v} \ge \beta - (\alpha - 1) > f^T \mathbf{y}^1$. In the latter case, since $|C_j^v| > |C_j^1|$, we have $f^T \mathbf{v} \ge (\beta + 1) - \alpha > f^T \mathbf{y}^1$.

If $CDG(\mathbf{y}^1, \mathbf{v})$ is a collection of directed paths, then we can decompose it into valid clustering difference graphs $CDG(\mathbf{y}^1, \mathbf{y}^3), ..., CDG(\mathbf{y}^1, \mathbf{y}^\ell)$ at \mathbf{y}^1 where each consists of a

single directed path. Then, as before, it holds that $f^T \mathbf{y}^i > f^T \mathbf{y}^1$ for $i = 3, ..., \ell$. This implies

$$f^{T}(\mathbf{v} - \mathbf{y}^{1}) = f^{T}(\mathbf{y}^{3} - \mathbf{y}^{1}) + \dots + f^{T}(\mathbf{y}^{\ell} - \mathbf{y}^{1}) > 0 + \dots + 0 = 0$$

as desired.

The circuits of $PP(\kappa^{\pm})$ have a significantly simpler characterization than the edges: Two vertices of $PP(\kappa^{\pm})$ are joined by a circuit step if and only if the corresponding clustering difference graph is a directed path or cycle.

Lemma 4. The circuits of $PP(\kappa^{\pm})$ consist of those $\mathbf{g} \in \{0, 1, -1\}^{kn}$ that describe a single cyclical exchange or sequential movement of items among the clusters.

Proof. By Lemma 2, a circuit \mathbf{g} of $PP(\kappa^{\pm})$ satisfies $\mathbf{g} \in \{0, 1, -1\}^{kn}$. Furthermore, we have $\sum_{i=1}^{k} \mathbf{g}_{ij} = 0$ for j = 1, ..., n, implying that \mathbf{g} describes some set of transfers among a clustering of X – an entry $\mathbf{g}_{ij} = 1$ implies that x_j is added to cluster C_i , and $\mathbf{g}_{ij} = -1$ implies that x_j is removed from C_i . The inequality constraints $B\mathbf{y} \leq \mathbf{d}$ for this polytope consist of non-negativity constraints and cluster size constraints. Hence, the support of any $B\mathbf{g}$ consists of the support of \mathbf{g} along with the indices of any clusters whose sizes are changed by the transfers of \mathbf{g} . It follows that $B\mathbf{g}$ is support-minimal over all such transfers if and only if no subset of the cluster size changes implied by \mathbf{g} can be achieved by a proper subset of the transfers of \mathbf{g} .

Suppose that \mathbf{g} describes a single cyclical exchange of items. Then no cluster sizes are changed when applying the transfers of \mathbf{g} , but applying any nontrivial subset of these transfers results in at least two cluster size changes. Hence, \mathbf{g} is a circuit of $PP(\kappa^{\pm})$. Similarly, if \mathbf{g} describes a single sequential movement of items among the clusters (i.e. the *CDG* implied by the transfers of \mathbf{g} consists of a single directed path), then only two cluster sizes are changed by the transfers of \mathbf{g} . Any nontrivial subset of these transfers necessarily changes the size of a third cluster. Hence, \mathbf{g} is again a circuit of $PP(\kappa^{\pm})$.

Conversely, suppose that \mathbf{g} does not describe a single cyclical exchange or sequential movement, and let D be a CDG whose transfers are described by \mathbf{g} . If D contains a directed cycle as a subgraph, the transfers given by this cycle are a proper subset of those given by \mathbf{g} that result in no cluster size changes. Hence, \mathbf{g} must not be a circuit. If D is acyclic, D must properly contain a maximal directed path D'. The only two clusters whose sizes are changed as a result of the transfers of D' correspond to the two endpoints of D'. By the maximality of D', the sizes of these two clusters are also changed by the transfers of \mathbf{g} . Hence, \mathbf{g} again must not be a circuit of $PP(\kappa^{\pm})$.

By Corollary 1, we know that all circuit walks in $PP(\kappa^{\pm})$ are vertex walks. However, Lemmas 3 and 4 highlight the differences between edges and circuits in $PP(\kappa^{\pm})$ and show that its circuit walks can have much more general behavior than its edge walks.

5.4 Fixed-size Partition Polytopes

As a special class of transportation polytopes introduced in [5], the fixed-size partition polytope $PP(\kappa)$ is associated with the partitioning of a set $X = \{x_1, ..., x_n\}$ of items into clusters $C_1, ..., C_k$ where each cluster C_i has prescribed size $\kappa_i \in \mathbb{Z}_+$. Note that the wellknown Birkhoff polytope is an instance of this polytope for k = n and $\kappa_i = 1$ for i = 1, ..., n. Further, $PP(\kappa)$ is equivalent to the bounded-size partition polytope $PP(\kappa^{\pm})$ of Section 5.3 when $\kappa_i^- = \kappa_i^+$ for i = 1, ..., k. However, we show here that $PP(\kappa)$ has more restrictive circuit walk behavior than $PP(\kappa^{\pm})$.

For i = 1, ..., k and j = 1, ..., n, let y_{ij} be a binary variable indicating whether or not item x_j is assigned to cluster C_i . Then $PP(\kappa)$ is the 0/1-polytope defined by the following system of constraints:

$$\sum_{j=1}^{n} y_{ij} = \kappa_i \quad i = 1, ..., k$$
$$\sum_{i=1}^{k} y_{ij} = 1 \quad j = 1, ..., n$$
$$y_{ij} \ge 0 \quad i = 1, ..., k, \ j = 1, ..., n$$

As in Section 5.3, the vertices of $PP(\kappa)$ consist of all feasible clustering assignments $\mathbf{y} \in \{0,1\}^{kn}$. Given two such assignments $\mathbf{y}^1, \mathbf{y}^2$, recall the definition of the *clustering* difference graph $CDG(\mathbf{y}^1, \mathbf{y}^2)$ from \mathbf{y}^1 to \mathbf{y}^2 . It is shown in [5] that \mathbf{y}^1 and \mathbf{y}^2 are adjacent in $PP(\kappa)$ if and only if $CDG(\mathbf{y}^1, \mathbf{y}^2)$ consists of a single directed cycle. This characterization yields useful bounds on the combinatorial diameter of $PP(\kappa)$.

We now characterize the circuits of $PP(\kappa)$. Since it is an instance of the bounded-size partition polytope, a circuit **g** of $PP(\kappa)$ must satisfy the condition of Lemma 4: **g** describes either a cyclical exchange or a sequential movement of items among the underlying clusters. However, **g** must also satisfy $\sum_{j=1}^{n} \mathbf{g}_{ij} = 0$ for i = 1, ..., k; that is, the set of transfers described by **g** cannot change the size of any cluster. Therefore, **g** is a circuit of $PP(\kappa)$ if and only if **g** describes a cyclical exchange of items.

It follows that $PP(\kappa)$ is ECW. If \mathbf{y}^1 is a vertex of $PP(\kappa)$ and \mathbf{g} is a feasible circuit direction at \mathbf{y} , taking a maximal step in the direction of \mathbf{g} corresponds to applying a single cyclical exchange of items. Hence, the resulting vertex \mathbf{y}^2 yields a clustering difference graph $CDG(\mathbf{y}^1, \mathbf{y}^2)$ consisting of a single directed cycle, implying that \mathbf{y}^1 and \mathbf{y}^2 indeed share an edge in $PP(\kappa)$.

6 Proof of Theorems 5 to 7

In this section we prove three characterizations of simple ECW polytopes. Recall the definitions of elementary arrangements, elementary cones, and inner cones from Section 2.3. Without loss of generality, consider a full-dimensional polyhedron $P = \{\mathbf{x} \in \mathbb{R}^n : B\mathbf{x} \leq \mathbf{d}\}$ given by a minimal representation. (Note that any polyhedron $P = \{\mathbf{x} \in \mathbb{R}^n : A\mathbf{x} = \mathbf{b}, B\mathbf{x} \leq \mathbf{d}\}$ can be expressed in this form with dimension $n = n' - \operatorname{rank}(A)$ by using the equality constraints to reduce the number of variables.) Recall that although the circuits of a polyhedron P are determined by its constraint system, a minimal representation ensures that each constraint appears as a facet in P, allowing us to characterize the set of circuits of Pvia its geometric properties. Our first observation is that elementary cones are generated by circuits.

Lemma 5. Let $P = {\mathbf{x} \in \mathbb{R}^n : B\mathbf{x} \leq \mathbf{d}}$ be full-dimensional polyhedron. A pointed cone formed by the elementary arrangement of P is generated by circuits of P. Conversely, each circuit of P is the intersection of n-1 hyperplanes from the elementary arrangement.

Proof. Let C be a cone from the elementary arrangement of P; i.e., C can be represented as $C = \{\mathbf{x} \in \mathbb{R}^n : B'\mathbf{x} \leq \mathbf{0}\}$, where B' is a row-submatrix of B (with some rows possibly scaled by -1). Since an extreme ray of C is formed by the intersection of n-1 facets from the system $B'\mathbf{x} \leq \mathbf{0}$, it follows from Lemma 1 that all such extreme rays are circuits of P.

Conversely, if **g** is a circuit of P, Lemma 1 yields a row-submatrix B' of B with $\operatorname{rank}(B') = n - 1$ such that $B'\mathbf{g} = \mathbf{0}$. A set of n - 1 linearly independent rows from B' then corresponds to a set of hyperplanes from the elementary arrangement whose intersection contains **g**.

Note that if $C = {\mathbf{x} \in \mathbb{R}^n : D\mathbf{x} \leq \mathbf{0}}$ is an elementary cone of P generated by circuits ${\mathbf{g}_1, ..., \mathbf{g}_k}$, its opposite $-C = {\mathbf{x} \in \mathbb{R}^n : D\mathbf{x} \geq \mathbf{0}}$ is also an elementary cone of P generated by circuits ${-\mathbf{g}_1, ..., -\mathbf{g}_k}$. Theorem 5 relates the inner cones of a simple ECW polytope to these elementary cones.

Theorem 5 (Elementary Cone Condition) Let $P = {\mathbf{x} \in \mathbb{R}^n : B\mathbf{x} \leq \mathbf{d}}$ be a fulldimensional, simple polytope. All circuit walks in P are edge walks if and only if for each vertex $\mathbf{v} \in P$, the inner cone $I(\mathbf{v})$ is an elementary cone of P.

Proof. Suppose first P is ECW and let \mathbf{v} be a vertex of P. The inner cone $I(\mathbf{v})$ is generated by the n circuits of P corresponding to the n edge directions incident to \mathbf{v} . If $I(\mathbf{v})$ is not an elementary cone, there exists an elementary cone C of P strictly contained in $I(\mathbf{v})$. By Lemma 5, C is generated by at least n circuits of P. At least one of these circuits is different from the n circuits generating $I(\mathbf{v})$. However, this implies that $I(\mathbf{v})$ contains a circuit that is not an edge direction incident to \mathbf{v} . Since P is bounded, this contradicts the fact that Pis ECW.

Conversely, suppose P is not ECW. Then for some vertex $\mathbf{v} \in P$, the inner cone I(v) contains a circuit \mathbf{g} in addition to the n circuits which generate I(v). According to Lemma 5, \mathbf{g} is generated by n-1 hyperplanes H_1, \ldots, H_{n-1} from the elementary arrangement of P. Suppose that none of these hyperplanes intersect the interior of I(v) – i.e., suppose that $I(v) \cap H_i$ is a face of I(v) for $i = 1, \ldots, n-1$. This implies that the intersection $I(v) \cap H_1 \cap \cdots \cap H_{n-1}$ is also a face of I(v). However, this intersection must in fact be generated by \mathbf{g} , contradicting the fact that \mathbf{g} is not an edge direction of I(v). Therefore, one of the hyperplanes H_1, \ldots, H_{n-1} must intersect the interior of I(v), implying that I(v) is not an elementary cone.

Theorem 5 is a quite straightforward characterization of simple ECW polytopes. We use it to prove a more descriptive characterization which we call the symmetric inner cone condition. First, we show that this condition is a necessary property of any ECW polytope. Recall that given a pair of vertices \mathbf{u}, \mathbf{v} of a polyhedron P, we let P^{uv} denote the minimal face of P containing \mathbf{u} and \mathbf{v} and let $I^{uv}(\mathbf{u}), I^{uv}(\mathbf{v})$ denote the inner cones of \mathbf{u}, \mathbf{v} with respect to P^{uv} .

Lemma 6. Let $P = {\mathbf{x} \in \mathbb{R}^n : B\mathbf{x} \leq \mathbf{d}}$ be a full-dimensional, simple polytope whose only circuit walks are edge walks. Then $I^{uv}(\mathbf{u}) = -I^{uv}(\mathbf{v})$ for all pairs of vertices \mathbf{u}, \mathbf{v} in P.

Proof. Let \mathbf{u}, \mathbf{v} be a pair of vertices in P, and let $d := \dim(P^{uv})$. If d = 1 and \mathbf{u} shares an edge with \mathbf{v} in P, the result is trivial, so assume that $d \ge 2$ and that \mathbf{u}, \mathbf{v} are not adjacent.

Note that the direction $\mathbf{v} - \mathbf{u}$ belongs to the inner cone $I^{uv}(\mathbf{u})$ and that its opposite $\mathbf{u} - \mathbf{v}$ belongs to $I^{uv}(\mathbf{v})$. By the definition of P^{uv} , both of these directions belong to the strict interiors of their respective cones, implying that the interior of $I^{uv}(\mathbf{u})$ intersects the interior of $-I^{uv}(\mathbf{v})$. By Theorem 5, $I(\mathbf{u})$ and $I(\mathbf{v})$ are elementary cones of P. Hence, $I^{uv}(\mathbf{u})$ and $I^{uv}(\mathbf{v})$ are elementary cones of P. Hence, $I^{uv}(\mathbf{u}) = -I^{uv}(\mathbf{v})$.

To show that the symmetric inner cone condition of Lemma 6 is also a sufficient condition for a polytope to be ECW, first suppose that P satisfies this condition while containing a pair of vertices sharing no facets. It then must hold that P is a parallelotope, immediately implying that all of its circuit walks are edge walks.

Lemma 7. Let P be an n-dimensional, simple polyhedron which satisfies $I^{uv}(\mathbf{u}) = -I^{uv}(\mathbf{v})$ for all pairs of vertices \mathbf{u}, \mathbf{v} in P. If P contains a pair of vertices that shares no facets, then P is an n-parallelotope.

Proof. The statement is straightforward for $n \leq 2$, so assume $n \geq 3$. Let \mathbf{u}, \mathbf{v} be a pair of vertices in P that shares no facets. Hence, $I(\mathbf{v}) = -I(\mathbf{u})$. Note that this immediately implies that P is a polytope since any extreme ray of P would have to belong to the two n-dimensional cones $I(\mathbf{u})$ and $-I(\mathbf{u})$. Furthermore, the n facets containing \mathbf{u} are parallel to the n facets containing \mathbf{v} . Let \mathcal{F} denote this set of 2n facets which form an n-parallelotope Q. Unless P contains a facet outside of \mathcal{F} , we have P = Q.

So suppose that P contains facets outside of \mathcal{F} . Some such facet F contains a vertex \mathbf{w} which is a neighbor of some vertex from Q. Such a vertex \mathbf{w} must not also be a vertex of Q itself, else it would be a degenerate vertex in P. Hence, \mathbf{w} is formed by the intersection of F with an edge e of Q, cutting off some vertex $\mathbf{y} \in Q$ from P. Note that if e is incident to \mathbf{u} , then \mathbf{w} shares no facets with \mathbf{v} and by assumption $I(\mathbf{w}) = -I(\mathbf{v})$. However, this then implies $I(\mathbf{w}) = I(\mathbf{u})$, a contradiction. Hence, \mathbf{y} must not be a neighbor of \mathbf{u} . Similarly, \mathbf{y} must not be a neighbor of \mathbf{v} .

Now, let $F \notin \mathcal{F}$ be such a facet in P that cuts off a vertex $\mathbf{y} \in Q$ sharing the most facets with \mathbf{u} in Q, and let k denote the number of facets shared by \mathbf{y} and \mathbf{u} in Q. Since \mathbf{y} must not be adjacent to \mathbf{u} in Q, we have $k \leq n-2$. We will show that there then exist three vertices of P from Q which share more facets with \mathbf{u} than \mathbf{y} in Q such that \mathbf{y} completes a 2-parallelotope with these three vertices. In order for P to satisfy the symmetric inner cone condition, it must follow that $\mathbf{y} \in P$, a contradiction.

In particular, let $F_1, ..., F_n$ denote the facets of Q incident to \mathbf{u} and $G_1, ..., G_n$ denote the facets of Q incident to \mathbf{v} . Assume $F_1, ..., F_k, G_{k+1}, ..., G_n$ are the facets incident to \mathbf{y} in Q. As Q is a parallelotope, the point \mathbf{x}_1 formed by the intersection of facets $F_1, ..., F_{k+1}, G_{k+2}, ..., G_n$ is a vertex of Q. Since \mathbf{x}_1 shares more than k facets with \mathbf{u} , it is not cut off by any facet outside of \mathcal{F} and is also a vertex of P. Similarly, the point \mathbf{x}_2 formed by $F_1, ..., F_{k+2}, G_{k+3}, ..., G_n$ and the point \mathbf{x}_3 formed by $F_1, ..., F_k, G_{k+1}, F_{k+2}, G_{k+3}, ..., G_n$ are vertices of P.

However, consider the two-dimensional face P' of P formed by the intersection of facets $F_1, ..., F_k, G_{k+3}, ..., G_n$. It holds that $\mathbf{x}_1, \mathbf{x}_2, \mathbf{x}_3$ are vertices of P'. Further, vertices \mathbf{x}_1 and \mathbf{x}_3 of P' share no facets in P', so in order for the symmetric inner cone condition to be satisfied, P' has to be a 2-parallelotope. The vertex opposite of \mathbf{x}_2 in P' must then be \mathbf{y} , but this contradicts $\mathbf{y} \notin P$. Therefore, no such facet F exists in P, implying that all facets of P belong to \mathcal{F} and thus P = Q.

Next, we prove that if a polytope P satisfies the symmetric inner cone condition of Lemma 6 but does not necessarily contain a pair of vertices sharing no facets as in Lemma 7, then P must be a highly symmetric generalization of the parallelotope: the (n, d)-parallelotope. Recall Definition 2 and the surrounding discussion in Section 2.3. If k denotes the minimum number of facets shared by any pair of vertices in P, we show that P must be an (n, n - k)-parallelotope.

Lemma 8. Let P be an n-dimensional, simple polytope that satisfies $I^{uv}(\mathbf{u}) = -I^{uv}(\mathbf{v})$ for all pairs of vertices \mathbf{u}, \mathbf{v} in P. Then P is an (n, n-k)-parallelotope, where k is the minimum number of facets shared by any pair of vertices in P.

Proof. If k = 0, Lemma 7 implies that P is a parallelotope, so assume $k \ge 1$ and let \mathbf{u}, \mathbf{v} be a pair of vertices in P that shares exactly k facets. Note that P^{uv} is the intersection of the k facets shared by \mathbf{u} and \mathbf{v} . Hence, P^{uv} is an (n - k)-dimensional polytope satisfying the symmetric inner cone condition in which \mathbf{u} and \mathbf{v} share no facets. By Lemma 7, P^{uv} is an (n - k)-parallelotope.

Next, note that P has at least 2n - k facets: the k facets shared by \mathbf{u} and \mathbf{v} , the n - k facets containing \mathbf{u} but not containing \mathbf{v} , and the n - k facets containing \mathbf{v} but not \mathbf{u} . Let \mathcal{F} denote this set of 2n - k facets. By the structure of P^{uv} , each vertex of P^{uv} is the intersection of n of these facets. In fact, we show that these are the only facets of P.

First, suppose that P contains some facet $F \notin \mathcal{F}$ that intersects one of the edges of P that leave P^{uv} . This intersection forms a vertex \mathbf{w} that shares an edge with some vertex $\mathbf{u}' \in P^{uv}$. Since P^{uv} is a parallelotope, there exists a vertex $\mathbf{v}' \in P^{uv}$ that shares no facets with \mathbf{u}' in P^{uv} . Thus, the only facets shared by \mathbf{u}' and \mathbf{v}' in P are the k facets forming P^{uv} . However, since \mathbf{v}' must not be contained in F, this implies that \mathbf{w} and \mathbf{v}' share only k-1 facets in P, a contradiction with the choice of k.

Therefore, no facet outside of \mathcal{F} intersects any of the edges leaving P^{uv} in P. Hence, since P is bounded, every edge that leaves P^{uv} hits some facet of \mathcal{F} . Additionally, the vertex \mathbf{w} formed by this intersection shares exactly k facets with some vertex of the (n-k)parallelotope P^{uv} . Namely, if \mathbf{u}' again denotes the neighbor of \mathbf{w} in P^{uv} and \mathbf{v}' is the vertex of P^{uv} sharing exactly k facets with \mathbf{u}' in P, then \mathbf{w} also shares exactly k facets with \mathbf{v}' in P: k-1 of the facets forming P^{uv} and one facet incident to \mathbf{v}' but not \mathbf{u}' in P. Thus, the face $P^{wv'}$ of P is an (n-k)-parallelotope formed by the facets of \mathcal{F} which contains the vertex \mathbf{w} .

Proceeding inductively on combinatorial distance from P^{uv} , we see that all vertices of P belong to some (n-k)-parallelotope face of P formed by the facets of \mathcal{F} . Therefore, the only facets of P are those of \mathcal{F} . It follows that P is an (n, n-k)-parallelotope. \Box

An *n*-parallelotope P given by a minimal representation has only *n* circuit directions: the directions of its *n* classes of parallel edges. Hence, it is quite clear that P is ECW. We show in the following lemma that this result generalizes to (n, d)-parallelotopes.

Lemma 9. All circuit walks in an (n, d)-parallelotope given by a minimal representation are edge walks.

Proof. Let P be an (n, d)-parallelotope given by a minimal representation. By Theorem 5, it suffices to show that the inner cone of each vertex in P is an elementary cone. Thus, suppose for the purpose of contradiction that the inner cone of a vertex $\mathbf{v} \in P$ is not an elementary cone. Then there exists a facet F of P with corresponding inequality $\mathbf{b}^T \mathbf{x} \leq \delta$

such that the parallel hyperplane $H_0 = \{ \mathbf{x} \in \mathbb{R}^n : \mathbf{b}^T \mathbf{x} = \mathbf{0} \}$ divides the inner cone $I(\mathbf{v})$ into two *n*-dimensional cones. In particular, an edge of $I(\mathbf{v})$ leaves H_0 on either side of H_0 . If this were not the case, the corresponding hyperplanes of all facets of P would intersect $I(\mathbf{v})$ within a proper face of $I(\mathbf{v})$, implying that $I(\mathbf{v})$ is an elementary cone.

Therefore, consider the hyperplane $H = {\mathbf{x} \in \mathbb{R}^n : \mathbf{b}^T \mathbf{x} = \mathbf{b}^T \mathbf{v}}$ which is parallel to Fand incident to \mathbf{v} . Then there exist edges incident to \mathbf{v} in P that leave H on either side of H. Namely, since P is simple, there exist facets F_1 and F_2 incident to \mathbf{v} such that the edge e_1 leaving F_1 at \mathbf{v} leads to a vertex \mathbf{z}_1 satisfying $\mathbf{b}^T \mathbf{z}_1 < \mathbf{b}^T \mathbf{v}$, and the edge e_2 leaving F_2 at \mathbf{v} leads to a vertex $\mathbf{z}_2 > \mathbf{b}^T \mathbf{v}$.

Since P is an (n, d)-parallelotope, **v** belongs to a d-parallelotope face of P and there exists a vertex **u** in this face sharing exactly n - d facets with **v**. Further, since $\mathbf{v} \notin F$ and P has only n + d facets, we must have $\mathbf{u} \in F$.

Now suppose **u** belongs to neither F_1 nor F_2 . Then the edges e_1 and e_2 must be two of the d edges incident to **v** in P^{uv} since F_1 and F_2 are not among the n-d facets shared between **u** and **v**. We will say that an edge with direction **e** is parallel to a facet with normal **b** if and only if $\mathbf{b}^T \mathbf{e} = 0$. Hence, neither of the edges e_1 and e_2 are parallel to F. However, in order to satisfy the symmetric inner cone condition $I^{uv}(\mathbf{v}) = -I^{uv}(\mathbf{u})$, there must exist a pair of edges incident to **u** in P^{uv} which are parallel to e_1 and e_2 . This contradicts the fact that since P is simple, only one of the n edges incident to **u** is not parallel to F.

Therefore, **u** must belong to at least one of F_1 and F_2 . If **u** belongs to both F_1 and F_2 , we may take a step along the edge incident to **u** that leaves F_2 to reach a new vertex in F_1 sharing exactly n - d facets with **v**. Hence, there always exists a vertex sharing n - dfacets with **v** that is incident to precisely one of F_1 and F_2 . Without loss of generality we will assume $\mathbf{u} \in F_1$ and $\mathbf{u} \notin F_2$.

There exists an edge incident to **u** that leaves F_1 and intersects some facet G of P at a vertex **w**. Recall that $\mathbf{u} \in F$, so since the edge between **u** and **w** does not leave F, we also have $\mathbf{w} \in F$. As in the proof of Lemma 8, **w** shares exactly n - d facets with **v** in P. Hence, if G is not F_2 , it holds that **w** is a vertex in F belonging to neither F_1 nor F_2 , and we again obtain the above contradiction. Thus, we may assume $G = F_2$ and therefore $\mathbf{w} \in F_2$.

Since **v** shares exactly n-d facets with **w** in the (n, d)-parallelotope P, the face P^{wv} is a d-parallelotope. Because $\mathbf{w} \notin F_1$, the edge e_1 incident to **v** is contained in P^{wv} . Furthermore, since $\mathbf{w} \in F$ while $\mathbf{v} \notin F$, it holds that $P^{wv} \cap F$ is a facet of P^{uv} . Note that in a parallelotope, the only edges that are not parallel to a given facet must intersect that facet. The edge e_1 is not parallel to F, so it must not be parallel to any of its lower dimensional faces. Thus, e_1 is not parallel to the facet $P^{wv} \cap F$ of P^{wv} , implying that e_1 intersects $P^{wv} \cap F$. This yields $\mathbf{z}_1 \in F$.

Similarly, if we consider the edge e_2 in the *d*-parallelotope P^{uv} , we see that $\mathbf{z}_2 \in F$. However, this would imply that $\mathbf{b}^T \mathbf{v} > \mathbf{b}^T \mathbf{z}_1 = \delta = \mathbf{b}^T \mathbf{z}_2 > \mathbf{b}^T \mathbf{v}$, a contradiction. \Box

Theorems 6 and 7 now follow directly from Lemmas 6, 8 and 9. If a simple polytope is ECW, then the symmetric inner cone condition must be satisfied, implying that the polytope is an (n, d)-parallelotope. Conversely, any simple polytope that satisfies the symmetric inner cone must be an (n, d)-parallelotope, which then implies the ECW property if the polytope is given by a minimal representation.

Acknowledgments

Borgwardt gratefully acknowledges support through an ORS Large Grant at the University of Colorado Denver and the Collaboration Grant for Mathematicians "Polyhedral Theory in Data Analytics" of the Simons Foundation.

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