



Internal Note/ITS

ALICE reference number

ALICE-INT-2002-15 1.0

Institute reference number

Date of last change

2002-05-27

Device Simulation of the ALICE Silicon Drift Detector.

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Abstract:

In this report we present the work of simulation that has been carried out to determine and refine the design of the ALICE Silicon Drift Detector. The simulation phase is fundamental to get a full comprehension of the device, and as a consequence, it allows the designer to reduce the R&D times and costs.

First we provide a general description of the detector as it is in its final design. Then we give a detailed description of the simulations performed in each part of the device, namely: drift region, collection zone, guard region, charge injectors.

1 General detector description.

The ALICE silicon drift detector [1] is a symmetrical structure. The electrons drift from the central p^+ cathode towards two opposite linear arrays of n^+ anodes. Even though the silicon pad containing the detector is cut from the wafer as a rectangle with an area of $87.6 \times 72.5 \text{ mm}^2$, the detector itself has a hexagonal shape with a rectangular sensitive area. The main parts of the detector are:

Drift region. It is composed by 292 cathodes per half-detector, having a pitch of $120 \mu\text{m}$. The resulting length of the sensitive area of the detector is 70.0 mm .

Collection zone. It consists of 256 anode pads with a pitch of $294 \mu\text{m}$. The width of the sensitive area results 75.3 mm . The collection zone is completed by 3 cathodes with specific functions: the *grid cathode* on the n -side separates anodes one from another, while two *kick up cathodes* on the p -side force the drifting charge towards the anodes array.

Guard region. Aside the drift region, there are two triangular areas constituted by the guard p^+ cathodes. There is one guard cathode every two drift cathodes, so, the potential difference between adjacent guards is twice that between adjacent drift strips. The pitch of the guard cathodes is $32 \mu\text{m}$.

MOS injectors. To monitor the drift velocity across the sensitive area, and to calibrate the drift time for temperature variations, 'point-like' MOS charge injectors are implemented [2]. In each half-detector three arrays of injectors are realized on both n - and p -side at distances of 3 mm , 17.6 mm and 34.0 mm from the anodes. The injector pitch is 2.35 mm (every eight anodes).

The whole system of cathodes is biased with an integrated divider accommodated in two columns between the drift region and the two guard regions.

2 The simulator.

The simulations are carried out with ATLAS Device Simulator [3], produced by Silvaco International. It is a 2D simulator, thus, it is important to select properly a device region in which the variations of the quantities to be simulated are negligible in the third dimension. This is our case when considering cross sections orthogonal to the cathode strips. All the simulations are performed solving both the Poisson's equation and the carrier continuity equations. In this way it is possible to have a complete description of the system in terms of electrical quantities (potential and electric field distributions, carrier distributions, and

current densities).

The following paragraphs provide an exhaustive description of the simulations carried out for each of the above-mentioned regions.

3 Drift region.

The electric field needed to drift the electron cloud is imposed by a suitable bias of the drift cathodes. Each drift region of the ALICE detector consists of 291 cathodes having a width of $70\ \mu m$ and a pitch of $120\ \mu m$. The operation conditions for the ALICE SDD foresee a voltage difference of $8\ V$ between adjacent cathodes, which implies a drift field of about $670\ V/cm$.

The simulation of this region is necessary to verify the absence of ripples along the drift channel. The figure below shows the structure adopted for the simulations. It is a cross section of the 3D device along a plane perpendicular to the drift cathodes. In order to obtain a realistic result, the lateral boundaries must be kept far from the central region, where we expect the exact solution. For this reason we used a high number of cathodes (9), leading to a total length of about $1.5\ mm$ against a device depth of $0.3\ mm$. Moreover, the length of the first couple of cathodes on the left is extended to further prolong the left side. An anode is located at the right side in order to provide the bulk contact. Two results, extracted from the simulation of this structure, are depicted in figure 2. In the first

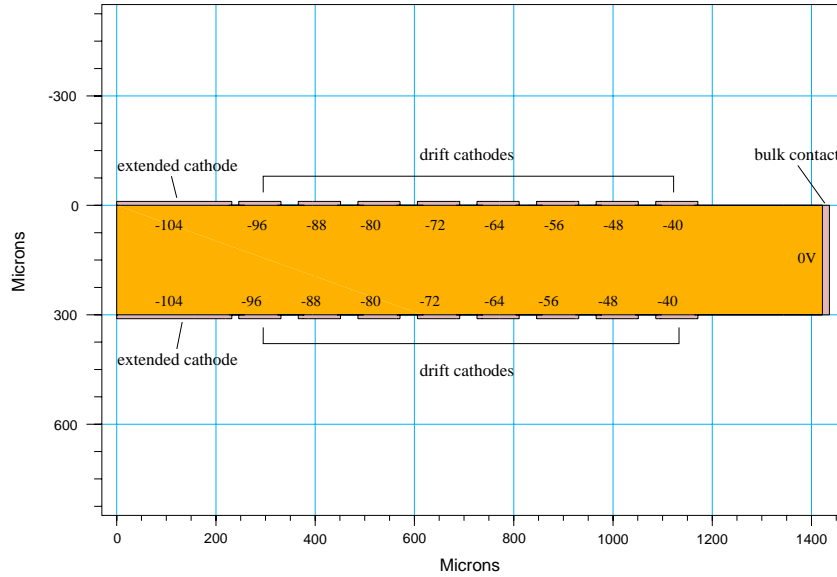


Figure 1: Structure adopted for the simulation of the drift region.

plot we see the behaviour of the potential along two lines parallel to the wafer surface: one is located in the middle of the wafer thickness, the other is just below the $Si - SiO_2$ interface. The second plot represents the potential profile along a line crossing the centre

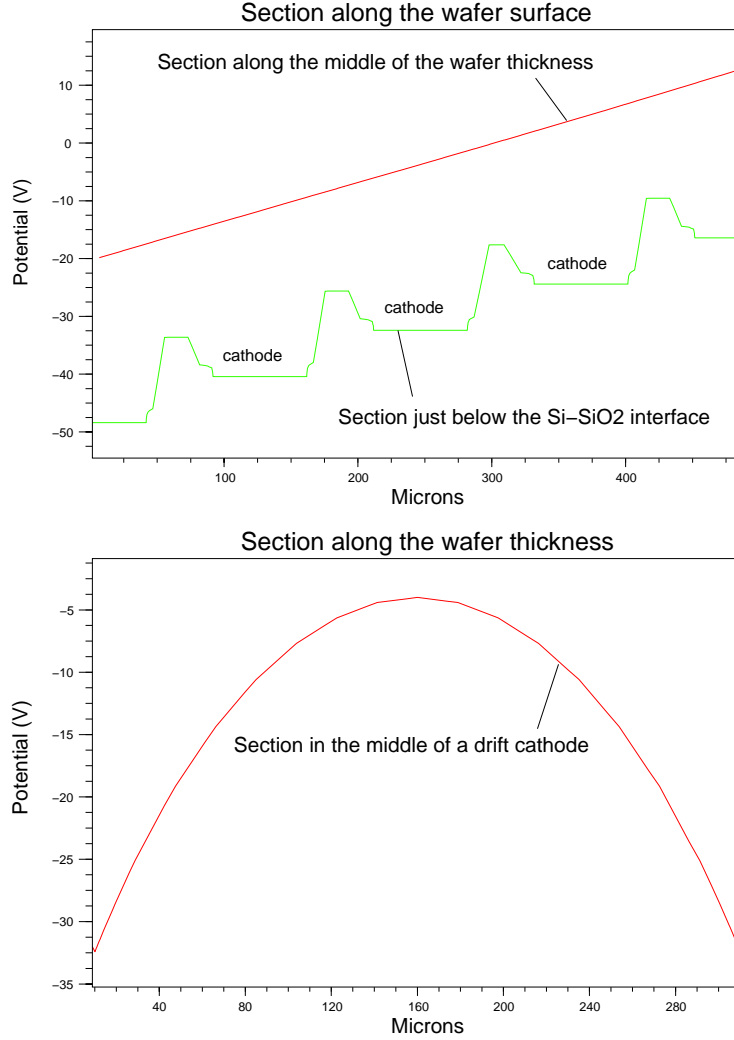


Figure 2: Simulated profile of the potential distribution in the drift region.

of two opposite cathodes, that is along the detector thickness. As expected for a $3k\Omega$ -silicon, the depth of the parabolic potential gutter is around 30 V . The relevant aspect is that the potential gradient along the drift direction, in the middle of the wafer, is perfectly linear.

The ALICE detector is a bi-directional structure, so, there is a change of the drift direction passing from one half of the detector to the other. In order to fulfil the requirement of a constant drift velocity, the slope of the potential gutter should change abruptly in

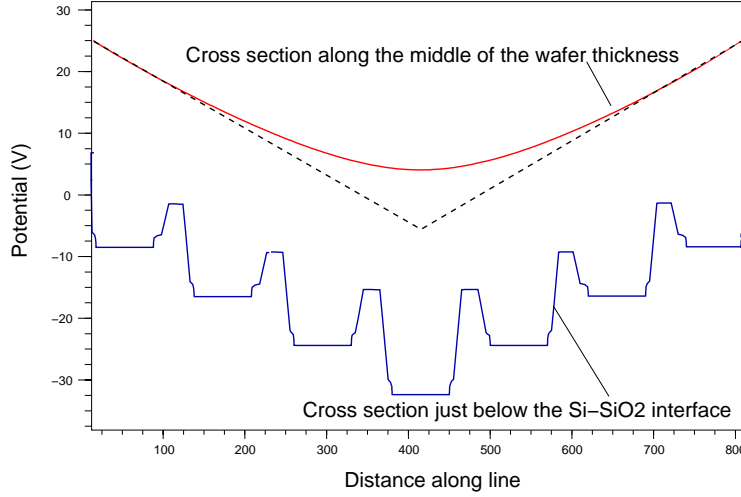


Figure 3: Simulation of the potential distribution at the top of the drift region.

correspondence of the most negative cathode. This condition is represented by the dashed line in figure 3. In reality, the simulation states that there is a non-linearity of the potential at the bottom of the gutter having an extension of about $400 \mu m$ per half. This introduces a systematic error to be accounted for. Furthermore, an eventual injector line should be placed beyond this region to prevent an erroneous calibration of the drift time.

4 Collection zone.

The collection zone is one of the critical regions in a SDD. Here the electron cloud is forced to move from the middle plane of the detector toward the anode array in the n-side. The forcing electric field is applied by properly biasing the last few cathodes in the proximity of the anodes. It is very important to simulate precisely the potential distribution because of the constraints we have to satisfy. First, we must avoid a trapping of the signal electrons under the oxide when approaching the surface. Second, we have to minimise the non-linearity of the drift speed associated with the transversal movement towards the n-side of the detector. Third, we have to guarantee a good potential separation between anodes and perimeter to avoid inefficiencies of the electron collection.

Figure 4 represents the structure used for the simulation of the collection zone of the ALICE detector. It is a cross section along a plane perpendicular to the drift cathodes and passing in the centre of an anode. As mentioned for the drift region, a crucial point for a good simulation is the length of the cell. Indeed, the solution at the boundaries must not alter the result in the region of interest.

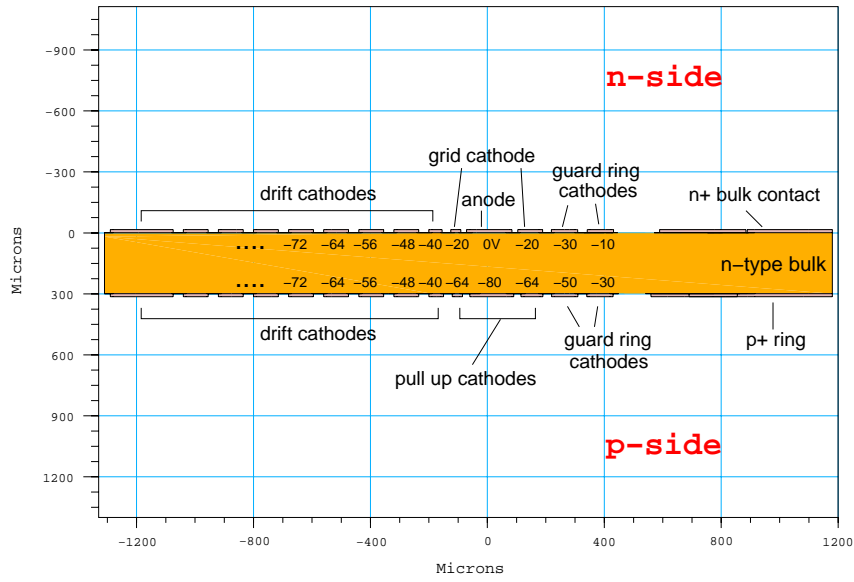


Figure 4: Structure adopted for the simulation of the collection zone.

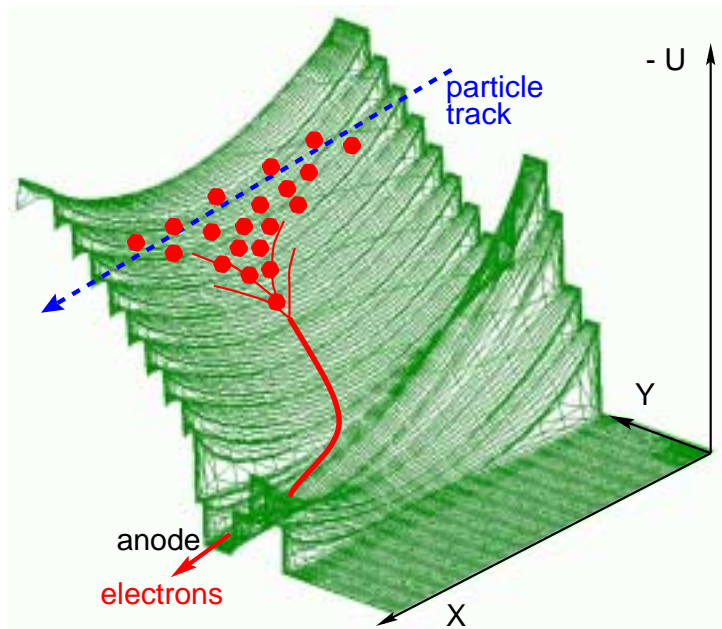


Figure 5: 3D view of the potential distribution in the collection zone.

From the sketch of figure 4, we note that the length of the region is 2.5 mm against a wafer thickness of 0.3 mm . This assures a correct solution in the collection region. Such a complicated structure requires a very high number of mesh points and as a consequence a long computational time.

After several simulations we found the appropriate bias scheme for this geometry. An artistic view of the potential distribution is depicted in figure 5. We can distinguish where the drift region is transformed in the collection zone. This kind of representation gives an idea on the principle of operation of a silicon drift chamber. In particular, we can appreciate the function of the collection zone that forces the electrons to move toward the anodes.

It is worthwhile noting that, in this design, we tried to minimise the extent of the collection zone. In standard linear SDDs, the last drift cathodes are biased in a way to shift the bottom of the potential gutter gradually to the n -side. The reason is to guide the electrons toward the anodes. This approach has two disadvantages: it introduces a variation of the drift velocity in the last part of the drift path, and there is a risk of losing electrons when moving too close to the surface. In the ALICE design, we maintain the same voltage difference between adjacent cathodes in the whole drift region, meanwhile we apply quite high voltages to the cathodes opposite to the anodes. With this configuration, electrons travel along the middle of the wafer almost till the anodes, and then they are abruptly pushed toward the anodes. The path of the electrons is well visible in figure 6, represent-

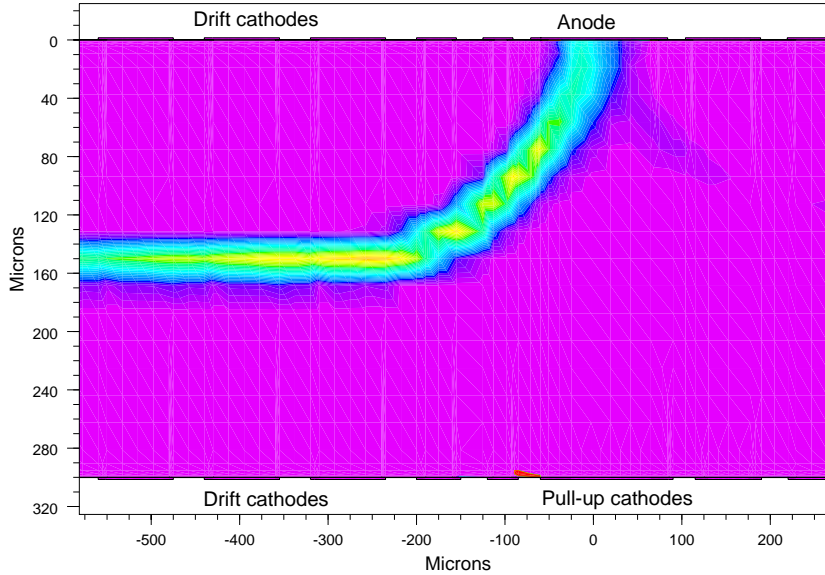


Figure 6: Density distribution of the electron component of the leakage current.

ing the intensity of the leakage current. This plot also evidences that no electrons escape towards the outer n^+ ring. Indeed, as shown in figure 7, the cathodes are biased in a way to create a potential valley which does not permit the electrons to find an alternative way to reach the bulk contact. This point has been experimentally checked in the laboratory.

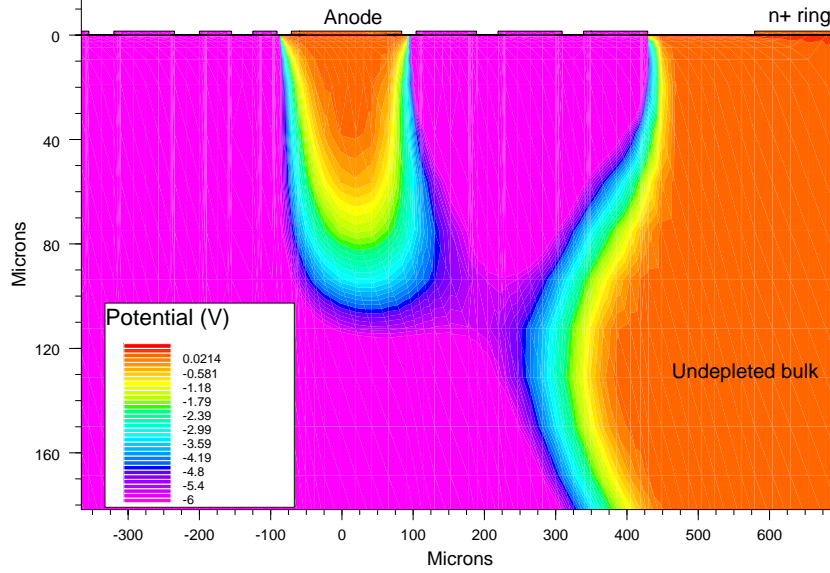


Figure 7: Close-up of the potential distribution in a region surrounding the anode. The colour palette is squeezed from -6 to 0 V, in order to evidence the potential barrier between the anode and the outer undepleted region.

We injected charge with the MOS injectors placed in the middle of the drift region and we varied one by one the potential of all the cathodes composing the collection zone. We verified that the biasing scheme shown in figure 4 provides the maximum collection efficiency with a safety margin of several volts around the values indicated in the sketch. This means that we can afford a certain variation of the resistivity of the wafer without encountering inefficiency problems.

5 Guard region.

At each flank of the drift cathode array, p^+ implants (guard strips) grade the potential from the highest negative voltages to the grounded outer n^+ implant ring. This region should be as small as possible to maximise the sensitive-to-total-area ratio. For this reason, the design has to be carefully studied to avoid problems like breakdown or punch-through currents.

It is not straightforward to build a structure able to simulate the electric quantities as they are in the real working conditions. If we simply compose a rectangular cell with nine cathodes per side (as done for the drift region), the lateral boundary conditions corrupt the solution in the central region where we expect the real situation. This happens because the structure is too short compared with the device depth ($300\text{ }\mu\text{m}$). On the other hand, we can not increase the number of cathodes to prolong the structure because of the limited amount of memory. To overcome this problem we realised a cell having lateral edges approximatively shaped as the equipotential lines foreseen for the real device (see figure 8) in the working conditions (16 V between cathodes). In this way the almost correct solution at the edges of the structure will lead to a correct result in the central region. The metal on the right edge is the anodic contact, and its potential is 30 V higher than the

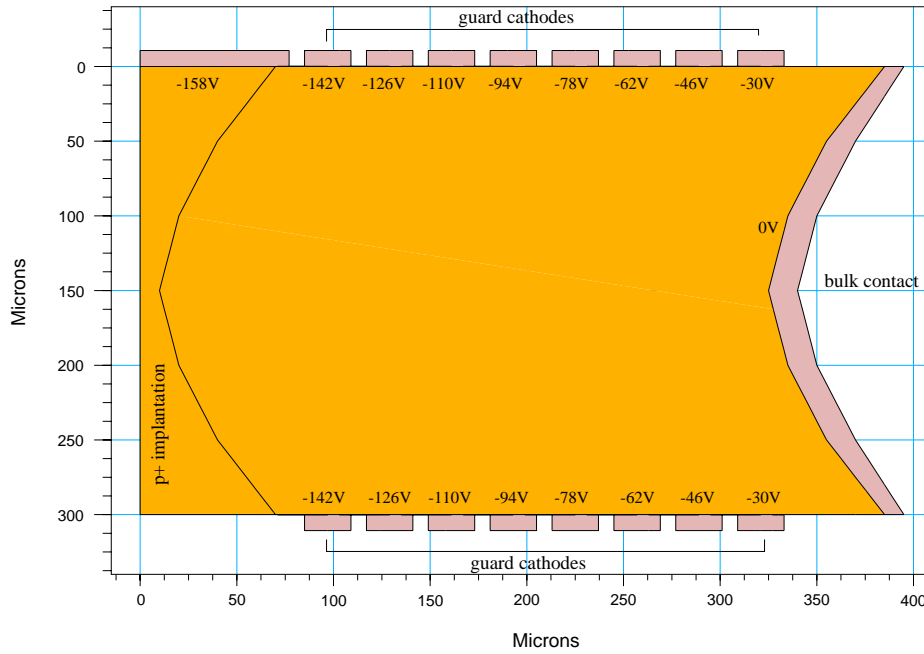


Figure 8: Structure adopted for the simulation of the guard region.

potential of the first couple of cathodes. This is the expected depth of the potential gutter

generated between two opposite cathodes. The left side is shaped using a p^+ implant in order to fix the behaviour of the lowest potential lines. Figure 9 shows the result, in terms

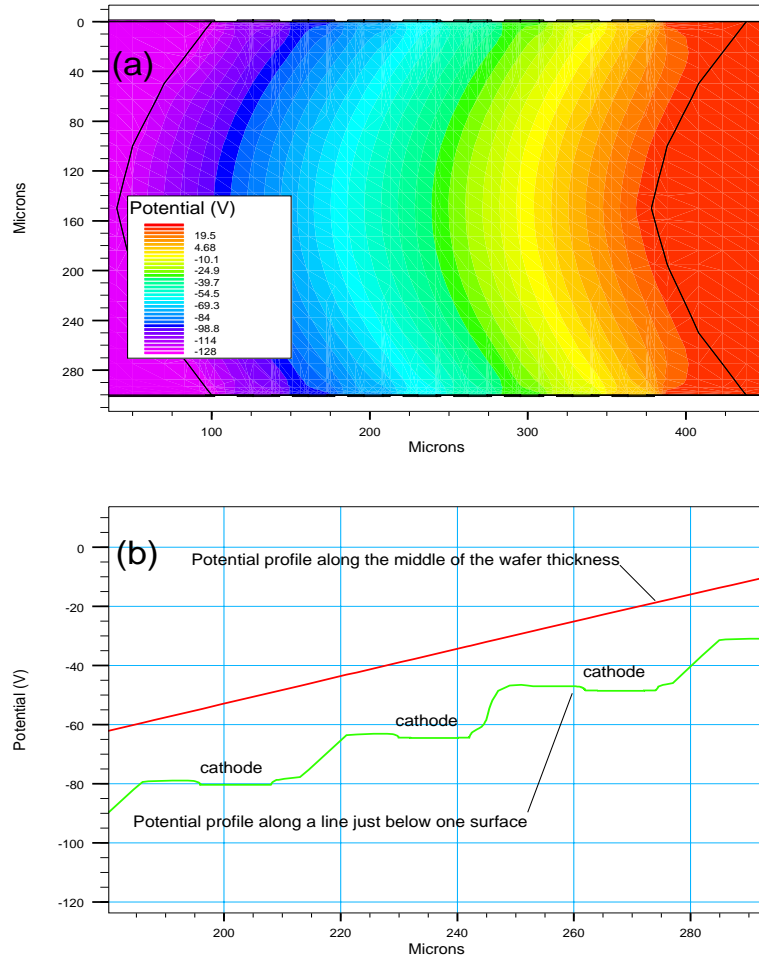


Figure 9: (a) Potential map imposing a voltage difference between consecutive cathodes of 16 V ; (b) Section of the potential map along two lines, both parallel to the detector surface.

of potential distribution, of a simulation in which we applied a voltage difference of 16 V between adjacent cathodes. We can see a very regular solution from one side to the other of the device. In particular, from the second plot we note that the potential along the middle of the wafer thickness is a straight line with a slope of $16\text{ V}/\text{cathode}$. This is what we expect for the real case, where the slope of the potential profile along a line parallel to the wafer surface is ruled only by the voltage difference between cathodes.

From these bases, it is possible to start a detailed analysis of the surface region.

5.1 Breakdown.

Let's now evaluate the risk of breakdown. It is known that a drifting carrier can gain enough energy to free an electron when colliding with a crystal atom. The generation rate is given by the following equation:

$$G = \frac{1}{q}[\alpha_n J_n + \alpha_p J_p] \quad (1)$$

where α_n and α_p are the ionization rates respectively for electrons and holes. These parameters represent the number of carriers generated by an electron or a hole per unit length and are strongly field-dependent. J_n and J_p are the respectively the electron and hole current densities.

When a sufficiently high electric field is present on a certain spatial extent we can undergo to avalanche breakdown. We reach the condition for avalanche breakdown when the ionization integral

$$I_{ion} = \int_0^W \alpha_n e^{\int_x^W (\alpha_p - \alpha_n) d\xi} dx \quad (2)$$

is equal to 1, where W is the extent of the high field region. The simulator allows both the direct evaluation of the current density via the generation rate and the determination of the ionization integral along a generic line. In reality, the conditions near the surface are quite more elaborated and it is difficult to reproduce the reality. The main concern regards the high level of defects in the vicinity of the silicon surface which introduces several complications: reduction of the mean free path, increment of the leakage current and, localised regions with high electric field. As soon as the simulations cannot account for the presence of these problematics, we decided to consider only the electric field strength as a parameter for our analysis. In particular, our aim is to maintain the electric field strength below $30 \text{ V}/\mu\text{m}$, which is generally considered a dangerous value.

In this section we do not deal with the determination of the main geometry of the guard region, which is, more or less, predetermined by the space available on the silicon pad and by the choice of having one guard every two drift cathodes. Instead, we verify the effectiveness of geometrical and/or technological solutions able to decrease the electric field intensity. In particular, we consider two methods: field-plate, and lowly-doped lateral implants. The first, widely used in solid state detectors, requires the extension of the p^+ contact metallisation beyond the metallurgical junction. This overhanging metal modifies the potential distribution below the surface and reduces the curvature effect near the implant. The second technique aims at the same result realising a p^- doped zone at the periphery of the junction.

First, we consider the simplest case where neither field-plate, nor lowly-doped implant are present. In particular, looking at figure 9b, we concentrate our attention to the

right edge of a p^+ implant which undergoes to a higher potential gradient. The field-

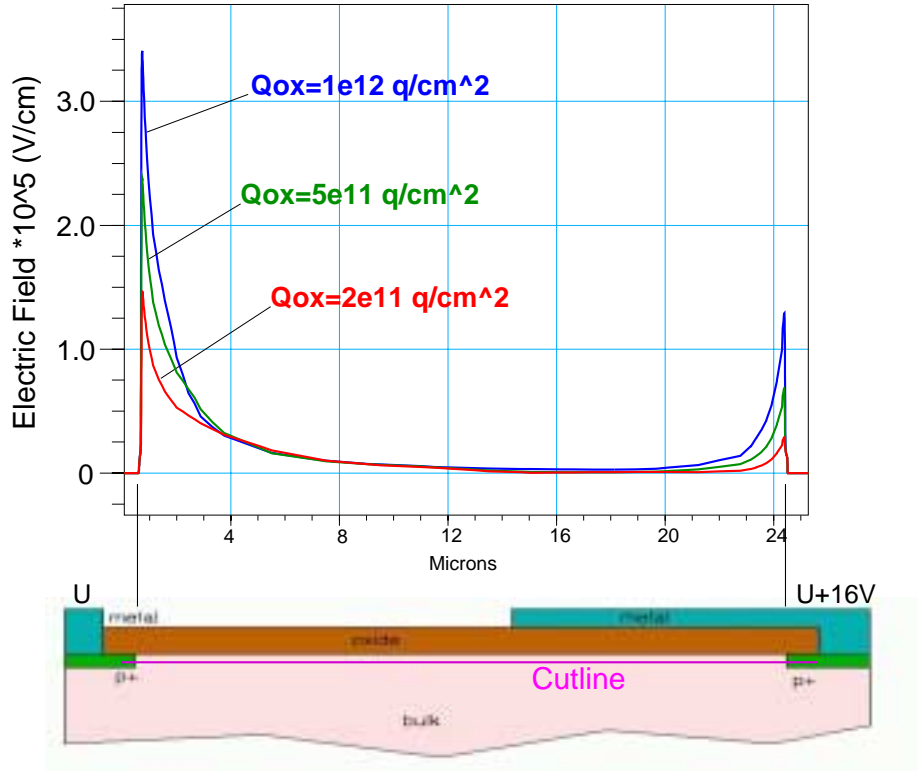


Figure 10: Electric field intensity along the cutline for different oxide charges.

plate on the left side of the cathode (see sketch of figure 10) is used to avoid the punch-through phenomenon (see next paragraph). The cathodes, according to process simulations, present a gaussian decay of the acceptor concentration, with a $0.3 \mu m$ FMHW. The electric field intensity along a cutline located $0.4 \mu m$ below the $Si - SiO_2$ interface is shown in figure 10. We can see that, with an oxide charge density of $2 \times 10^{11} cm^{-2}$ (typical for a $< 100 >$ crystal), the electric field magnitude at the junction's edge stays well below our critical value. But, when we consider higher densities, due, for example, to radiation damage or concentration non-uniformities, the electric field peak approaches rapidly this value. Thus, the structure is not safe as far as breakdown is concerned.

Now, we introduce, on the stressed edge, a metal overhanging the oxide $5 \mu m$ beyond the junction. The effect of the field-plate is shown in figure 11. There are two peaks of the electric field in the vicinity of the stressed side: one is located at the junction, while the other is placed under the edge of the metal. As a consequence, the stress is split in two separated regions, and both peaks are well below the critical value for all the oxide charge densities considered. A field-plate could be considered sufficient for our purposes.

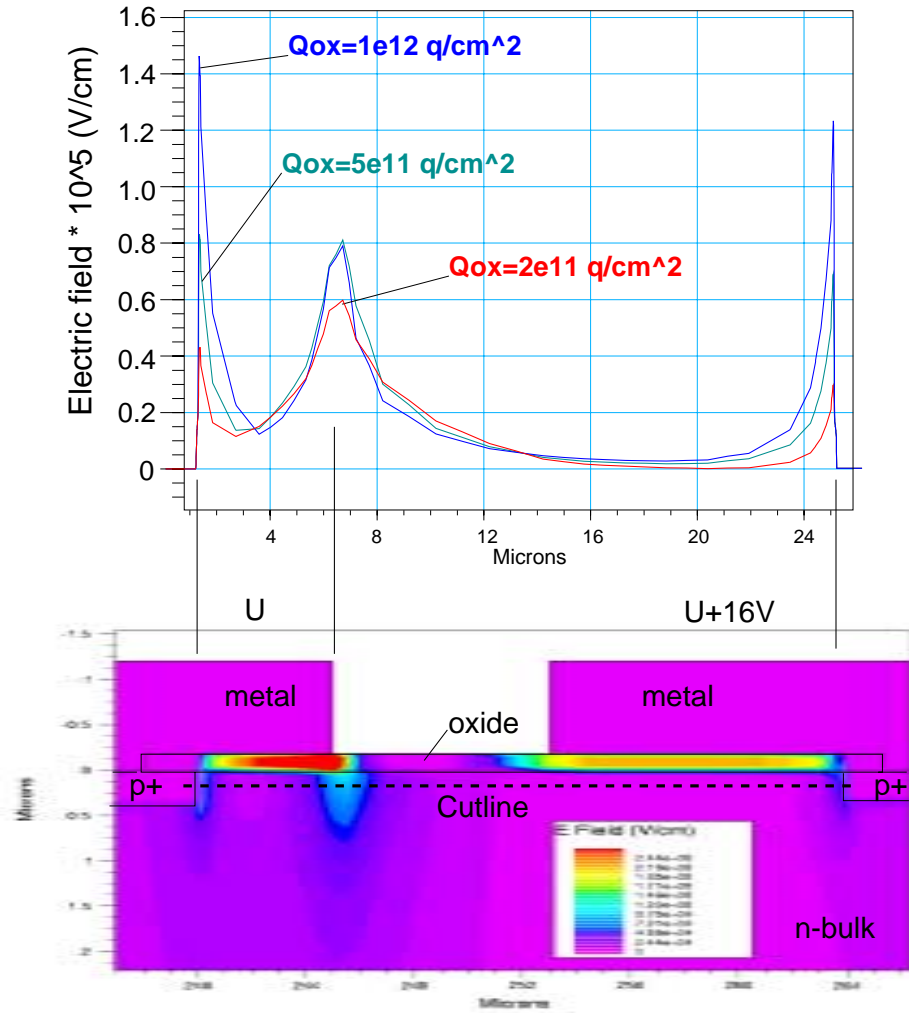


Figure 11: Electric field intensity along the cutline for different oxide charges.

The last step is to introduce a lowly-doped implant at the junction edge. The same doping decay is used for both implants. Figure 12 shows a plot of the electric field intensity in this situation. The p^- implant is $2\text{ }\mu\text{m}$ wider than the p^+ one, thus the field-plate results $3\text{ }\mu\text{m}$ wide. A third small peak of the electric field is visible in that region. It is related to the variation of the dopant concentration passing from the p^+ to the p^- implant. The electric field in the junction region is further reduced with respect to the previous case, even though not in a significant way.

We can conclude that the field-plate is mandatory to reduce significantly the risk of breakdown. Using this technique we can tolerate quite high oxide charges, due, for example, to radiation damage. These results are supported by several measurements on irradiated detectors (see [4]). The lowly-doped implant method does not improve the

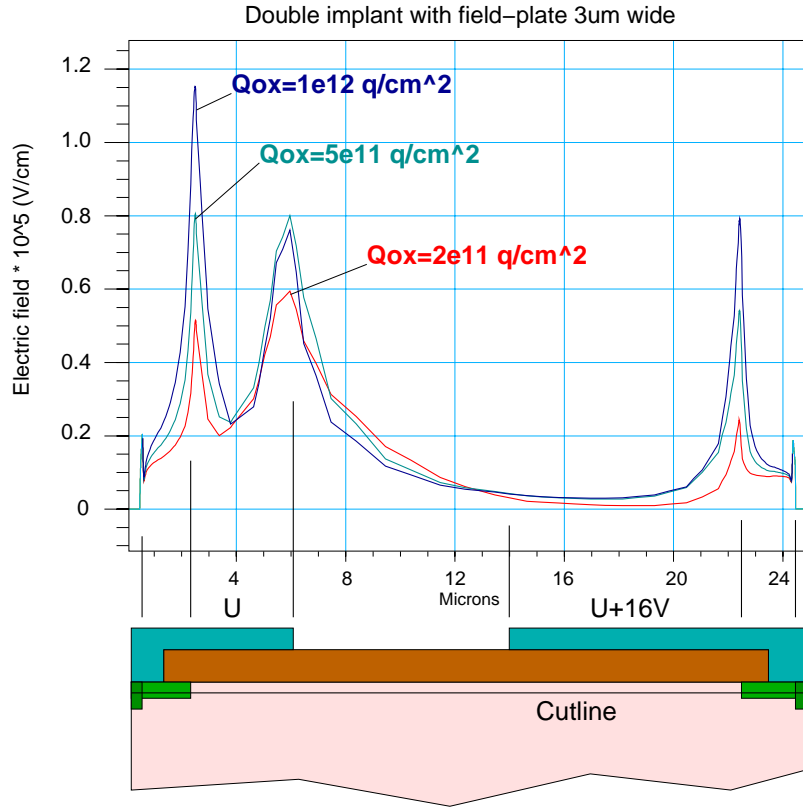


Figure 12: Electric field intensity along the cutline for different oxide charges.

situation significantly. Anyway, since an implant with this concentration has to be realized for the integrated divider, this improvement is achievable with no additional costs.

5.2 Punch through.

A second concern regarding the design of the guard cathodes is the hole current that appears between two reverse-biased cathodes when their potential difference reaches the “punch-through” voltage (V_{pt}). At this voltage the potential saddle present between the cathodes is compensated, and holes are injected from the more positive p^+ implant to the other. The height of the potential saddle, and as a consequence V_{pt} , depends on the bulk resistivity, on the distance between cathodes, but above all on the density of the positive fixed oxide charge. Simulating the punch-through voltage between cathodes of a test structure, we found a very high value. As shown in figure 13a, there is a sudden increase of the current in both cathodes at about 80V. In reality, laboratory measurements demonstrated that this voltage is much lower, i.e. some 20V (see figure 13b) [5]. This discrepancy is due to the partial compensation of the positive oxide charges by the environmental moisture. We found that the punch-through voltage is time-dependent. In

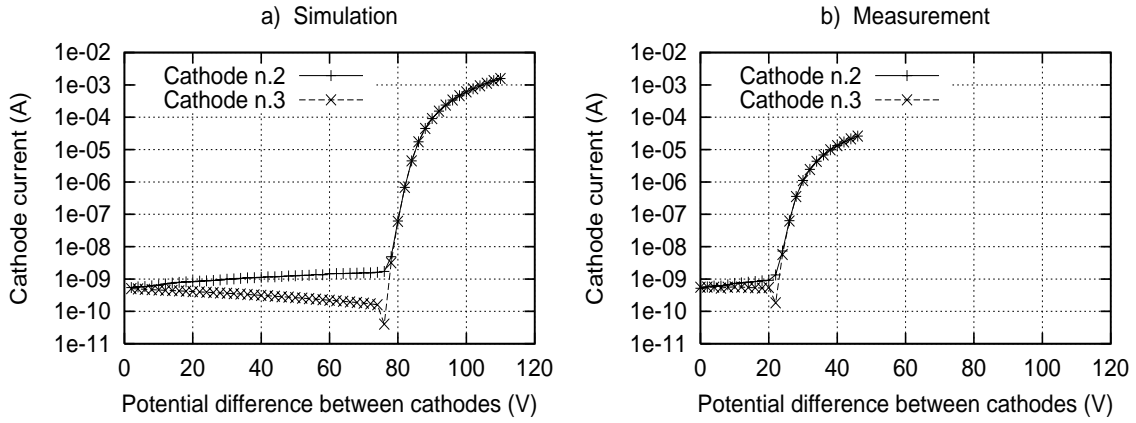


Figure 13: Simulated (a), and measured (b) current of the cathodes as a function of their potential. difference

particular, its value decreases exponentially, as the compensation becomes stronger, to reach a stable value within a time that depends on the relative humidity. The effectiveness of the charge compensation depends on the oxide thickness, and as a consequence the punch-through voltage depends on it [5].

This phenomenon creates problems in a silicon drift detector, when the punch-through voltage is lower than the operating voltage difference between consecutive cathodes. Indeed, the hole current flowing from one guard cathode to the other alters the linearity of the potential distribution on the drift cathodes. The aim of the simulations is to find an artifice that renders the device insensitive to this phenomenon in any condition.

The solution is represented in figure 14. In practice, we enlarge the field plate of the more

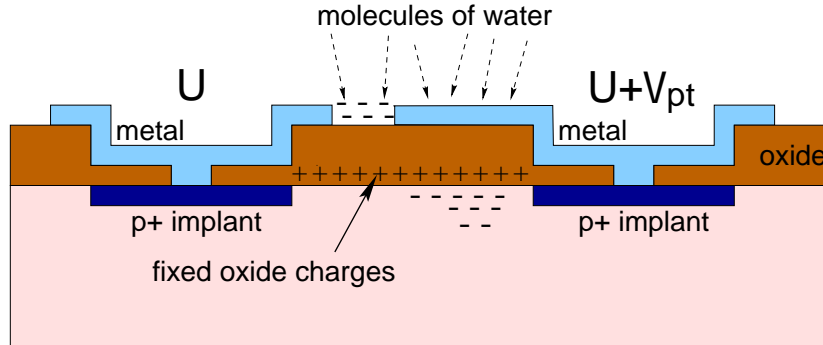


Figure 14: Enlarged positive field-plate to avoid premature punch-through.

positive cathode well beyond the metallurgical junction. In this way, we protect the covered oxide against the accumulation of negative charges, and, simultaneously, we build up a “positive” potential. The effectiveness of this solution is depicted in figure 15a. This

simulation is carried out imitating the effect of humidity as a negative field-plate applied

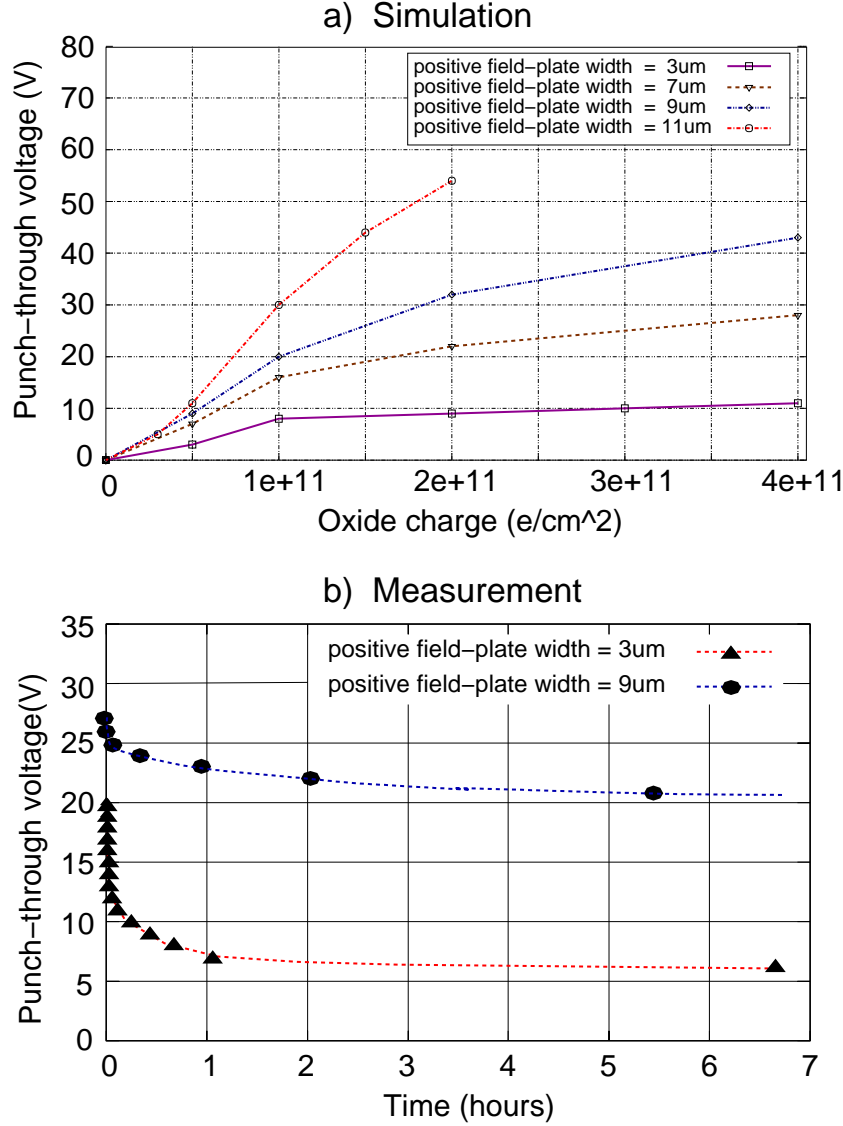


Figure 15: Simulations (a), and measurements (b) on the effectiveness of the positive field-plate on the punch-through voltage. The geometrical parameters are those of the guard structure. The oxide thickness is 180nm.

on the uncovered part of oxide. This trick is found to reproduce very well the reality. In the plot we see that the larger the positive field-plate the higher the punch through voltage. In particular, for normal oxide charge densities of $1.5 \times 10^{11} cm^{-2}$ a field-plate length of 9 μm is enough to satisfy our requirements of 16V between consecutive guard cathodes. In the calculations we used a very thin oxide (180 nm) in order to be in the worst conditions.

Experimentally we found a very good agreement with this results. As an example, in figure 15b we see the punch-through voltage as a function of time respectively for a structure having a positive field-plate $3\mu m$ wide and for another with a $9\mu m$ -wide field-plate. The oxide thickness of this device is 180 nm with a positive oxide charge concentration of about $1 \times 10^{11}\text{ cm}^{-2}$. We note the good agreement of the measured asymptotic punch-through voltage with the simulations performed in the same conditions.

In conclusion, in the final design the guard cathodes are equipped with a positive field-plate having a width of $9\mu m$. This value does not provide a great margin of safety for low oxide charges (lower than $1 \times 10^{11}\text{ cm}^{-2}$). As a matter of fact, increasing the width of the metal overhang, we have to deal with another problem, that is the probability of a short circuit between the metallisations of consecutive cathodes. Thus, the value we choose is a compromise between the two concerns.

A detailed description of the simulations and experimental results can be found in [5].

6 MOS injectors.

The MOS injector is a basic component of a silicon drift detector [2]. It permits to calibrate the drift velocity which is strongly dependent on the temperature ($v_{drift} = \mu E_{drift} \sim T^{-2.4}$). Indeed, placing the injectors in known positions it is possible to extract the drift time and, as a consequence the drift velocity.

In the ALICE detector, three injector lines are inserted between consecutive drift cathodes at three different drift distances. Each line consists of a metal strip deposited over the oxide. Beneath the strip, separated by a 100 nm -thick oxide, it runs a p^+ implant interrupted in 33 points that constitute the injection locations. In these points, $100\mu m$ wide, there is an accumulation of electrons due to the positive oxide charge. Applying a negative pulse to the metal line we push a certain number of these electrons in the silicon bulk. At the anodes we obtain the drifted images of 33 point-like MOS injectors.

Assuming a sufficient number of electrons accumulated beneath the $Si - SiO_2$ interface, the injector can be viewed as a parallel plate capacitor. Thus for a certain gate area the number of electrons injected depends only on the oxide thickness. The thinner the oxide the higher the injection efficiency. Furthermore, increasing the pulse amplitude on the gate, we expect to see a linear growth of the charge collected at the anodes. This is valid till a certain point. Infact, when with a pulse we inject all the electrons in the pocket we have a saturation of the signal at the anodes.

Designing the MOS injectors, a critical point is to guarantee the accumulation of electrons under the gate. As for the classical MOS capacitor, the state of accumulation depends on the oxide thickness, oxide charge, and potential on the gate. The situation is

further complicated due to the presence of two drift cathodes, having different potentials, at each side of the injector itself. Simulations are mandatory to establish the range within which we are allowed to vary these parameters to obtain an efficient injection.

The structure used for the simulation is a cross section along a plane perpendicular to the drift cathodes and passing in the centre of an injector. In practice, it is the same used for the drift region inserting the injector between the two central cathodes. We consider a device with an oxide thickness of 200 nm and we perform the study for two oxide charge densities, namely of $2 \times 10^{11}\text{ cm}^{-2}$ and $4 \times 10^{11}\text{ cm}^{-2}$. What we want to see is the potential we have to apply to the gate in order to have a layer of accumulation. Figures 16 and 17 display the electron density in the region of the injector for different potentials of the gate and for the oxide charges mentioned above. The succession of plots evidences, for both cases, the creation of the accumulation layer as the potential applied to the gate increases. In particular, for the lower oxide charge density, a potential of 7 V higher than the more positive cathode is necessary to create the layer, while, for the higher oxide charge concentration, 5 V are sufficient. Thus, to have an efficient injection for any detector, we have to maintain the metal line 8 V (at least) more positive than the adjacent cathode. We tried to verify the simulation results measuring the charge injected by an injector. Keeping the generator pulse height constant, and being in the working bias conditions (8 V between consecutive drift cathodes), we applied growing potentials at the gate, and we measured the signal amplitude at the anodes. The sample has an oxide thickness of 200 nm and an oxide charge density of $2.8 \times 10^{11}\text{ cm}^{-2}$. Figure 18 shows the amplitude of the signal at the anodes as a function of the difference between the potential of the gate and the potential of the more positive cathode. From this plot we can evince that we start to accumulate electrons underneath the gate at a voltage difference of about 5.5 V . This result is in good agreement with the simulations.

For thicker oxides the effect of the potential applied on the gate is less pronounced. Thus, the presence of the accumulation layer is more related to the value of the oxide charge density. The simulations revealed that, given a certain oxide charge, the potential on the gate that allows the creation of an accumulation layer is lower with respect to a thin oxide. Thus, the conditions determined above are applicable also in this case.

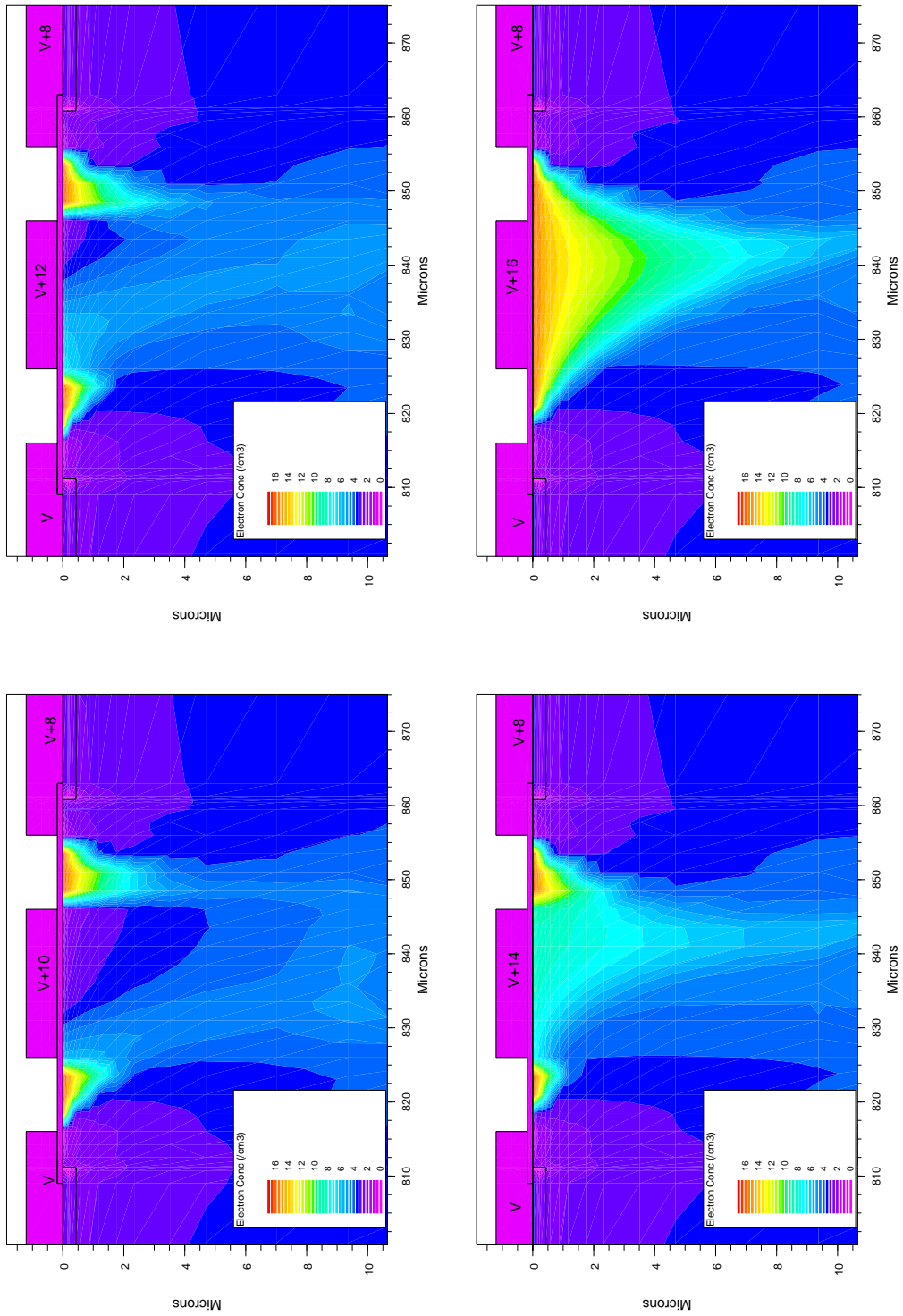


Figure 16: Simulation of the electron concentration under the injector for various potentials of the gate. The oxide thickness is 200nm while the oxide charge density is $2 \times 10^{11} \text{ } 1/\text{cm}^2$.

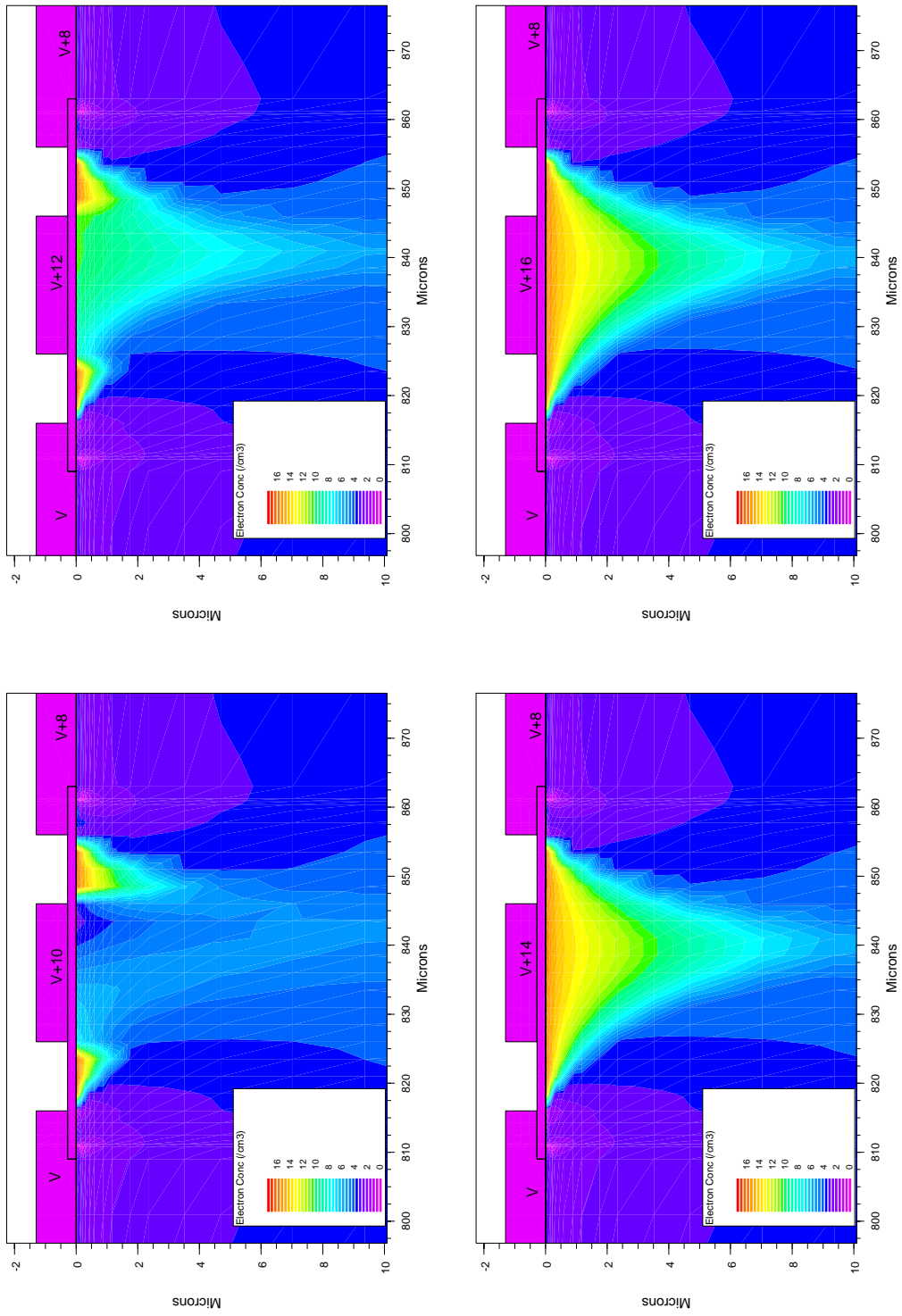


Figure 17: Simulation of the electron concentration under the injector for various potentials of the gate. The oxide thickness is 200nm while the oxide charge density is $4 \times 10^{11} \text{ } 1/\text{cm}^2$.

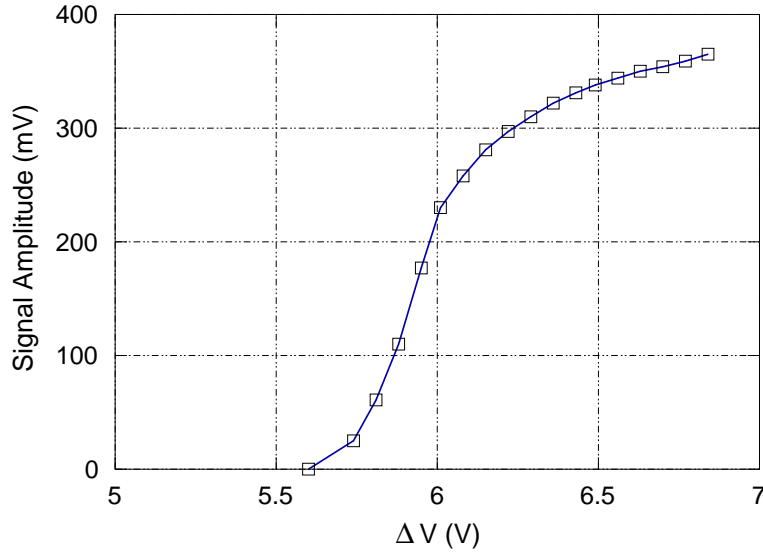


Figure 18: Signal amplitude at the anodes as a function of the potential of the injector gate referred to the more positive adjacent cathode.

7 Conclusions.

During the R&D of the ALICE silicon drift detector thorough computer simulations were performed to distill a robust and redundant design. Every single structure present in a linear SDD was analysed (drift region, collection zone, guard region, and charge injectors). Basing on the simulation results, we implemented several innovative solutions in the detector design. Laboratory measurements demonstrated the reliability of the solutions obtained with the simulator. In this way, we arrived to the final version of the detector with a low number of prototype iterations.

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