Current mode read-out circuit for InGaAs photodiode applications

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A B S T R A C T

Infrared focal plane arrays have many military, industrial, medical, and scientific applications that require high-resolution and high-performance read-out electronics. In applications involving InGaAs sensor arrays, data read-out can be carried out by circuits implemented with 0.35 μm CMOS technology. In this paper we propose a dynamically regulated cascode current mirror for pixel read-out. From simulation results, we expect this circuit to achieve a better trade-off between silicon area, signal-to-noise ratio, and output dynamic range than the trade-off that is currently achieved by current mode CMOS read-out circuits.

1. Introduction

The design of read-out integrated circuits (ROICs) for infrared image sensors [1–6] is similar to the design of ROICs for visible light image sensors [7–13]. Many (infrared) focal plane applications exist—military, industrial, medical, and scientific—in which high-performance read-out electronics and high-resolution are simultaneously required. There is a conflict between these requirements: increasing the number of pixels and keeping the overall chip area constant will reduce the complexity and therefore impair the performance of the ROIC.

The performance of a current mode ROIC involves the following desirable properties: well-controlled bias point, low noise, low input impedance, and high dynamic range:

- The accurate bias point and the low noise reduce the smallest detectable signal, taking into account the minimum light level that is set by the photodetector dark current [14].
- A lower input impedance contributes to a higher injection efficiency [3], so that the same integration capacitor can be used to implement a detector with larger bandwidth.
- A larger dynamic range leads to an increase in the maximum stored charge, for the same integration capacitance. If large integration capacitors must be used, they should be placed outside the pixel as shown in Fig. 1. This figure, which represents a typical application of current-mode read-out circuits, conveys the idea that the current mode is usually restricted to the pixel area, and the distribution (multiplexing) of pixel samples is accomplished in voltage mode.

Most of the reported ROICs are implemented in voltage mode. In this case, the voltage mode is also used in the pixel area. In either case—current-mode pixel or voltage-mode pixel—all pixels share a common architecture for the implementation of column and row addresses for array read-out. This architecture, which is often implemented in voltage mode regardless of the pixel mode, is shown in Fig. 2. When analog-to-digital converters are used, they often digitize the integrated current at the output of the column amplifiers. As the minimal transistor channel length becomes smaller in CMOS technologies, the supply voltage is reduced. This impairs the output dynamic range of the column amplifiers.

By contrast, the output dynamic range of current-mode read-out amplifiers is not impaired by the reduction of the supply voltage. A current-mode ROIC is easily integrated with current-mode image processing circuits, so that an image can be processed in analog domain, i.e. before digitization takes place. Depicted in Fig. 3, this idea has been known for some years as *smart pixels* [15–19]. Current-mode image processing circuits use simpler building blocks and have higher operation speed than their voltage-mode counterparts. The ROIC must have a very high output impedance, and the integration of current signals into read-out capacitor voltages does not happen.

In this work we propose two current-mode amplifiers for ROIC applications. Using electrical simulations, we compare the proposed circuits with state-of-the-art ones. We present a

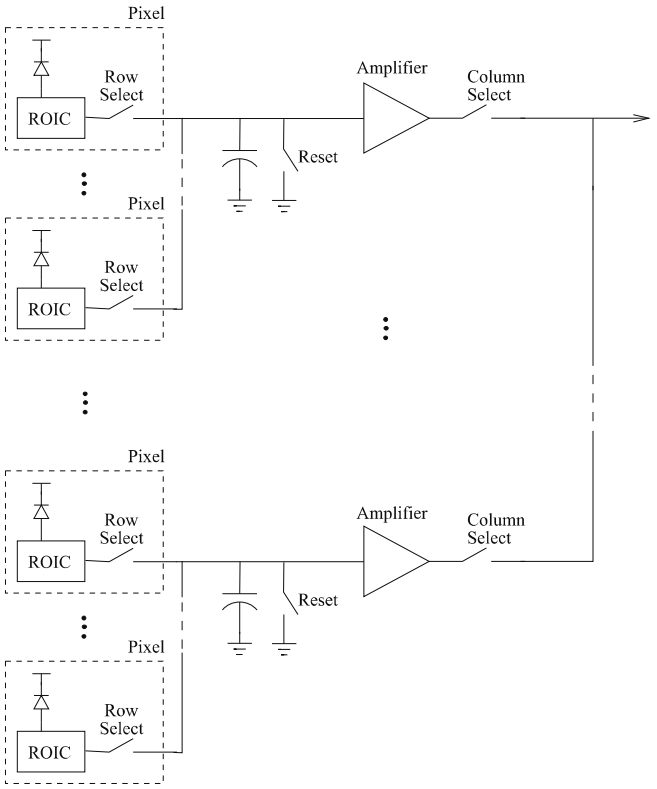

Fig. 1. Typical application of current-mode read-out circuits. Note that the current mode is restricted to the pixel area. Pixel samples are actually read-out of the sensor array in voltage mode.

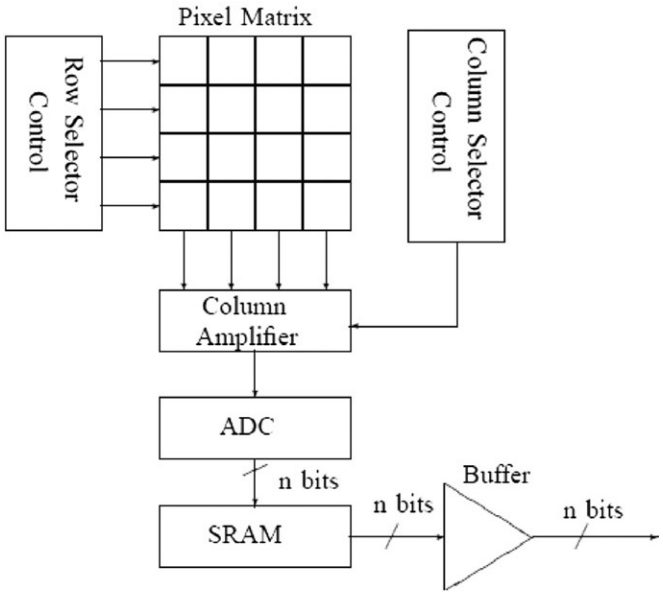

Fig. 2. Array architecture for the implementation of read-out schemes based on row and column addresses. Pixel samples are usually represented in voltage mode, regardless of pixel inner circuits being current-mode or voltage-mode.

state-of-the-art review in Section 2, and a model for the InGaAs infrared photodiode in Section 3. The regulated cascode current mirror and the dynamically regulated cascode current mirror are introduced in Section 4. In Section 5, noise and harmonic distortion performance figures are computed for both circuits. Post-layout electrical simulations with BSIM3V3 models are presented in Section 6, and the conclusions are presented in Section 7.

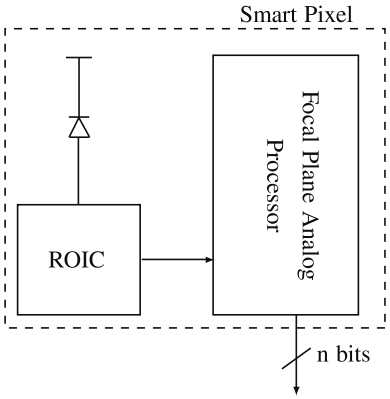

Fig. 3. Application of current-mode read-out circuits for current-mode focal plane image processing.

2. State-of-the-art review

InP–InGaAs infrared sensors have been considered as potential alternatives to low bandgap semiconductor infrared photodetectors such as HgCdTe. HgCdTe photodetectors suffer from (responsivity nonuniformity) at the infrared band, and the InP-InGaAs alternative offers long-wavelength infrared arrays at a significantly lower cost [6]. A disadvantage of InP–InGaAs techniques for infrared applications is their lack of flexibility: it is difficult to adjust the peak detection wavelength by changing the barrier/well material composition. As a consequence, the peak responsitivity is limited to a narrow band around 8 μm [20].

An InGaAs photodiode can be easily modelled as a silicon photodiode. The design of a ROIC for CMOS technology can be copied in a straightforward manner [21] for a hybrid CMOS-InGaAs implementation—the photodiodes are implemented in InGaAs technology and the CMOS ROIC is connected to the photodiode array by means of flip-chip indium bonds.

The majority of the reported ROICs is implemented with the three-transistor active pixel sensor (APS) topology [7–13]. This topology has three elements: (i) a voltage amplifier (for voltage mode applications) or a transconductance amplifier (for current mode applications), (ii) a switch for resetting the photodiode voltage level at the beginning of a charge integration period (also in current mode), and (iii) a switch for row or column read-out. This topology is associated with techniques such as self-integration, one source follower per detector, and direct injection [2,4–6].

More recent amplifier structures, such as buffered direct injection and capacitive feedback transimpedance amplifier, provide a better performance in terms of injection efficiency and detector bias stability [5], with the help of an in-pixel operational amplifier. However, their performance is limited by the performance of the operational amplifier that can be implemented in the pixel area. Another technique, known as buffered gate modulation input [5], provides in-pixel detector current amplification and current-mode background level suppression. The integration capacitance is placed outside the pixel, but an operational amplifier is still required for detector bias stabilization. Another interesting technique is switched current integration [6]: it provides a large storage capacity by means of an off-pixel integration capacitor. However, this technique still requires an in-pixel operational amplifier. A technique known as current mirroring direct injection [3] satisfies the requirements of high injection efficiency and detector bias stability, but an in-pixel integration capacitor is used, which impairs pixel area, dynamic range, and charge storage capacity. Finally, in [2], the authors achieved high-performance (i.e. stable bias point and high injection efficiency) without using neither an in-pixel operational

amplifier nor an in-pixel integration capacitor, by means of a technique called current mirroring integration. The current mirroring integration ROICs are based on amplifiers with a cascode output. The output impedance should be reduced further if one wishes to use these ROICs for analog image processing applications based on smart pixels (Fig. 3).

3. InGaAs sensor electrical model

When a (silicon) photodiode is inversely biased and is not exposed to light, it yields a reverse current known as dark current (i_{dark}) [22]. When photons are absorbed, a photocurrent (i_{ph}) is added to i_{dark}. The light intensity information is contained in i_{ph} [21]. Because of the depletion region, the junction of an inversely biased photodiode has an equivalent resistor–capacitor circuit model described by parameters R_j and C_j. In the InGaAs sensor, the intrinsic region has a fixed thickness, which allows for an accurate evaluation of R_j and C_j. The ohmic behavior of the contacts is modelled by a series resistor, whose resistance (R_s) is usually neglected.

The InGaAs sensor model can be obtained as shown in [21]. Fig. 4 shows the sensor model that will be used in our electrical simulations. The models of silicon and InGaAs photodiodes are very similar. This motivates the use of CMOS image sensor ROICs also for photodiodes in InGaAs technology.

Table 1 summarizes the model information. The wavelength range indicates the appropriate application. The image sensor sensitivity is defined by i_{dark}. The current noise of the sensor is added to the current noise of the ROIC. The sensor responsivity indicates the photon-to-electron conversion rate, and it is important for estimating the input current range as a function of the incident light power. The photodiode junction is modelled as a capacitance C_j in parallel with an ideal current source i_{ph}. Since the ROIC must be implemented on top of the image sensor array, the photodiode area imposes a constraint on the area available for the ROIC.

4. Current amplifier structure

For specific input and output ranges, a current mirror is a linear current amplifier. The current gain is defined by the ratio between the aspect ratios (W/L) of transistors that are created in the same stage of an integration process. The current gain is thus highly accurate, and its accuracy is mostly determined by the accuracy of the integration process. Non-linear distortion in a current mirror is mainly caused by the modulation of the output transistor channel length according to the voltage between its drain and source terminals [23]. Fig. 5 shows a regulated cascode current mirror (RCCM). Taking into account channel length modulation effects [26], the RCCM current gain is given by

$$I_O = I_{IN}\frac{W_2/L_2}{W_1/L_1}\frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}} \tag{1}$$

Channel length modulation occurs if λ cannot be neglected and if $V_{DS2} \neq V_{DS1}$. The bias current I_B is a fraction of I_{IN}. It is used to set $V_{GS\,3}=V_{GS\,1}$—in this case, the scale factor between I_B and I_{IN} is the same as the ratio between the aspect ratios W_3/L_3 and W_1/L_1. Since $V_{DS\,1}=V_{GS\,1}$ and $V_{DS\,2} = V_{GS\,3}$, the channel length modulation is suppressed by the feedback loop composed by N3 and N4.

To provide an example of how the sizes of the transistors in Fig. 5 can be found, we arbitrarily chose current gain equal to 10, bias current $I_B = 10\,\mu A$, and cutoff frequency $f_c=2$ MHz. Since the current amplifier reads the photodiode current i_{ph} directly, the ROIC operates in continuous time. A sampling rate is set by the analog image processing circuits that would use the output of the ROIC. If frames are processed at 10 kHz (see e.g. [24]) and each pixel is read-out independently, then the cutoff frequency $f_c=2$ MHz is much larger than the 10 kHz sampling rate. We assumed that all transistors operate in saturation mode. The focus of this design was on maximizing the dynamic range while keeping the required area as small as possible: the transistor sizes shown in the caption of Fig. 5 satisfy the channel current density limits of the fabrication process. Since these sizes are minimal for the given current density limit, they minimize the *average* capacitance in circuit nodes. The frequency response of the RCCM depends on its own DC current gain and on the capacitance of the input current source [25].

However, the RCCM eventually has $V_{DS2} \neq V_{DS1}$ when its output dynamic range is large. We can thus still improve on its harmonic distortion. To see this, note that, in the case of Fig. 5, $V_{DS\,2}$ is given by

$$V_{DS2} = \sqrt{\frac{2I_B}{K_n}\frac{L_3}{W_3}} + V_{Tn} = 0.55\,V \tag{2}$$

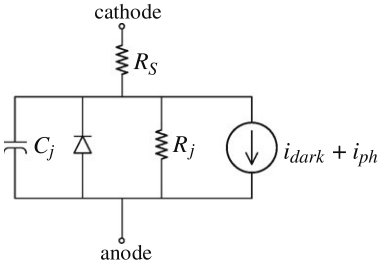

Fig. 4. Photodiode model.

Table 1
Electrical properties of InGaAs photodiode.

Property	Value
Wavelength range	$1.5\,\mu m < \lambda < 3.7\,\mu m$
i_{dark}	-600 pA
Reverse bias voltage	3–5 V
Current noise	1.82×10^{-11} A/$\sqrt{\text{Hz}}$
Responsivity	0.6 A/W
C_j	650 fF
Area	$10\,\mu m \times 10\,\mu m$ up to $75\,\mu m \times 75\,\mu m$

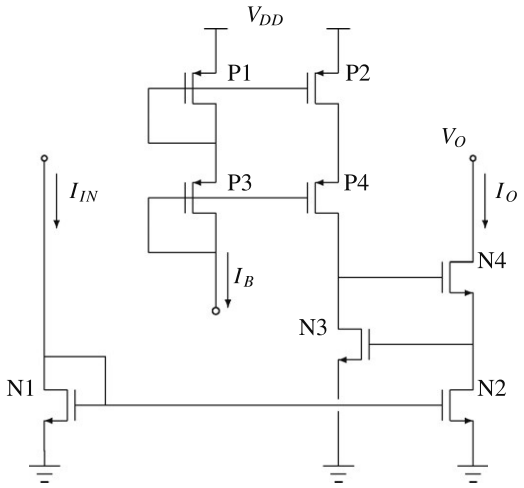

Fig. 5. Regulated cascode current mirror ($W_1 = W_3 = 1.4\,\mu m$ and $W_2 = W_4 = 14\,\mu m$ for the n-type transistors. All p-type transistors have width equal to 1.4 μm. For all transistors, $L = 0.7\,\mu m$).

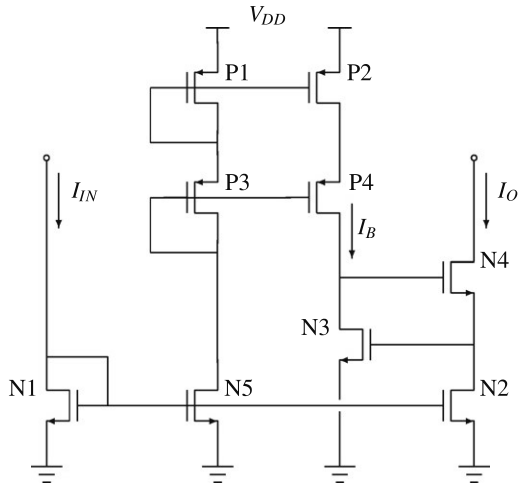

Fig. 6. Dynamically regulated cascode current mirror ($W_1 = W_3 = W_5 = 1.4\,\mu m$ and $W_2 = W_4 = 14\,\mu m$ for the n-type transistors. All p-type transistors have width equal to 1.4 μm. For all transistors, $L = 0.7\,\mu m$).

where K_n and V_{Tn} are parameters from the fabrication process, and that $V_{DS\ 1}$ is given by

$$V_{DS1} = \sqrt{\frac{2I_{IN}}{K_n}\frac{L_1}{W_1}} + V_{Tn} \tag{3}$$

from which we conclude that $0.51\,V \le V_{DS1} \le 0.58\,V$. Thus $V_{DS\ 1}$ changes significantly with respect to $V_{DS\ 2}$, which remains constant. The harmonic distortion caused by the channel modulation effect corresponds to a current gain error of $\pm 2\%$. To further reduce the channel length modulation, we propose the dynamically regulated cascode current mirror (DRCCM) that is shown in Fig. 6. In this circuit, the bias current I_B of the regulation loop composed by N3 and N4 is set dynamically. As in the RCCM, the regulation loop yields $V_{GS\ 3} = V_{GS\ 1}$, provided that the scale factor between I_B and I_{IN} is the same as the ratio between the aspect ratios W_3/L_3 and W_1/L_1. Also as in the RCCM, the DRCCM therefore achieves $V_{DS\ 1} = V_{DS\ 2}$, which yields a suppression of the distortion due to channel modulation effect. The improvement of the DRCCM with respect to the RCCM comes from the fact that I_B is mirrored from I_{IN}. Since I_B tracks change in the input photocurrent I_{IN}, we can achieve $V_{DS\ 2} = V_{DS\ 1}$ with an error under 1 mV for any input photocurrent, according to analytical and simulation results. After sizing the transistors in Fig. 6 by following the same design approach[1] that was applied for Fig. 5, we found the results that are shown in the caption of Fig. 6. For this DRCCM, the harmonic distortion caused by the channel modulation effect corresponds to the significantly reduced gain error of $\pm 0.2\%$.

5. Circuit analysis

To compare the RCCM and the DRCCM with respect to noise and total harmonic distortion, we propose a theoretical analysis using noise models and harmonic distortion models. The dynamic range is evaluated from the noise floor to the largest output current having a total harmonic distortion (THD) low enough for subsequent image processing applications. For comparison purposes, we will arbitrarily assume in Section 6 that the maximum acceptable THD is $-40\,dB$.

5.1. Noise analysis

For both the RCCM and the DRCCM, the output current noise power is computed as

$$I_O^2 = I_{nbias}^2 + I_{nRCi}^2, \quad i = 1 \text{ or } 2 \tag{4}$$

where

$$I_{nbias}^2 = \frac{g_{m,N4}^2 r_{o3}^2}{r_{o2}(g_{m,N4} + 1/r_{o4}) + 1}\left(I_{P2}^2 + I_{P4}^2 + \frac{g_{m,P2}^2}{g_{m,P1}^2} I_{P1}^2 + \frac{g_{m,P4}^2}{g_{m,P3}^2} I_{P3}^2\right) \tag{5}$$

is the noise power in the bias transistors (P1 to P4). Fig. 7 shows the RCCM noise model. For the RCCM,

$$I_{nRC1}^2 = I_{N2}^2 + I_{N4}^2 + \frac{g_{m,N2}^2}{g_{m,N1}^2} I_{N1}^2 + \frac{g_{m,N4}^2 r_{o3}^2 I_{N3}^2}{r_{o2}(g_{m,N4} + 1/r_{o4}) + 1} \tag{6}$$

is the noise power in the current mirror transistors (N1 to N4). Fig. 8 shows the DRCCM noise model. For the DRCCM,

$$I_{nRC2}^2 = I_{nRC1}^2 + \frac{g_{m,N2}^2}{g_{m,N5}^2} I_{N5}^2 \tag{7}$$

is the noise power in the current mirror transistors (N1 to N5). Since N5 has the same size of N1, we expect that the overall output noise power does not increase significantly with the inclusion of N5 in the DRCCM.

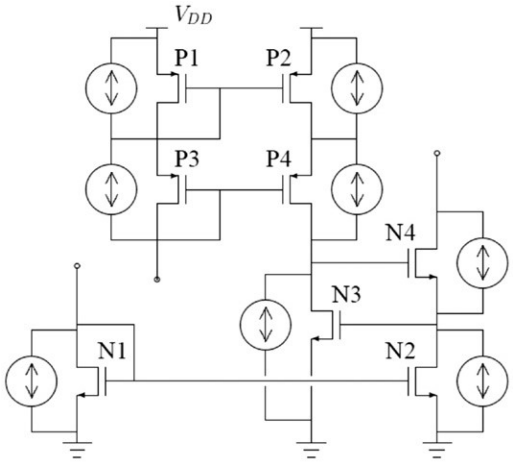

Fig. 7. RCCM noise model.

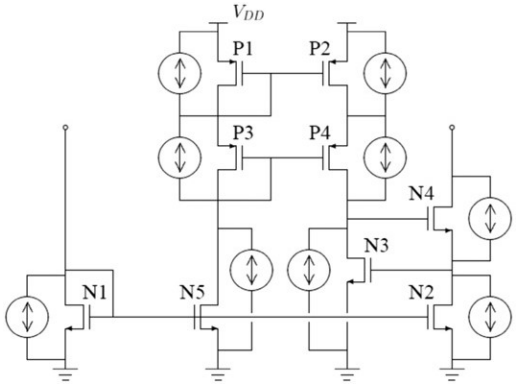

Fig. 8. DRCCM noise model.

[1] The design procedure is based on straightforward analysis using the drain currents of MOS transistors operating in saturation mode and, for simplicity, it is not included in this text. The supply voltage is $V_{DD} = 5\,V$ for the RCCM and for the DRCCM.

Since the RCCM and DRCCM circuits have dominant poles at 2 MHz, as chosen for the design example in Section 4, their noise frequency band is π MHz [26]. For a single pixel, the theoretical noise analysis based on Eqs. (5)–(7) yields:

- For the RCCM: I_{nbias}=0.69 nA RMS, $I_{nRC\ 1}$=4.27 nA RMS, and I_O=4.33 nA RMS.
- For the DRCCM: I_{nbias}=1.00 nA RMS, $I_{nRC\ 2}$ =8.10 nA RMS, and I_O=8.20 nA RMS.

As expected, the I_{nbias} values are quite lower than the I_{nRCi} values, so that the output current noise is mostly given by I_{nRCi}. Also as expected, the DRCCM output current noise is approximately at the same magnitude order of the RCCM output current noise.

5.2. Total harmonic distortion analysis

For an approximately sinusoidal current signal $i(t)$ with DC level equal to zero, the total harmonic distortion (THD) is defined as

$$\mathrm{THD} = \sqrt{\frac{I_2^2+I_3^2+I_4^2+I_5^2+\cdots}{I_1^2}} \tag{8}$$

where I_k, k=1,2,… are the coefficients of the expansion of $i(t)$ as an exponential Fourier series. To simplify the analysis, we neglect all the coefficients from I_4 on. To do the computation of second and third-order harmonic distortion coefficients, we use the equations from the SPICE models for MOSFETs, the transistors sizes from the design (Section 4), and the parameters of the 0.35 μm CMOS fabrication process [27].

In Fig. 9, we compare the RCCM and the DRCCM with respect to their THD as a function of the input current magnitude. The DRCCM achieves an improvement of at least 10 dB in THD for input currents ranging from near zero to 1.2 μA. The results in Fig. 9 were computed from Eq. (8) and, therefore, they do not take into account transistor mismatch or random deviations typical of the fabrication process. For a more detailed analysis, electrical simulations were carried out, and the results are shown in Fig. 14.

6. Simulation results

In this section, we compare the RCCM and DRCCM ROICs with current mirror integration (CMI) and three-transistor (3T) current mode ROICs that have been presented in the literature [2,7]. It is important to note that the comparisons presented in Table 2 are based on information available in the literature, whereas the plots presented in Figs. 13–17 are results of the work described in this paper. These plots show the advantages of employing the dynamic biasing technique. The comparisons are based on electrical simulations using circuit parameters extracted from the RCCM and DRCCM layouts, which are shown in Figs. 10 and 11, respectively. Whereas the DRCCM is slightly less insensitive to process variations, both circuits are sufficiently robust for the applications considered in this paper: the standard deviations around 10.0 A/A current gain are 2.47% for the RCCM and 2.57% for the DRCCM. Monte Carlo simulation details are thus not included in this paper.

Figs. 12–17 present simulation results which are specific to the RCCM and the DRCCM. Fig. 12 shows their frequency responses: both circuits achieve a 20 dB current gain with a cutoff frequency of 2.3 MHz. Results from an output current DC sweep are shown in Fig. 13. As the input current changes from 8 nA to 120 μA, the DRCCM exhibits a smaller output distortion. We can also see the larger distortion of the RCCM in Fig. 14. If we limit the acceptable THD at −40 dB, then the RCCM can be driven with currents in the [50 nA, 50 μA] range, while the DRCCM admits input currents in the range [50 nA, 70 μA]. The input impedance, displayed in Fig. 15 as a function of the input current, is similar for both circuits. The output impedance is constant at 236 kΩ for both circuits. The power dissipation is shown in Fig. 16, also as a function of the input current, indicating that the DRCCM dissipates more power than the RCCM. A trade-off hence exists

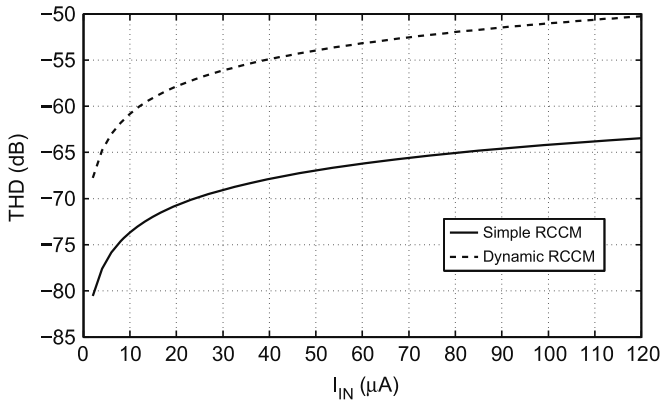

Fig. 9. THD comparison: RCCM and DRCCM.

Table 2
Comparison between read-out circuits: CMI [2], 3T current mode APS [7], RCCM, and DRCCM.

	CMI	3T (0.35 μm)	3T (0.18 μm)	RCCM	DRCCM
Area (μm²)	500	100	100	273	292
R_O	$g_m r_{ds}^2$	$r_{ds}/(1+g_m r_{ds})$	$r_{ds}/(1+g_m r_{ds})$	$g_m^2 r_{ds}^3$	$g_m^2 r_{ds}^3$
SNR (dB)	N/A	42	39	77	79
DR (dB)	20	64	53	60	63

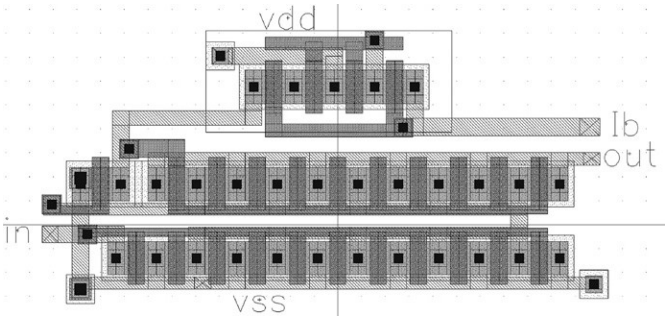

Fig. 10. RCCM layout.

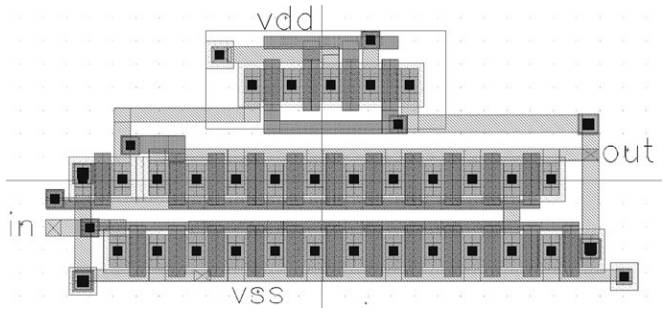

Fig. 11. DRCCM layout.

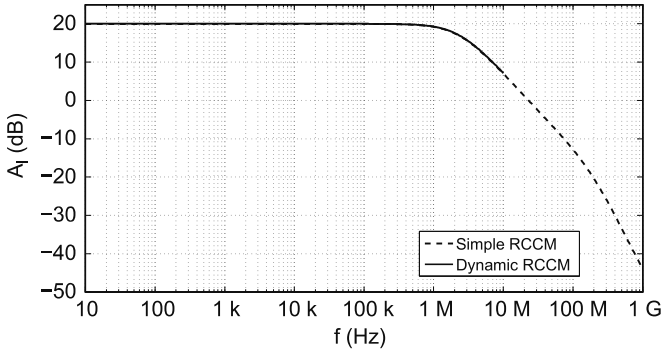

Fig. 12. Simulated frequency response: RCCM and DRCCM.

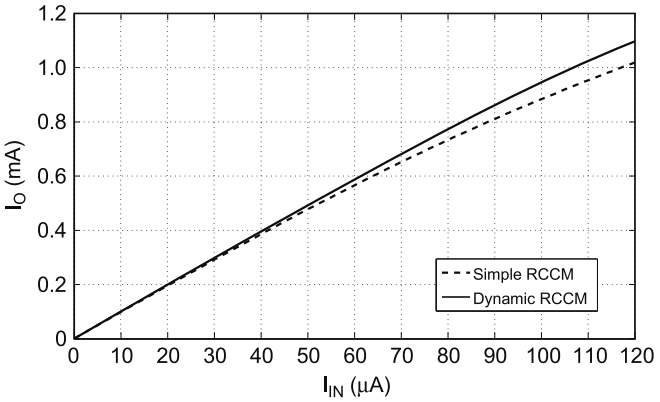

Fig. 13. Signal range (output current DC sweep).

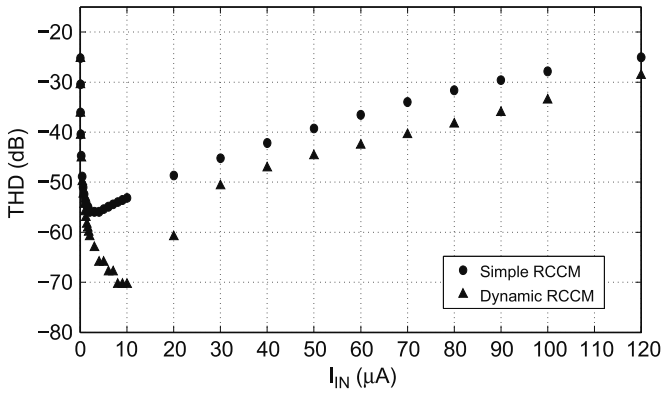

Fig. 14. THD comparison based on post-layout electrical simulations: RCCM and DRCCM. By limiting the acceptable THD to −40 dB, the input dynamic range can be estimated: it is [50 nA, 50 μA] for the RCCM, and [50 nA, 70 μA] for the DRCCM.

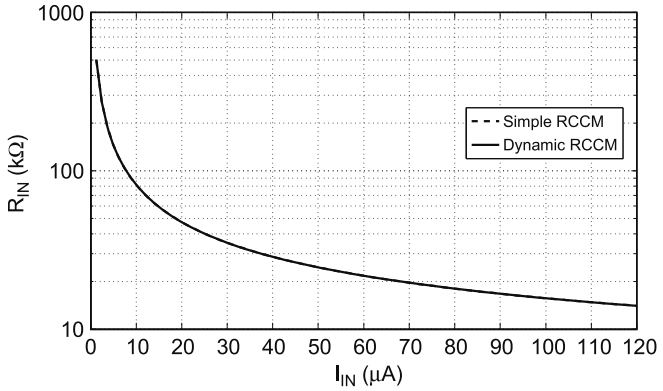

Fig. 15. Simulated input impedance.

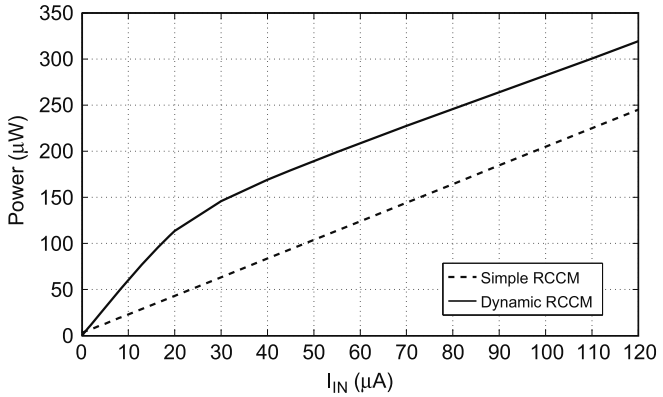

Fig. 16. Simulated power dissipation.

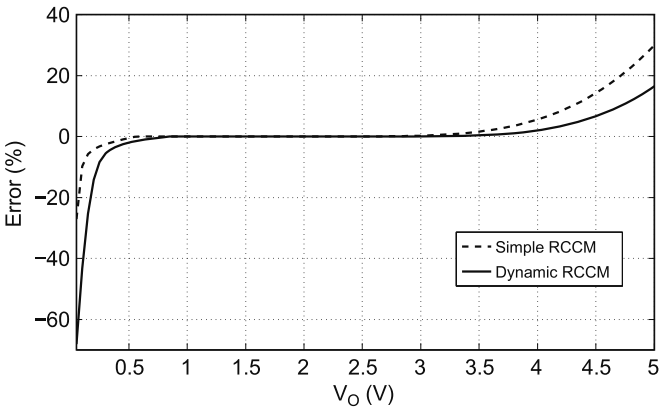

Fig. 17. Relative error of the output current, as a function of the output voltage.

between the DRCCM power consumption and its several advantages over the RCCM. Its higher power consumption is due not only to the additional transistor used for dynamic bias, but also due to the fact that I_B increases as I_{IN} increases. Fig. 17 shows the relative error of the output current, as a function of the output voltage. If we consider a relative current error below 1%, then the output voltage range of the RCCM is [0.45 V, 3.35 V] and the output voltage range of the DRCCM is [0.60 V, 3.75 V]. So the DRCCM has a slightly larger output voltage range.

Using the post-layout electrical simulations, we also computed the RMS output noise, and obtained 6.85 nA for the RCCM, and 8.06 nA for the DRCCM. The dynamic range is 60 dB for the RCCM and 63 dB for the DRCCM. We estimate the SNR to be 77 dB for the RCCM, and 79 dB for the DRCCM. In Table 2, we compare these figures with similar figures that have been recently reported for the CMI and 3T current mode approaches. We notice that the results reported in [2,7] are experimentally obtained from fabricated circuits, whereas our results are from post-layout simulations, which might partially explain the large discrepancy observed in the SNR and dynamic range figures. Yet, the results in Table 2 are an indication that the RCCM and the DRCCM ROICs may achieve significant improvements in SNR and dynamic range. Both the 3T current mode ROICs have quite high SNR and dynamic range, but their output impedance is rather small because of the single output transistor. The RCCM and the DRCCM require less silicon area than the CMI, and they have a higher output impedance than the 3T current mode ROICs.

7. Conclusion

In this work, we studied two implementations of ROICs for application in hybrid CMOS-InGaAs technologies, where the CMOS part of the technique is based on a 0.35 μm fabrication process. We named the ROICs under study RCCM and DRCCM. Using post-layout electrical simulations of the RCCM and the DRCCM, we compared them with previously reported experimental results for CMI and 3T current-mode ROICs, in terms of area, output impedance, dynamic range and SNR. The RCCM and the DRCCM achieve a remarkable balance between small silicon area, high SNR, large dynamic range, and high output impedance. They are therefore a good choice for on-sensor analog image processing applications that use smart pixels operating in current mode.

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