An Implementation of Hot-swap Circuit with High Reliability

Dagang Li[a,b], Zehong Li[a], Wei Li[a], Hua Fan [a,*], Ce Wang[b], Hongrui Che[b], Xuanhong Zeng[b], Quanyuan Feng[c], Hadi Heidari[d]

[a]*School of Electronic Science and Engineering, University of Electronic Science and Technology of China, Chengdu, China*
[b]*Chengdu Sino Microelectronics Technology Co.,Ltd, Chengdu, China*
[c]*School of Information Science and Technology, Southwest Jiaotong University, Chengdu 611756, China*
[d]*Electronics and Nanoscale Engineering Division, School of Engineering, University of Glasgow, G12 8QQ, Glasgow, UK*

Abstract

For the information transmission and application field of the bus, it is necessary to design a bus transceiver with high reliability and hot-swap ability. In order to achieve this requirement, this paper proposes a novel transceiver circuit with hot-swap structure. This structure effectively improves the transistor utilization efficiency and reduces the chip area on the premise of achieving the hot-swap performance. Furthermore, the traditional Schottky diode is avoided, and the hot-swap circuit proposed in this work can be implemented in any CMOS process. A prototype was fabricated in CSMC $\mathbf{0.5\mu m}$ CMOS technology, and the measurement results match well with the simulation results show that the chip meets the design requirements.

Keywords: Hot-swap, Bus Transceiver, High-impedance state, Schottky diode.

1. Introduction

The bus is a common transmission line for transmitting information widely used in modern complex electronic systems. It generally includes data bus, address bus and control bus. The data bus commonly adopts a many-to-one trans-

*Corresponding author
Email address: fanhua7531@163.com (Hua Fan)

mission. In the design and application of new-generation electronic products, there is often a need for an interface circuit for level shift and data transmission due to different voltages between systems. A bus transceiver is such a circuit that, in the case of many-to-one and time-sharing transmission, if the data path is not strobed, the path is in a high-impedance state and acts as an isolator; when the path is strobed, the path provides level shifting and driving. This application requires the bus transceiver to have a hot-swap ability[1, 2, 3].

The conventional hot-swap circuit always relies on the schottky diode, always has a large area and a single function [4, 5]. In this work, a new structure without schottky diode is proposed, and the components of the hot-swap can be reused. The hot-swap circuit proposed not only effectively prevents the signals on the bus from coupling into the chip through the parasitic diode, but also modulates the threshold voltage in response to the driving current so as to improve the driving ability, which finally has reduced the chip area, improved the driving capability, and effectively decreased the product cost.

2. Design of transceiver with hot-swap ability

In the actual application of the interface circuit, as shown in the Fig. 1(a), it is usually required that multiple bus IO chips are simultaneously connected to the bus, and some bus IO chips that do not need to transmit data temporarily are in a sleep or power off state to reduce system power consumption. Some IO chips need to be hot-swapped in special applications, which requires the port of the IO chip to have hot-swap capability. The hot-swap ability is reflected in the isolation capability of the chip to the bus port, that is, the chip should not have the ability to interfere with the bus when it doesn't work (especially when the chip is powered off and powered on). Fig. 1(b) shows the unprocessed conventional output port of IO chip. Once V_{cc} is grounded, the voltage of the bus is connected to V_{cc} through the drain parasitic PN junction (D0) of the PMOS (P0). This path can seriously interfere with the bus signal and even change the bus level. Therefore, it is necessary to process the port of the IO chip.

Since the bus voltage is always greater than or equal to the ground potential (GND), the pull-down transistor (N0) does not have an output-to-ground path in the event of a power-off, so the IO circuit only process the pull-up transistor (P0). The driver MOS of the IO port is in a state of high-impedance when

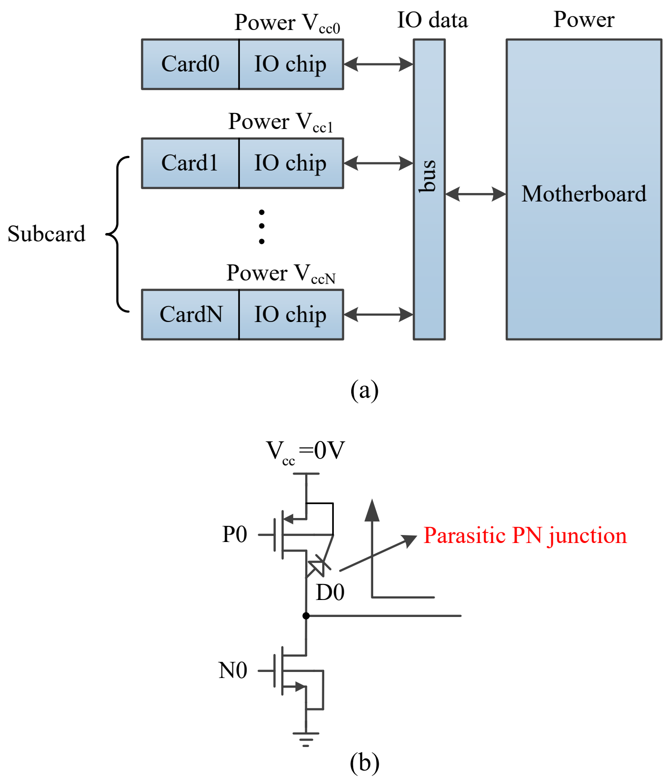


Figure 1: (a) Practical application environment of IO chip. (b) Unprocessed conventional output port of the IO chip.

there is no current between the source and drain. Fig. 2 shows the schematic diagram of PMOS transistor. To ensure PMOS is in a high-impedance state, on the one hand, the MOS transistor is in an off state, that is, the gate-source voltage V_{gs} should be close to 0 (the MOS transistor is a bidirectional device, and the source is defined by the actual current flow direction); on the other hand, parasitic PNP effect should be isolated. In summary, an effective method is to select the higher voltage of V_d and V_s as the substrate potential V_b and the higher voltage of V_d and Vs as the gate potential V_g, which can block the current between source and drain. Next, we will discuss the implementation of the above methods in detail.

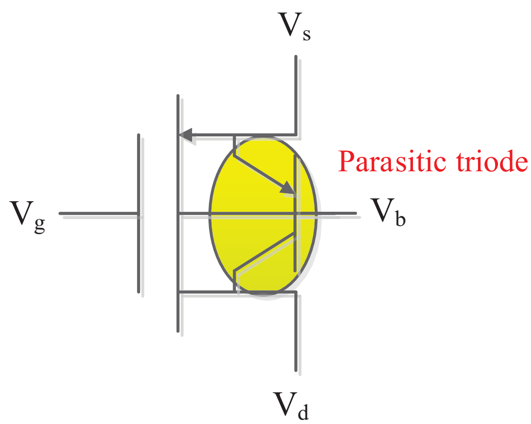


Figure 2: The schematic diagram of PMOS transistor.

The implementation of the hot-swap ability mainly includes two modules: the I_{off} function module and the power-up tri-state module. The I_{off} module realizes the function that when $V_{cc} = 0V$, the port is in high-impedance state. While the power-up tri-state module realizes hot-swap function, if the power supply voltage of the IO chip does not reach the expected value, the IO port in contact with the bus maintains a high-impedance state, as shown in Fig. 3. In addition, there is another case in which the port is in a high-impedance state, the EN (enable) signal forces the port to be in a high-impedance state.

The conventional processing scheme of output power transistor is shown in Fig. 4(a), the substrate potential generating circuit is composed of D0 and P1, and D0 is a Schottky diode. The function of the LOGIC 1 module is to invert the input signal (IN) through the V_{ug} port to make transistor P0 turn on and off, and the chip select signal S/SN is used as the enable signal of the module.

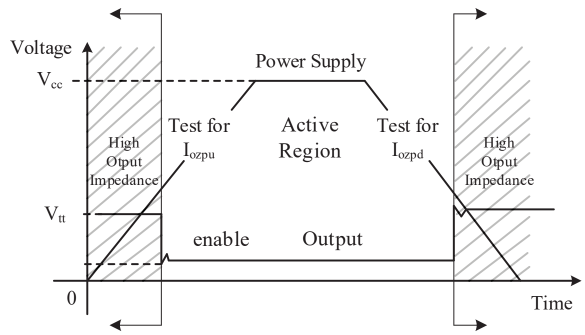


Figure 3: Schematic diagram of power-up tri-state[6].

The function of the LOGIC 2 module is the same as LOGIC 1, the input signal (IN) is inverted to output through the V_{dg} port to control the opening of the N0, the enable signal of LOGIC 2 is still the chip select signal S/SN. When the circuit normally transmits signals, as shown in Fig. 4(b), P1 is turned off, D0 is turned on, and provides the substrate potential V_{pb} for P0, and V_{pb} also supplies the power for the LOGIC 1 module. When the power supply is powered off, as shown in Fig. 4(c), $V_{cc} = 0V$, P1 and P2 are turned on, provide the substrate potential and the gate potential for the P0 respectively, so that P0 is turned off.

The advantage of the conventional processing method at the output of the interface circuit is that the circuit is simple and easy to implement; while the disadvantage is that not all CMOS process can provide Schottky diodes. Moreover, the Schottky diode D0 of this structure occupies a certain chip area, and the generation of substrate potential of P0 increases the design complexity to some extent.

To address this problem, Fig. 5(a) is a hot-swap circuit of the IO port proposed in this paper. Compared with the conventional circuit in Fig. 4, the hot-swap processing circuit proposed integrates the substrate potential generating circuit and the output driving transistor to provide the current driving

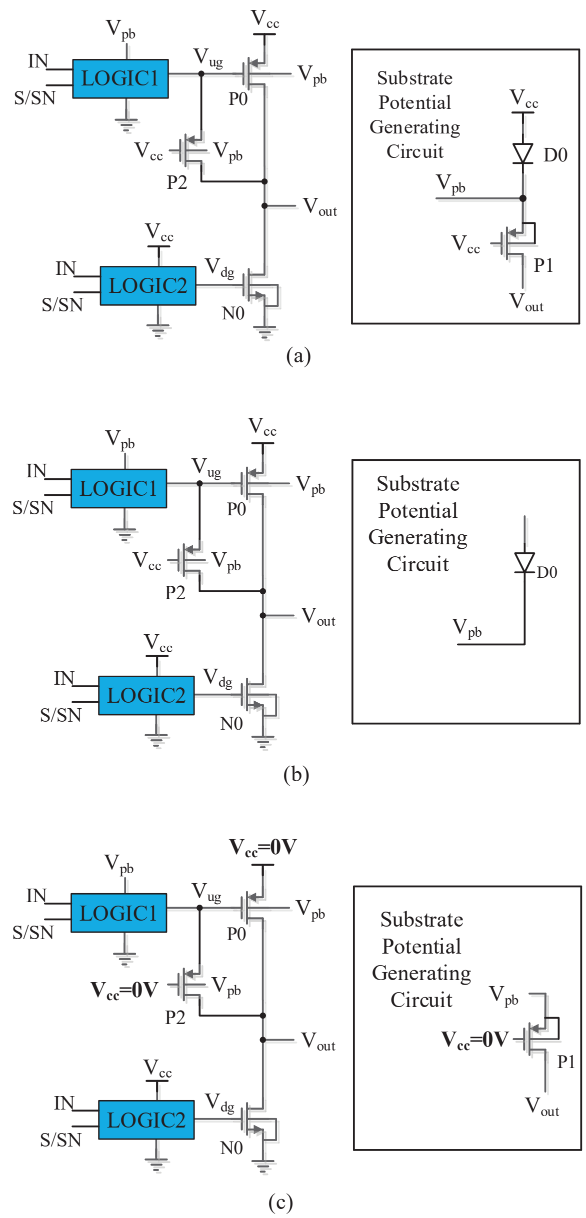


Figure 4: (a) Conventional processing method of interface chip. (b) Working principle of normal signal transmission. (c) Working principle of power-off.

capability of the IO port. At the same time, in the case of large current, the substrate bias voltage V_{pb} will drop to bring about a significant MOS threshold voltage modulation effect, so that the output driving transistor has a stronger current driving capability. In this way, in the case of the same chip area, the circuit proposed can achieve stronger current driving capability; in addition, no Schottky diode is applied in this design. The circuit only uses MOS devices, which can be implemented in any CMOS process.

The working principle is as follows: LOGIC 1, LOGIC 2 modules have the same function with LOGIC 1 and LOGIC 2 in Fig. 4. When the circuit normally transmits signals, as shown in Fig. 5(b), the output voltage will dynamically turn on N1, so that the gate voltage of P1 always maintain the ground potential, $V_{pb} \approx V_{cc}$, not only provides the substrate voltage for the pull-up PMOS transistor (P0), but also provides the substrate voltage for the P1 itself, and the P1 transistor is in the normally on state. When the output voltage becomes high, the current of P1 will flow to the load through the P2, providing additional driving current for the output. When the chip outputs a low level, $V_{dg} = V_{cc}$, N0 is turned on, $V_{ug} = V_{pb}$, P0 and P2 are in off state, $V_{out} = 0V$. When the circuit is in power-off state, as shown in Fig. 5(c), $V_{cc} = 0V$, at this time the chip output should be in a high-impedance state, because the power supply voltage $V_{cc} = 0V$, $V_{dg} = 0V$, the pull-down transistor N0 is in off state. Since the output terminal is connected to the bus, V_{out} may be in high level or low level. When V_{out} is low, since $V_{cc} = 0V$, P0, P1, and P2 are all in off state, the output is in a high-impedance state. When V_{out} is high, V_{ug} and V_{pb} are both high, P0, P1, and P2 are off, and the output is in a high-impedance state.

Furthermore, the power detection module implements the tri-state function. When EN is low (enable is inactive), the circuit is forced to operate in a high-impedance state. When V_{cc} is not powered up to the specified potential, the power detection module forces circuit to operate in a high-impedance state. The indication signal of the circuit in high-impedance state is S = GND.

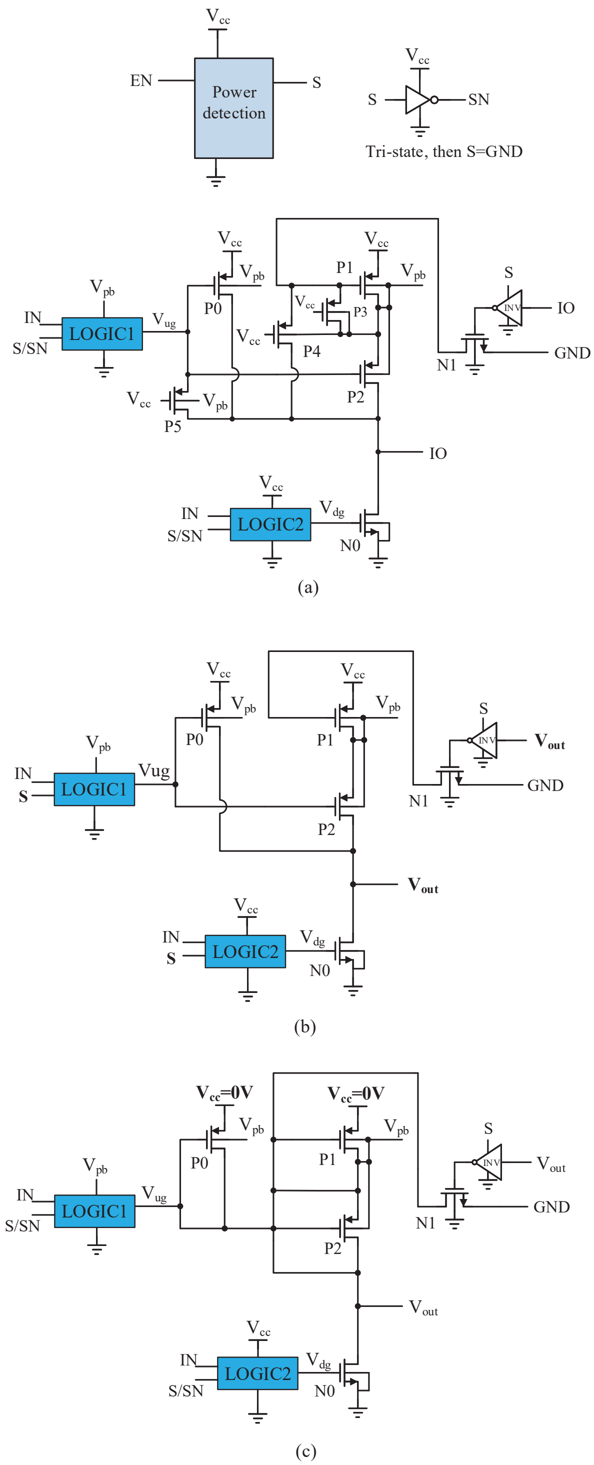


Figure 5: (a) The proposed hot-swap circuit. (b) Working principle of normal signal transmission. (c) Working principle of power-off.

3. Simulation and measured results

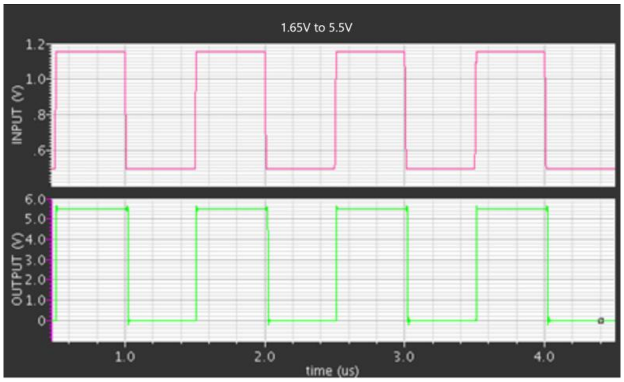
The function of bus transceiver is simulated by Cadence Spectre in CSMC 0.5μm CMOS technology. The simulation results under three conditions with 1MHz of input frequency are shown in Fig. 6. In Fig. 6(a), the input power supply voltage V_{cca} is 1.65V and the output power supply voltage V_{ccb} is 5.5V. According to the general definition of high and low levels, the input low level is 0.495V (0.3×1.65V) and the input high level is 1.155V (0.7×1.65V), which demonstrates that the bus transceiver designed in this work functions well in a wide voltage range of 1.65V $\sim$ 5.5V.

Layout design is an important part of the transceiver design, which directly determines the cost and performance of the chip[7, 8]. Fig. 7 shows the overall layout of the transceiver, it is a 16 channels transceiver with a total area of 4.39mm $\times$ 1.34mm.

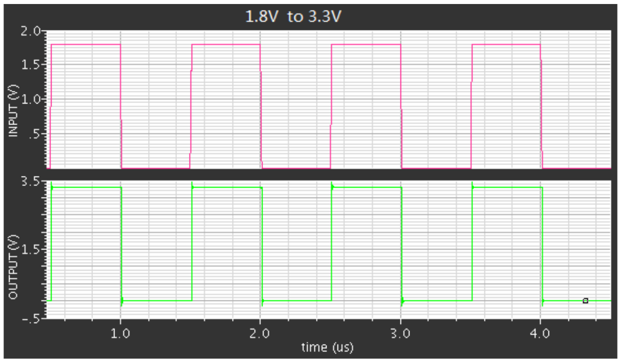
Fig. 8 shows the chip photo. The measured results are shown in Fig. 9, which are consistent with the simulation results shown in Fig. 6(b) and (c). Also, the measured results meets the design requirements of the whole system. Table 1 shows the performance of bus transceiver under various supply voltages from 1.65V to 5.5V.

4. Conclusion

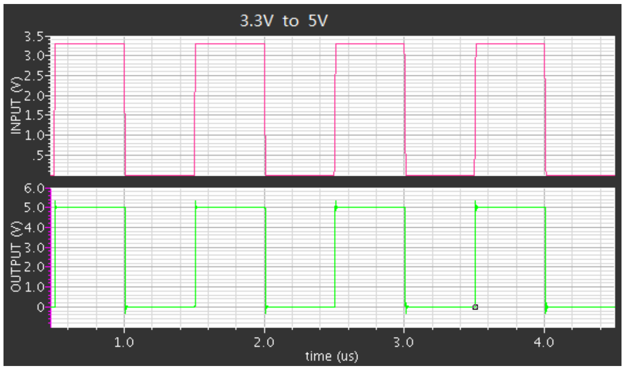
This paper describes the design of a wide-voltage range bus transceiver, details the principle and implementation of the hot-swap circuit in the transceiver, and proposes a new structure based on the conventional processing, which can reduce the chip area to some extent and increase the output driving efficiency of the chip. The simulation results and tapeout of the circuit are given, it can be seen from the test results that the transceiver designed in this paper realizes all functions. Compared with the traditional structure, the parameters are obviously improved and the chip area is reduced.



(a)



(b)



(c)

Figure 6: Transient simulation results with 1MHz of input frequency: (a) $V_{cca} = 1.65V$, $V_{ccb} = 5.5V$. (b) $V_{cca} = 1.8V$, $V_{ccb} = 3.3V$. (c) $V_{cca} = 3.3V$, $V_{ccb} = 5V$.

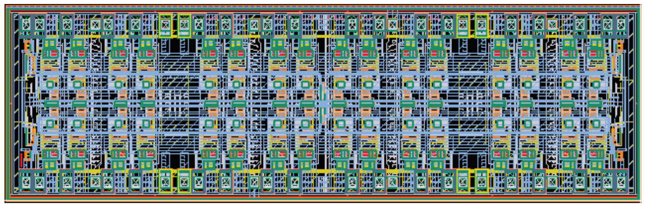


Figure 7: Layout of 16 channels transceiver.

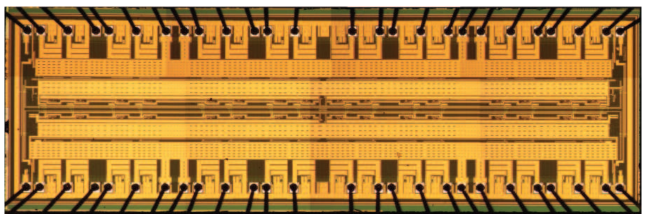


Figure 8: Chip photo of 16 channels transceiver.

Table 1

Performance table

	Condition	Proposed structure
Chip area		4.39mm × 1.34mm
Transmission delay (t_{PD})	25°C, $V_{cca} = 1.65V$, $V_{ccb} = 2.5V$	3.5ns
	25°C, $V_{cca} = 1.65V$, $V_{ccb} = 3.3V$	3ns
	25°C, $V_{cca} = 1.65V$, $V_{ccb} = 5.5V$	2.5ns
Output high level (V_{oh})	25°C, $V_{cco} = 1.65V$, $I_{oh} = 4mA$	1.53V
	25°C, $V_{cco} = 2.3V$, $I_{oh} = 8mA$	2.1V
	25°C, $V_{cco} = 4.5V$, $I_{oh} = 32mA$	4.1V

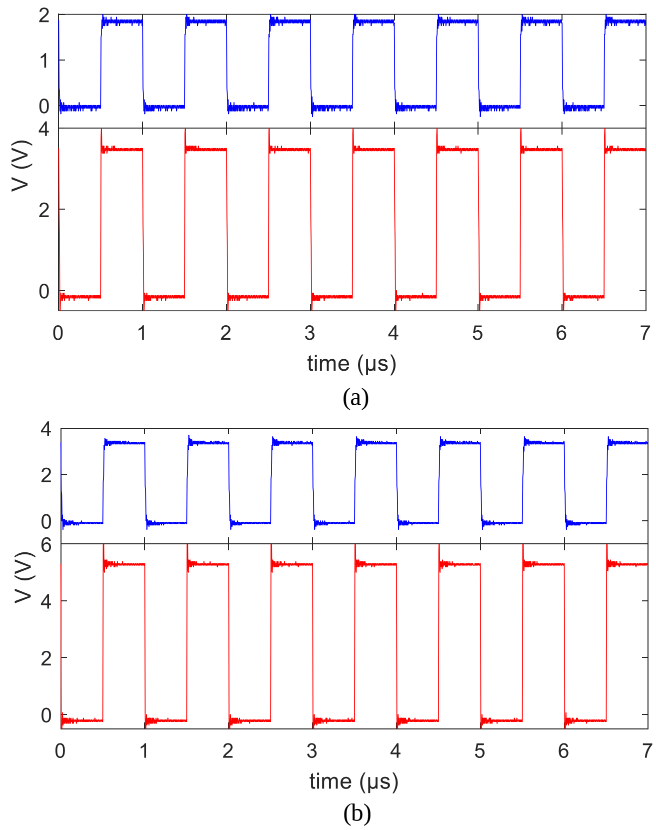


Figure 9: Transceiver measured results with 1MHz of input frequency: (a) $V_{cca} = 1.8V$, $V_{ccb} = 3.3V$. (b) $V_{cca} = 3.3V$, $V_{ccb} = 5V$.

Acknowledgment

The work of Hua Fan was supported by the National Natural Science Foundation of China (NSFC) under Grant 61771111, supported by Sichuan Provincial Science and Technology Important Projects under Grant 19ZDYF2863, as well as supported by China Postdoctoral Science Foundation under grant 2017M612940 & 2019T120834 and Special Foundation of Sichuan Provincial Postdoctoral Science Foundation.

The work of Quanyuan Feng was supported by the National Natural Science Foundation of China (NSFC) under Grant 61531016, supported by Sichuan Provincial Science and Technology Important Projects under Grant 2018GZ0139, 2018ZDZX0148 and 2018GZDZX0001.

The work of Hadi Heidari was supported by the Royal Society under grant RSG\R1\180269 and EP/R511705/1 from the EPSRC, United Kingdom.

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