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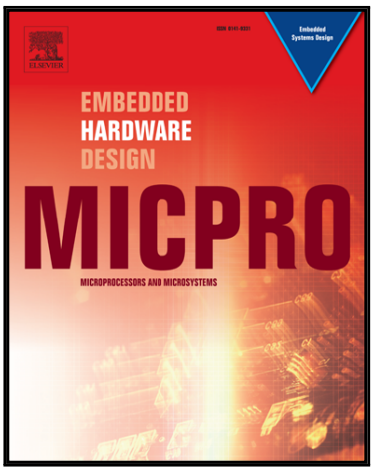

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Jens Sparsø

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Special issue:

Selected papers from the 2nd IEEEE Nordic Circuits and Systems Conference (NorCAS), 2016.

This special issue includes selected papers from the 2nd IEEEE Nordic Circuits and Systems Conference (NorCAS), held in Linköping, Sweden, October 24-25, 2016. The IEEE NorCAS conference is the main circuits and systems event of the Nordic and Baltic countries representing both academia and the electronics industry. The NorCAS conference emerged in 2015 from the merger of the Norchip conference held annually in different Nordic and Baltic countries since 1983, and the International Symposium on Systems on chip held annually in Tampere, Finland since 1999.

As the name of the conference hints, it has a rather broad scope within electronics, ranging from analog and digital circuit design to systems and applications. Papers are submitted to one of three tracks: analog, digital and systems-on-chip. This special issue include papers from the, digital and systems-on-chip tracks.

Nine of the top rated papers accepted the invitation to submit an extended version to this special issue. These papers have been subject to the regular MICPRO review process. In the end, after two rounds of reviewing, four papers were accepted for this special issue.

A brief introduction to the selected papers follows.

The first paper is “Sensor Data Fusion in the Context of Electric Vehicles Charging Stations using a Network-on-Chip” authored by Ivan Stoychev, Philipp Wehner, Jens Rettkowski, Tobias Kalb, Patrick Wichert, Diana Göhringer and Jürgen Oehm from Ruhr University Bochum and TU Dresden, Germany. It is an application paper exploring the use of a network-on-chip based multi-core processing platform to simulate a charging station for electric cars. The charging station use sensor data fusion techniques and this is handled by using multiple processor cores. The system uses an ARM processor and a number of Microblaze processors as well as dedicated hardware. The system is both simulated using the MPSoCSim simulater extended with processor models from Open Virtual Platforms (OVP), and implemented on a Zilinx Zync FPGA board.

The second paper is “Energy Efficient Wearable Sensor Node for IoT-based Fall Detection Systems ” authored by Tuan Nguyen Gia, Victor Kathan Sarker, Igor Tcarenko, Amir M. Rahmani, Tomi Westerlund, Pasi Liljeberg and Hannu Tenhunen from University of Turku, Finland, University of California, Irvine, USA and TU Wien, Austria. It is an application paper exploring the design of a wearable fall detection sensor node that can be used in an internet-of-things context. Should the person wearing the device fall it detects this and sends an alarm. This can be relevant for elderly people living alone, and the ability to react quickly influences the prospects for recovery. The paper explains the design and the underlying design decisions and presents a prototype implementation. Focus is on battery lifetime and minimization of energy consumption.

The third paper is “Application-Specific Architectures for Energy-Efficient Database Query Processing and Optimization” authored by Stefan Scholze, Sebastian Höppner, Annett Ungethüm, Christian Mayr, René Schüffny, Wolfgang Lehner, and Gerhard Fettweis from TU Dresden, Germany. The paper explores acceleration of database queries by extending an existing processor with special instructions for this. The work uses the Tensilica processor from Cadence. The resulting application specific instruction set processor (ASIP), is implemented in a 28 nm CMOS technology, and the paper include measured results on power and performance.

The fourth and last paper is “Ultra-Low Voltage and Energy Efficient Adders in 28 nm FDSOI Exploring Poly-Biasing for Device Sizing” authored by Ali Asghar Vatanjou, Even Laate, Trond Ytterdal and Snorre Aunet, all from the Department of Electronic Systems, Norwegian University of Science and Technology (NTNU) . Ultra low power design using near-threshold or sub-threshold operation is currently an active area of research. The paper explores the design and optimization of adders operating in this regime using a 28 nm FDSOI technology. The paper reports both simulated and measured results on energy and performance.

On behalf of the editorial board I want to thank the authors for submitting their work to Microprocessors and Microsystems. I would also like to thank the reviewers for their feedback that helped improve the quality of the final published manuscripts. Finally I would like to thank the Elsevier staff for guiding me through the workflow in the EVISE system.

Guest editor

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Jens Sparsø is Professor in Cyber-Physical Systems at the Technical University of Denmark (DTU). His research interests include: design of digital circuits and systems, design of asynchronous circuits, low-power design techniques, application-specific computing structures, computer organization, multi-core processors, and networks-on-chips – in short hardware platforms for embedded and cyber-physical systems. He has published more than 90 refereed conference and journal papers and is coauthor of the book ``Principles of Asynchronous Circuit Design - A Systems Perspective'' (Kluwer, 2001), which has become the standard textbook on the topic.

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