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Experimental and Numerical Investigations on Delayed Short-Circuit Failure Mode of Single Chip IGBT Devices

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Abstract

This paper presents experimental and numerical investigations on the delayed failure mode of IGBT devices observed under short-circuit operations. For short-circuit energies lightly higher than a critical value, the default current may be successfully turned-off but a leakage current takes place leading to a thermal runaway and finally to a delayed failure. Numerical investigations have been carried out and a detailed analysis of the physical mechanisms occurring during the delayed failure mode is presented. We show that the classical short-circuit failure mode (energy limited) is a limit case of the delayed failure mode with zero delay time to failure. So, the analysis is extended to the energy limited case and give better understanding of the failure process of this last failure mode. An electro-thermal model including the device and the solder layer is presented as well as all leakage current components models like saturation, thermal and avalanche generation currents. A detailed description of the thermal runaway is given and main parameters influence on critical energy value are presented, especially, case temperature and solder layer thickness. Finally, numerical results allow to show that the critical energy which separates two failure modes corresponds to a threshold temperature of about 650^oC in the vicinity of the junction location which seems to be independent of test conditions.

Key words: IGBT, short-circuit, power devices, thermal runaway, thermal modeling.

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1 Introduction

Hard working conditions may be subjected repetitively to power semiconductor devices, like short-circuit or avalanche operations, depending on the application circuit and its environment. This is the case, for example, for integrated power converters in hybrid electric vehicles (HEV) applications where Insulated Gate Bipolar Transistors (IGBT) power modules are used in high bus voltages across the terminals (400V) where they are required to switch on and off rated current. Thus, the use of standard devices with 600V breakdown voltages makes them vulnerable to hard working operations such as short-circuit. So, it is of the first importance to carry out investigations on the behavior of power devices under such severe repetitive working operations.

Many papers have been published on the topic of the behavior of IGBT devices under short-circuit conditions [1-8]. Recently, some of them have described the influence of repetitive short-circuit operations in device lifetime and reliability either in multichip power module package [5] or in single ship devices in TO247 packages [7,8] as our concern.

In a previous paper [8], we have described results concerning the effect of repetitive short circuit conditions in the lifetime of IGBT devices according to the energy level. As shown in Fig.1, in a schematic short-circuit robustness figure, it has been pointed out a critical energy (E_C) which distinctly separates two failure modes. The first one occurs for energies below the critical value (I) : devices can withstand a large number of short-circuits before failure with a cumulative damaging mechanism and a destruction phenomenon which looks like dynamic latch-up [4,8]. The second one occurs for energies higher but close to E_C (II) : devices fails at the first short-circuit test in a *"delayed failure mode"*. A tail current takes place after the turn-off process of the device and leads to a destructive thermal runaway phenomenon after several hundreds of microseconds [4-8]. For energies significantly higher than the critical value, the classical "energy limited" failure mode [2] is observed.

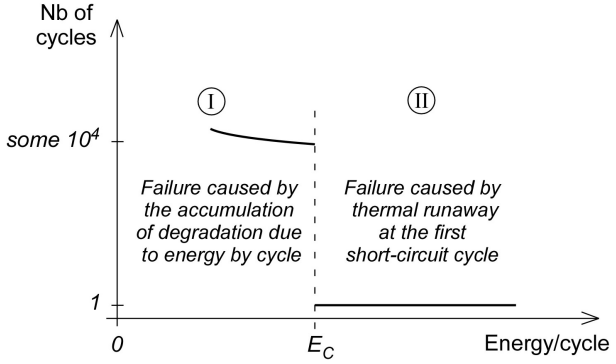

Fig. 1. Schematic short-circuit robustness figure.

In this paper, we focus in region (II), for energies equal or lightly higher than the critical value. On the basis of experimental measurements and numerical simulations, the critical energy and the delayed failure mode are especially analyzed and discussed. The thermal runaway, due to the positive feedback of heat generation by the leakage current of the device, has been particularly detailed and discussed. 600V Punch Through (PT) and Non Punch Through (NPT) as well as 1200V NPT IGBTs have been tested but only the NPT devices are discussed in this paper. In order to avoid any problem linked to the energy distribution in multi-chip devices we have chosen to perform tests on single chip IGBT devices. Even if the *"delayed failure mode"* have been reported by some authors [4,6-8], we propose some hypotheses of the physical mechanisms that should be involved in this failure process. Especially, we discuss how the heat wave acts on the diffusion component of the leakage current and may lead, or not, to the thermal runaway. The frontier between these two possibilities is the limit case which corresponds to the critical short-circuit energy.

2 Experimental Results

The test circuit as well as experimental protocols and results have been fully described in a previous paper [8]. Nevertheless, the main points are recalled in the following. Tests consist in repetitive short-circuits with the same energy, dissipated in the device under test (DUT), until destruction. We proceeded like this to many tests at different energy levels and package temperatures and we observed the number of cycles supported by the devices until failure. A repetitive cycle of 3 seconds has been chosen in order to avoid the average overheating of the chip. A heating plate allows to consider the device packages temperature influence, especially at 25^oC and 125^oC. The dissipated energy is controlled by supply voltage of the test circuit and by the short circuit duration t_{SC}. The tested devices, presented in this paper, are single chip devices 600 V NPT IGBTs from Infineon (SGW15N60) in TO247 package.

As illustration, the obtained results concerning the robustness in short-circuit repetitive conditions for these devices under 400V at 125^oC case temperature are plotted in figure 2. The critical energy E_C depends on the tested device and on test conditions [8]. For this case temperature, the critical energy value (E_C) is 0.62 Joules.

As visible in this figure, for $E > E_C$, only one short-circuit is supported by the devices during which failure occurs. Points (a) to (i) correspond to devices which have failed in the delayed mode as shown in figure 3 where short-circuit currents waveforms are given. Point (j) corresponds to the "energy limited" failure mode.

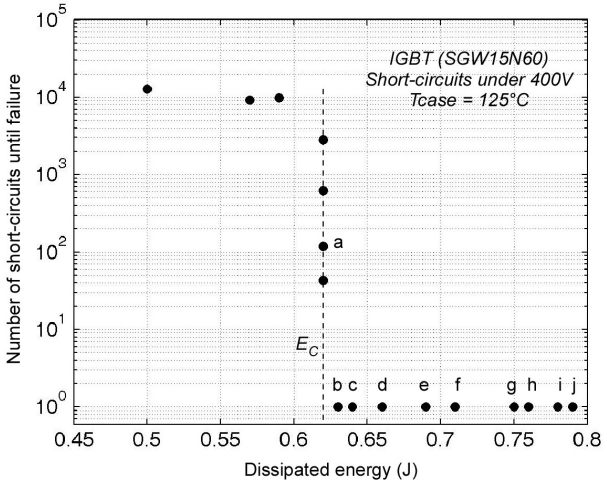

Fig. 2. Robustness in repetitive short-circuit conditions of 600V NPT IGBT.

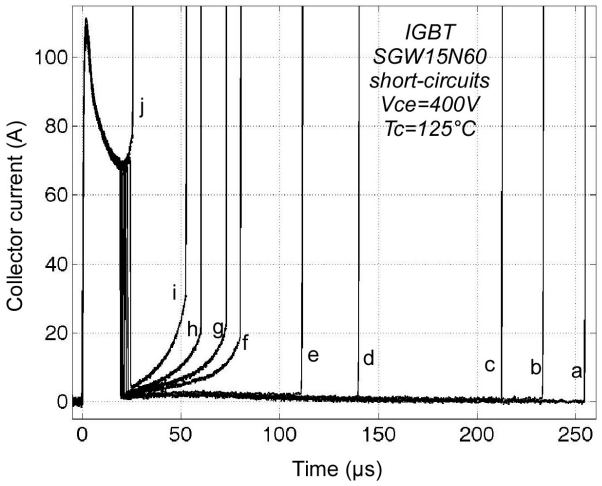

Fig. 3. Experimental short-circuit current waveforms for SGW15N60 devices under 400 V at 125^oC and for different short-circuit durations t_{SC}: (a) 19μs; (b) 19.2μs (d) 19.5μs; (e) 20μS; (f) 20.5μs; (g) 21.5μs; (h) 22.5μs; (i) 24μs.

For each current curve of Fig.3, the short-circuit duration (t_{SC}), related to the energy, is given. When the short-circuit energy is higher but close to E_C, at the first test, a tail current takes place after the turn-off process of the device and leads to a thermal runaway phenomenon. The failure occurs after a delay time (t_{df}) after the device has been switched off [8]. This phenomenon has been observed by some authors [5-9]. We observed, that the tail current level, just after the device is turned-off, and the delay time to failure (t_{df}) are energy dependent or more precisely device temperature dependent at the turn-off time. The higher the energy is, the higher the tail current level is and the shorter the delay time to failure is. For points (b) to (i), the short-circuit energy is higher than the critical value and the failure occurs at the first test. For point (a), at the critical energy value ($E = E_C$), the device is able to support many short-circuits before to fail in the delayed mode at the last test.

It has been shown in [8] that for high energy tests, tail currents may be very high and t_{df} tends to very short values. The limit case is for point (j) where the delay time is zero.

3 Electrothermal Model and Simulation Results

3.1 Methodology

For this modelling, we have focused on two objectives :

- The evaluation of the temperature distributions within the device during and after the short-circuit ;
- The computation of the leakage current evolution after the short-circuit current has been turned-off.

Consequently, the simulation process may be divided in two successive periods :

- The first one occurs during the short-circuit operation ($0 < t \leq t_{SC}$). Temperature distribution within the device are computed with collector current and collector voltage experimental evolutions ($I_C(t)$ and $V_{CE}(t)$). During, this period, the simulation is purely thermal.
- The second period starts at the turn-off time ($t > t_{SC}$). The collector current, due to the leakage current, is calculated with the temperature distribution within the device. Then, an electro-thermal simulation is used in order to compute the evolution of the coupling between the leakage current and temperature distributions within the device.

As said above, the dissipated energy is controlled by the short circuit duration t_{SC}. So, the current and voltage waveforms during short-circuits remain quite identical until the turn-off time (t_{SC}), as visible in Fig.3. So, short-circuit current and voltage experimental waveforms have been recorded and used as a basis for the first period purpose ($0 < t \leq t_{SC}$). These waveforms have been obtained for a very large short-circuit duration leading to an energy limited failure mode. From this current waveform, we can numerically simulate any short-circuit duration (t_{SC}) until $26\mu s$ (see Fig.3) and compute the temperature distributions until this time (first period). Then, the electro-thermal model may be used in order to compute the leakage current at the chosen turn-off time and its evolution after t_{SC}.

3.2 Thermal Model

A simplified 1D thermal model was used in order to estimate the temperature distributions in the device during and after short-circuit pulses. The device structure is a single silicon chip attached to the case by a solder material in TO247 package. The die width (W_{si}) and the solder layer width (W_{sld}) are visible in the schematic model in Fig.4.

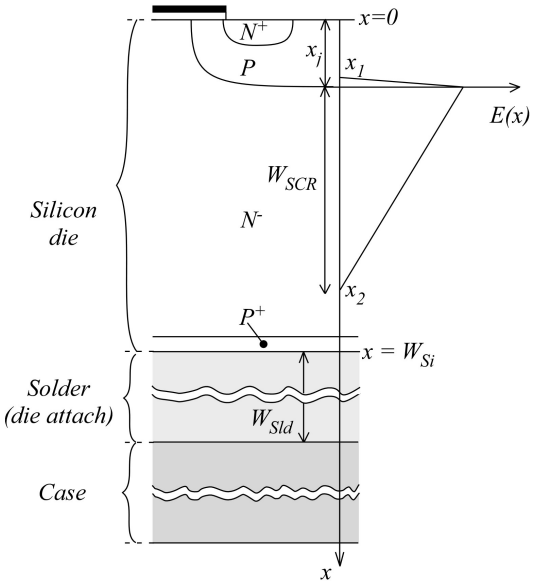

Fig. 4. IGBT thermal model.

The 1D approximation is justified because the thermal flow essentially occurs in one dimension and can affects the silicon chip and possibly the underneath solder layer if the heat transfer is long enough. Very high temperature values are reached by the silicon chip during short-circuit operations whereas the temperature variations of the solder layer remain relatively low. So, temperature dependence of the thermal conductivity and heat capacity of silicon must be taken into account in the thermal model and constant thermal properties are kept for the solder layer. The classical heat equation is solved over the thermal system composed by silicon die and the solder layer :

$$\frac{\partial}{\partial x}\left(\lambda(T)\frac{\partial T}{\partial x}\right) + Q(x,t) = \rho\, c(T)\,\frac{\partial T}{\partial t} \tag{1}$$

where $T(x)$ is the temperature distribution along the x axis, ρ, λ and c are respectively material density, local thermal conductivity and thermal capacity. $Q(x,t)$ is the heat generation source due to the power dissipation responsible for the thermal increase in the silicon chip. The material properties of the model are given in table 1. The chip depth, active area and total area, given in

table 2, were obtained from the device data sheet [9] for SGW15N60 devices. The solder layer thickness (W_{sld}) has been fixed arbitrarily at the realistic value of $100\mu m$.

Table 1
Material properties [2,14].

	silicon	solder
$\rho\,(Kg.m^{-3})$	2320	7400
$\lambda\,(W.m^{-1}.K^{-1})$	$(3\,10^{-4} + 1.56\,10^{-5}T + 1.65\,10^{-8}T^2)^{-1}$	50
$c\,(J.Kg^{-1}.K^{-1})$	$849\ + 0.155\,T - 1.6\,10^{7}\,T^{-2}$	190

Table 2
Given datasheet parameters [9].

Parameter	SGW15N60
W_{si} (μm)	100
Die active area (mm^2) S_a	10.7
Die total area (mm^2) S	14.4

The heat source is $Q(x,t) = E(x,t) \cdot J(t)$, where $E(x,t)$ is the electric field distribution in the space charge region (SCR) (voltage dependent) and $J(t)$ is the time dependent current density. $J(t)$ is given by experimental measurements for $0 < t \leq t_{SC}$ and by the calculated leakage current for $t \geq t_{SC}$. In spite of high current densities during short circuit operations, we suppose that the electric field distribution is not perturbed by the carrier flows. This assumption, verified in the literature by 2D physical simulations [2], assumes that holes and electrons flows are quite equal in the SCR during the short-circuit operation. Unfortunately, we had no informations concerning the internal structure data parameters, junction depth and N-base impurity concentration. Nevertheless, the blocking voltage of the NPT devices allows us to estimate in one hand x_j at about $10\mu m$ and on the other hand base doping (N_D) at about $2\times10^{14}cm^{-3}$ for the SGW15N60 (600V) devices. The SCR width W_{SCR}, defined by x_1 and x_2 (Fig.4), depends on the sustained voltage during short-circuits and bulk doping.

The initial condition is given by : $T(x, t = 0) = T_C$, which assumes temperature equilibrium at the case temperature. Isothermal temperature at a constant case temperature value is used as a boundary condition at the bottom side of the model : $T(x = W_{Si} + W_{Sld}, t) = T_C$. The heat flux is assumed to flow from the heated device to the thermal heat-sink and thus we assume that no heat transfer occurs through the top surface of the silicon die. So, adiabatic conditions are applied at this location : $\lambda\,(\partial T/\partial x)_{x=0} = 0$. Then the heat equation is solved by using the finite difference method.

3.3 Leakage Current Model

The leakage current is a combination of the thermal generation current (I_g^{th}), the avalanche generation current (I_g^{av}) and saturation (or diffusion) current (I_s) :

$$I_{leak} \approx I_g^{th} + I_g^{av} + I_s \tag{2}$$

If we assume S is the junction area and q the elementary charge, the two first components are obtained by integrating the associated generation rate through the space charge region, between x_1 and x_2 (see Fig.4) :

$$I_g^{th} = \int_{x_1}^{x_2} q \, \frac{n_i}{\tau_e} \, S \, dx \tag{3}$$

$$I_g^{av} = \int_{x_1}^{x_2} (\alpha_n |J_n| + \alpha_p |J_p|) \; S \, dx \tag{4}$$

The saturation current is given by the sum of the two terms at the SCR edges, I_{s1} and I_{s2}, respectively at x_1 and x_2 :

$$I_s = I_{s1} + I_{s2} = qS \left(\frac{n_i^2 \, D_n}{L_n \, N_A} \right)_{x_1} + qS \left(\frac{n_i^2 \, D_p}{L_p \, N_D} \right)_{x_2} \tag{5}$$

Concerning the thermal generation current, n_i is the intrinsic carrier density which is given with temperature dependence by : $n_i(T) = A.T^{3/2} exp(-E_G/2kT)$. For numerical calculations, n_i may be given in (cm^{-3}) for $A = 3.8{\times}10^{16} cm^{-3}.K^{-3/2}$ and energy bandgap is $E_G = 1.2 \; eV$ [10]. The temperature dependence of the thermal generation time constant τ_e is given by [11,12] :

$$\tau_e(T) = B \sqrt{T} \, exp(\Delta E/kT) \tag{6}$$

where k is the Boltzman's constant and activation energy ΔE is typically 0.1 eV [11]. The constant B has been taken equal to 10^{-7} SI in order to get realistic values.

Concerning the avalanche generation current, as assumed in the previous paragraph, the carrier current densities are assumed equal in the space charge region of the device. In the high electric field region of the SCR, these current densities are quite constant and in order to be in the worst case we have assumed $J_n = J_p = J/2$ where J is the total current density. The carrier ionization coefficients (α_n and α_p) relations have been chosen to be dependent

not only with electric field but with temperature as well [13] in order to have an electro-thermal model of this current component.

Finally, for the saturation current, the minority diffusion length L_p (or L_n) and the diffusion coefficient D_p (or D_n) are temperature dependent through both minority carrier mobility μ_p (or μ_n) and minority carrier lifetime τ_p (or τ_n) [10] :

$$L_p = \sqrt{D_p\,\tau_p} \tag{7}$$

$$D_p = \frac{kT}{q}\,\mu_p \tag{8}$$

$$\mu_p \approx \mu_{po}\,(T/300)^{-2.2} \tag{9}$$

$$\tau_p \approx \tau_{po}\,(T/300)^{2.32} \tag{10}$$

where k is the Boltzmann constant, q the elementary charge, T the absolute temperature, μ_{po} and τ_{po} are respectively the hole mobility and the hole lifetime in the low doped silicon region at 300K. The same expressions may be given for L_n, D_n, μ_n and τ_n in the high doped region (P^+) at x_1. If S is given in cm^2, combining eq.(8) with eq.(10) to (13) and their complements for electron parameters, we obtain the saturation current components I_{s1} and I_{s2} versus temperature, in Amps :

$$I_{s1} \approx 5.35 \times 10^{17}\,\frac{S}{N_A}\,\sqrt{\frac{\mu_{no}}{\tau_{no}}}\,T^{1.25}\,exp\left(\frac{-14000}{T}\right) \tag{11}$$

$$I_{s2} \approx 5.35 \times 10^{17}\,\frac{S}{N_D}\,\sqrt{\frac{\mu_{po}}{\tau_{po}}}\,T^{1.25}\,exp\left(\frac{-14000}{T}\right) \tag{12}$$

Concerning carrier mobilities and lifetimes, in the low doped region (N^- at x_2) μ_{po} is about $450\,cm^2.V^{-1}.s^{-1}$ and τ_{po} has been estimated at $10\mu s$, in the high doped region (P^+ at x_1) μ_{no} is about $800\,cm^2.V^{-1}.s^{-1}$ and τ_{no} has been estimated at $0.2\mu s$.

3.4 Simulation Results

Using the experimental waveforms of Fig.3, we have applied the methodology explained above. From these waveforms, we can "turn-off" numerically the short-circuit current for any duration t_{SC} until the experimental failure at $t = 26\mu s$. During this first period, the thermal model allows to compute temperature distribution evolutions. Then, the electro-thermal model allows to compute the leakage current at t_{SC} and its coupling evolution with temperature.

Fig.5 gives the simulated leakage current behavior for different short-circuit durations t_{SC}. Considering Fig.5a, for $t_{SC} \leq 17.7\mu s$, the leakage current ends to decrease towards zero. It can be noticed the high level leakage current, about 4A just after the switch-off, due to high temperature values within the device. If the short-circuit duration is lightly increased ($t_{SC} = 17.8\mu s, E = 0.57\ J$), we obtain a thermal runaway of the leakage current with a failure occurring about $t_{df} = 780\mu s$ after the turn-off time. This simulation of short-circuit duration corresponds to the simulated critical energy ($E_{Csim} = 0.57\ J$) and these values may be compared to the experimental ones ($E_C = 0.62\ J$ and $t_{SC} = 19\mu s$, see Fig.3). Then, as the short-circuit duration increases, the energy level increases and the t_{df} decreases. The short-circuit energy dependance on delay time to failure (t_{df}) is visible in Fig.6 for both the experimental results (see Fig.3) and the simulated results (see Figs.5a and 5b).

We can observe, in Fig.6, that the calculated and measured curves have vertical asymptotic limit corresponding to the respective critical values of energy (E_C) for which t_{df} have the more important values. On the other hand, for high energy values, t_{df} tends towards zero which is the limit case that corresponds to the limited energy failure shown in Fig.3, curve (j).

In order to understand the physical process of the thermal runaway which occurs during the delayed failure mode at the threshold case of the critical short-circuit energy, we have plotted, in Fig.7, the evolution of temperature distributions inside the structure. The first distribution, at time t_1, is the one which corresponds to the end of the short-circuit (t_{SC}) when current is turned-off. We can observe that at t_1 a maximum value of 600^oC is reached within the space charge region near the junction location whereas temperature at the solder interface has risen lightly. Then as time increases, from t_1 to t_4, the heat wave flows towards the backside of the chip. Consequently, temperature increases at the interface ($x = 100\mu m$) and decreases at the top side ($x = 0$). Then, for time t_5 to t_7, it can be seen that temperature saturates at about 350^oC at the solder interface (temperature distribution becomes linear in the solder) and temperature begins to rise sharply at the top side, especially in the depleted layer of the device.

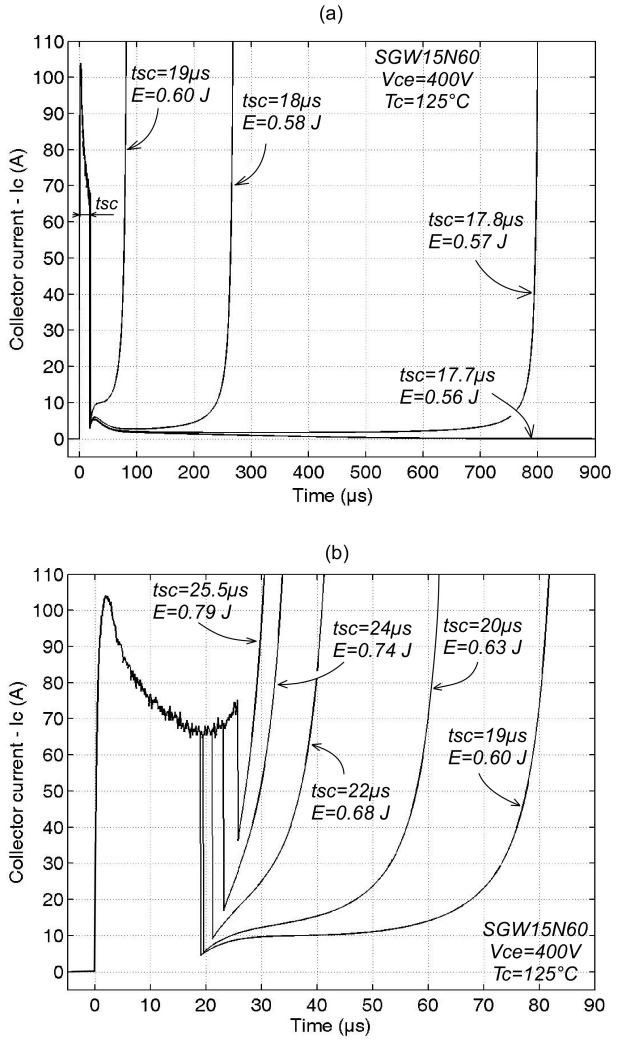

Fig. 5. Leakage current dependance with the short-circuit duration (t_{SC}) and energy (E) for small short-circuit energies (a) and higher short-circuit energies (b).

Fig.8 gives the calculated components of the leakage current during this short-circuit threshold case. We can see the total leakage current after the current switch-off ($t_{SC} = 17.8\mu s$) and the simulated thermal runaway. The different current components are shown : thermal generation I_g^{th}, components of saturation current I_{S1} and I_{S2}. The avalanche generation component is negligible and is not represented here. In addition, Fig.9 gives temperature evolutions, T_1 and T_2, at the space charge layer edges x_1 and x_2 which are used to compute the corresponding values of saturation currents I_{S1} and I_{S2}.

It can be seen that thermal generation remains at low values until $700\mu s$ and the leakage current is composed essentially by the saturation current, I_{S1} at the beginning due to electron diffusion and by I_{S2} after $100\mu s$ due to hole diffusion. These variations may be explained by the corresponding temperature evolutions given in Fig.9. It can be noticed that temperature

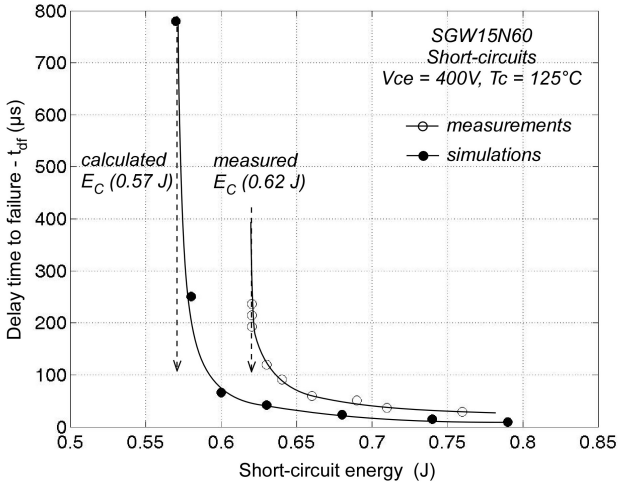

Fig. 6. Dependance of delay time to failure vs. short-circuit energy, comparison between calculated and measured results.

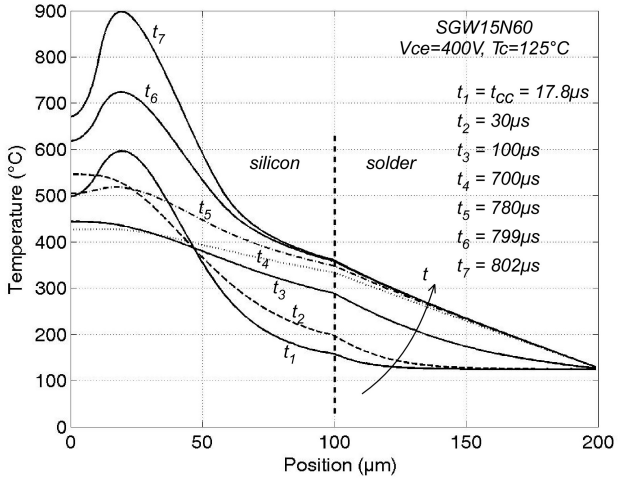

Fig. 7. Calculated evolutions of temperature distributions during the short-circuit at the critical energy.

T_2 has a monotonic increase evolution as well as I_{S2}. The relatively large variations of I_{S1} with T_1 compared to variations of I_{S2} with T_2 is due to the coefficients (i.e. the doping levels and carrier lifetimes) which appear in relations (14) and (15). As we can see, the hole saturation current in the low doped base seems to be responsible of the thermal runaway. This is due to the heat wave generated within the SCR and flowing towards the backside of the device which creates a positive feedback with the I_{S2} component. Finally, at the end of the process, temperatures increase sharply and all components of leakage current rise quickly.

Experimental measurements, have shown that the main parameter influence on the critical energy value is the case temperature (T_C). Tests have been done

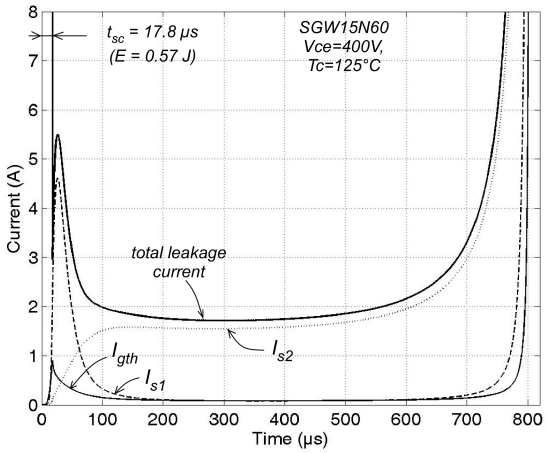

Fig. 8. Calculated evolutions of leakage current components during the short-circuit at the critical energy (E=0.57 J).

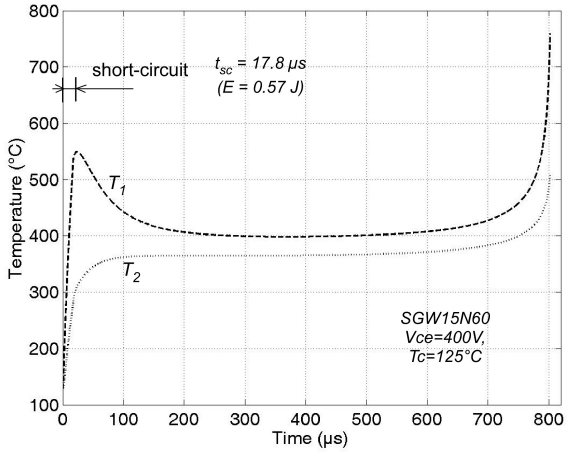

Fig. 9. Calculated evolutions of temperatures at the edges of SCR (T_1 at x_1 and T_2 at x_2 , see Fig.4) during the short-circuit at the critical energy.

for $T_C = 25^oC$ and 125^oC and the respective measured critical energy values were 0.82 J and 0.62 J, as shown in Fig.10. These measurements corroborates the simulated dependance of the case temperature on the critical energy which seems to be linear (Fig.10). The critical energy seems to be only the dissipated energy required to reach the threshold temperature which has been evaluated around 600^oC to 650^oC near the blocking junction. These results seems to show that the two failure modes, cumulative damage mode (for $E < E_C$) and delayed mode (see Fig.2), are in fact separated by this threshold temperature within the device rather than a critical energy. Further experimental tests have to be conducted in order to prove that this temperature threshold, which seems to be independent with the case temperature, is more largely independent from test conditions.

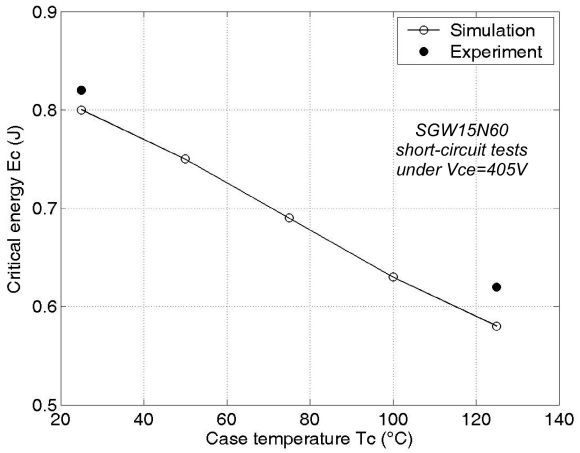

Fig. 10. Experimental and calculated dependence of the case temperature on the critical energy.

In addition, as shown in Fig.5b and discussed above, we can consider that the classical short-circuit failure mode (energy limited) is a limit case of the delayed failure mode with zero delay time to failure. So, we can extend the detailed analysis and explanations made in the delayed mode to the energy limited case and give better understanding of the failure process of this last failure mode.

4 Conclusion

[h] This paper has focused on the delayed failure mode, which is observed on IGBT transistors, after a successful but high energy short circuit turn-off. Presented devices are 600V NPT IGBTs in single chip TO247 packages. All the tested devices have shown the same behavior regarding their robustness against repetitive short-circuit tests. A critical value of short-circuit energy (E_C) has been found which separates two distinct failure modes. When the short-circuit energy is higher but close to E_C, devices fail at the first short-circuit test in a "delayed failure mode". A tail current takes place after the turn-off process of the device and leads to a destructive thermal runaway phenomenon after several hundreds of microseconds. The significance of this critical energy value (E_C) is related to the reach of high enough temperature values (about 650^oC) inside the device leading to a significant leakage current. It has been found that the leakage current is dominated by diffusion component and especially by hole saturation current.

In the realized works we have investigated the delayed failure mode for short-circuit energies greater or equal to the critical energy for NPT devices. Nevertheless, 2D physical modelisations and simulations of the thermo-electric

behavior must be performed in order to refine and complete the comprehension of the mechanisms which occur.

The work which remains to be done concerns the energies lower than E_C with a cumulative degradation and an ageing effect due to the repetitive short-circuit stresses. For this failure mode, several questions are still in abeyance. First, the ageing mechanism which leads to the failure must be identified. In a second step, we have to explore very low energies area. In addition, further investigations must be done in order to explain the different failure modes and mechanisms for PT IGBTs in comparison with NPT devices.

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