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Reduced temperature dependence of hot carrier degradation in deuterated nMOSFETs

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Abstract

Deuterated oxides exhibit prolonged hot carrier lifetimes at room temperature. We report evidence that this improved hot carrier hardness exists over the temperature range between -25 °C and 200 °C. However, the benefit of deuterium incorporation deceases with increasing stress temperature. Furthermore the V_T -shift shows a remarkable absence of temperature dependence for the deuterated samples. The results are compared to the existing vibration-relaxation model.

1. Introduction

Passivation of the Si/SiO_2 interface by deuterium (D) has been shown to increase the hot carrier lifetime of MOS transistors compared to the traditional hydrogen passivation [1,2,3,4]. So far published data on this effect are limited to degradation experiments at room temperature. We show the impact of D-passivation on the hot carrier induced parameter shifts over the temperature range between -25 and 200 °C and discuss the results in terms of the current understanding of degradation of deuterated interfaces.

2. Experimental

HC degradation was studied on nMOS transistors with L = 0.20 μm and W = 10 μm fabricated in an 0.18 μm CMOS process with a gate oxide thickness of 7 nm (the embedded-FLASH tunnel oxide). The final step in the fabrication process was a 30 minute post metal anneal at 450 °C in either in a H_2/N_2 or a D_2/N_2 mixture to passivate the dangling bonds at the Si/SiO_2 interface. The devices were stressed at V_{ds} = 3.75 V and V_{gs} = 2.05 V corresponding within 150 mV to peak substrate current (I_{sub}) conditions over the entire temperature range studied. The stress temperature was varied between -25 and 200 °C. Additional tests were performed at lower stress conditions, still at maximum I_{sub}, at room temperature and 125 °C.

Each bias condition was applied to 5 devices and the average value is presented in this paper. All I_{ds}-V_{gs} curves were measured in reverse mode, i.e. with the source and drain interchanged, since the hot-carrier damage is mainly located on the drain side. In this way the degraded region forms a part of the controlled channel and the device degradation can be more clearly observed [5,6]. For linear device characteristics V_{ds} = 10 mV was applied. V_T extraction was done using the maximum transconductance (g_m) criterion, using a constant current criterion gives comparable results. Prior to the hot carrier stress, the transistors annealed in H_2 or D_2 ambient (to be called H/D devices) were electrically indistinguishable over the entire temperature range [7], also with respect to the substrate current. For very small transistors it has been reported that there is a so-called cross-over point from negative to positive temperature dependence of the substrate current [8]. For the drain

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voltages used in this study this cross-over is at V_{gs} ~ 0.6 V, or when looking at the maximum substrate current condition at V_{ds} ~ 2.1 V. So the applied stress bias is far away from the substrate current cross over so for all applied bias conditions a negative temperature dependence is observed (reduction in I_{sub} for increasing temperature).

Charge pumping measurements at 500 kHz with 4 V voltage amplitude, a 1 μs pulse width and 100 ns rise time were used to study interface state generation.

All device characterizations were performed at room temperature to allow a fair comparison of stress results at different temperatures.

3. Results

Figure 1 shows the initial linear I_{ds}-V_{gs} characteristics, as well as those after 1000 s stress at substrate temperatures between -25 and +200 °C. The initial H and D characteristics are within the device-to-device variation on one wafer. The larger degradation for H-passivated samples reported in literature [1,7] can be clearly observed at room temperature. Figure 1 shows the expected stronger degradation at lower temperature for the traditional H devices. On the other hand the D samples show a remarkable lack of temperature dependence. Figure 2 depicts the temperature dependence of the degradation of the maximum transconductance (g_m), the saturation drain current ($I_{d,sat}$), the subthreshold swing (S) and the threshold voltage (V_T) after 1000 s

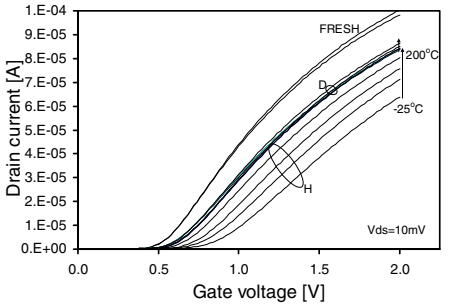

Fig. 1. Linear drain current before and after 1000 s stress V_{ds} = 3.75 V, V_{gs} = 2.05 V at various stress temperatures. Characterization was done at room temperature.

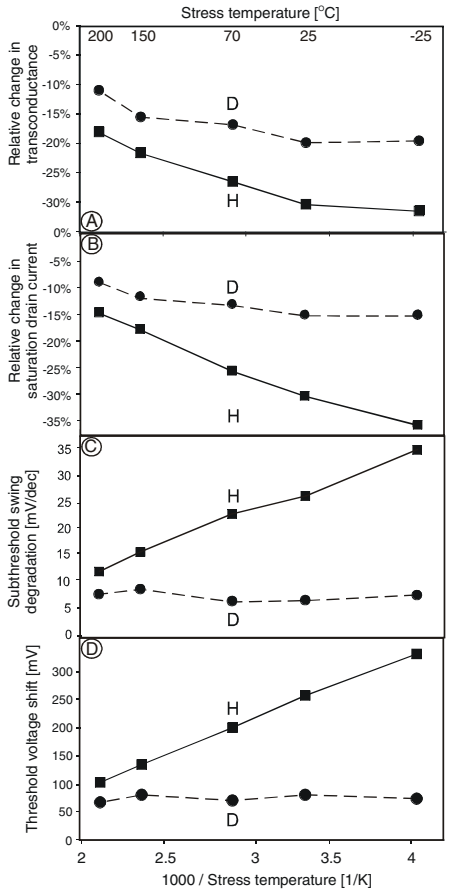

Fig. 2. Parameter degradation after 1000 s stress at various temperatures, V_{ds} = 3.75 V, V_{gs} = 2.05 V. Characterization was done at room temperature. a) maximum transconductance, b) saturation drain current, c) subthreshold swing, d) threshold voltage

stress. The D-samples show a reduced temperature dependence of the degradation in g_m and $I_{d,sat}$, compared to the H-devices. More interestingly is the almost negligible temperature dependence of the V_T-shift and the subtreshold swing for D-samples. These results imply that although the isotope effect can be observed over the entire temperature range studied, the advantage of D incorporation rapidly decreases with increasing operating temperature. The data of figure 2 was taken using only a 1000 s stress at the stress temperature and not measuring the time evolutions (in view of the measurement time related to the ramp back to room temperature for the device characterization). Since especially the H samples

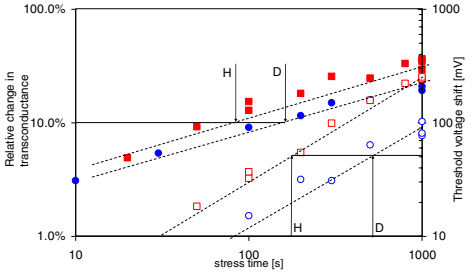

Fig. 3: Degradation the relative transconductance and threshold voltage at room temperature, V_{ds} = 3.75 V. The dotted lines are guides to the eye. The arrows give a schematic indication of the lifetime extrapolation using 10% g_m degradation and 50 mV V_T shift.

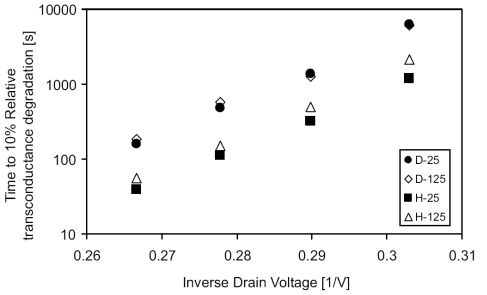

Fig. 4. Time needed for a 10% g_m degradation for stress conditions V_{ds} = 3.30, 3.45, 3.60 and 3.75 V at 25 °C and 125 °C. V_{gs} was corresponding to maximum I_{sub} conditions.

suffer from a significantly larger degradation than the typical end-of-life criteria (ΔV_T = 50 mV or 10% change in g_m or $I_{d,sat}$) it is important to consider the time evolution of the degradation as well. Figure 3 shows the degradation of the maximum transconductance and the threshold voltage at room temperature as a function of time. The degradation of the parameters with time t can de expressed as:

$$\Delta PAR \sim a.\ t^m \qquad (1)$$

As can be seen from figure 3 the exponent m is considerably different for the various degradation monitors. Hence depending on the lifetime criterion the critical parameter might be different. The variation in the exponent m for the H and D samples and for all applied bias conditions is equal within the device-to device variation (m = 0.4 for g_m and m = 0.7 for V_T). Within the experimental accuracy m is equal for T = 25 °C and T = 125 °C.

Please note that when estimating the isotope effect from data like plotted in figure 1 you observe a reduced degradation for deuterium passivated devices (2 times for g_m and 3 times for V_T, at room temperature after 1000 seconds) whereas looking at it from the time evolution point of view replacing hydrogen by deuterium retards degradation (3 times for g_m and 4 times for V_T). When comparing the degradation under different stress conditions or between several authors this difference should be kept in mind especially when the slopes of the degradation are different for the various degradation monitors.

In figure 4 we have plotted the time to 10% transconductance degradation at 25 °C and 125 °C for four stress voltages (all at peak I_{sub} conditions). The reduced temperature dependence of the degradation for the D samples is confirmed for lower stress voltages indicating that the projected lifetime of deuterium passivated transistors will be less sensitive to the operating temperature than that of the hydrogenated samples. The comparable degradation slopes illustrate that the phenomena found at elevated stress conditions will be similarly occurring at normal operating conditions.

3.1 Control experiments

We have performed several checks to investigate the validity of our measurements.

Bias temperature instability

At higher temperatures bias temperature instabilities (BTI) could play a role in our results. For both sets of samples we assessed the amount of BTI by stressing several devices at V_{gs} = 2.05 V and the source and drain grounded. In view of the recovery effects associated with BTI [9] ,for these experiments the devices were measured at the bias temperature. A 1000 s stress at 200 °C gives less than 1% degradation in g_m and a maximum V_T shift of 13 mV, showing that BTI is a relatively insignificant degradation mechanism at our stress conditions.

Process variation

Previous experiments at room temperature have shown that the incorporation of deuterium in an earlier stage in the process, for example in the gate oxide formation step, does not significantly improve the HC hardness [7]. This conclusion is confirmed over the entire temperature range.

Gate length

We have studied the temperature dependence of the hot carrier degradation for two different gate lengths (0.20 and 0.25 μm). The longer devices were stressed at V_{ds} = 4.0 V and V_{gs} = 2.1 V (also peak I_{sub} condition). The stronger temperature dependence for H samples is confirmed for this gate length. It should the noted that the V_T-shift for one of the D-passivated sets with L = 0.25 μm shows a slight increase with increasing bias temperature and for other sets a slight decrease. In both cases the temperature dependence for the H samples shows the expected behavior, comparable to the results in figure 2.

Charge pump measurements

Charge pump (CP) measurements were performed to quantify the interface state densities after periods of stress at 25 and 150 °C. Under peak I_{sub} stress conditions, interface state generation is the dominant degradation mechanism [10].

Deuterium passivation delays the creation of interface states so it will take a longer time to create the same amount of states. If interface state creation is the dominant factor in the degradation, plotting the increase in D_{it} versus the corresponding V_T-shift should give the same trend. Since charge trapping is not sensitive to the isotope effect in the longer time to reach a certain V_T-shift for the D samples more charge will be trapped [11]. So when a considerable fraction of the degradation is caused by charge trapping a smaller or larger slope can be seen in the correlation plot, depending on whether holes or electrons are the trapped species. The increase in D_{it} can be directly correlated to the increase in charge pump current (I_{CP}). Figure 5 shows the V_T-shift and the corresponding change in I_{CP} at room temperature and 150 °C. The correlation indicates that interface state generation is the dominant degradation mechanism for both wafers at 25 and 150 °C.

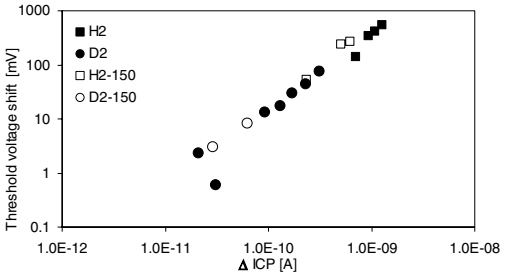

Fig. 5. Threshold voltage shift as a function of the change in charge pumping current at 25 and 150 °C.

Stress at high V_{gs}

For deep submicron MOSFETs it has been reported that biasing at peak I_{sub} conditions does not give the worst hot carrier degradation [12]. Instead biasing at $V_{gs} = V_{ds}$ creates more interface traps. This paper also reports enhanced degradation at elevated temperature, attributed to the location of the damage (more inside the channel at room elevated temperature, more under the drain for room temperature). Preliminary experiments on our devices indicates that stressing at $V_{gs} = V_{ds}$ = 3.75 V causes hot carrier degradation of comparable magnitude to peak I_{sub} condition. Also for this stress condition a large isotope effect is observed confirming interface state generation as dominant mechanism. Further temperature studies are needed before firm conclusions can be drawn.

4. Discussion

The negative activation energy for hot electron degradation as reported earlier [13] is confirmed for the hydrogenated wafers. At room temperature the deuterated samples are more robust against channel hot electron degradation due to the slower decomposition of the Si-D bonds compared to the Si-H bonds. The trend continues at elevated temperature, but does become less pronounced. The generation of interface states is due to HC stimulated hydrogen desorption. The dissociation of the Si-H bonds has been proposed to proceed via multiple-vibrational excitations by tunneling electrons. The improved HC hardness of deuterated MOS transistors is generally attributed to the better coupling of the Si-D vibrations to the Si phonon spectrum, [1,14] allowing faster relaxation of excited states, as shown by molecular dynamics (MD) simulations [15] and experiments [16]. This faster relaxation implies that less energy can pile up in the bonds making it more difficult to break the Si-D bond.

With increasing wafer temperature, the phonon spectrum will change while the Si-D and Si-H vibrations remain at the same energy. Given the complex structure of the phonon spectra, the temperature dependence of the isotope effect is not obvious. MD simulations predict slower relaxation of excited Si-H bonds than Si-D bonds even at much elevated temperatures [17]. Van de Walle predicted an increased HC isotope effect at lower than RT [18], based on the observed decrease in coupling of the Si-H bond to the bulk Si modes at lower temperatures

[19] and the absence of temperature dependence for Si-D bonds [16]. Our experimental data indeed show reduced temperature dependence for deuterated samples and hence fits qualitatively into the existing theory for the isotope effect in HC degradation. The remarkable lack of temperature dependence of the V_T-shift and subtreshold slope degradation for the D samples suggests that perhaps two competing degradation mechanisms might play a role. The larger slope m in the time evolution of V_T is also an indication that the degradation is not caused by pure channel hot carrier degradation only. We have performed a limited number of very long degradation experiments at room temperature. The slope m for the V_T degradation seems to be decreasing in time toward the same value as the slope of the transconductance degradation. This could imply that initially a second degradation mechanism plays a role that only affects the threshold voltage. For the bias conditions applied in this study the different slope for the time evolution in V_T and S exists until all parameters have exceeded the lifetime of the transistor but this effect needs to be studied more when extrapolating the lifetime to operating conditions.

Charge trapping has a different temperature dependency than interface state generation. Further charge pump studies over the entire temperature range will give more insight.

5. Conclusion

We have shown a reduced temperature dependence of hot electron degradation in nMOS transistors with a deuterium passivated Si-SiO_2 interface compared to hydrogen passivated transistors. The parameters g_m and I_{dsat} show a consistently lower shift when the devices are D-passivated and the V_T-shift and subtreshold slope degradation are not sensitive to the stress temperature. The observations are consistent with the existing explanation of the isotope effect however further studies are ongoing to investigate possible charge trapping contributions. The results presented in this paper imply that the isotope effect is present over the full temperature range of practical interest. The importance of D-processing to improve HC hardness decreases with increasing operating temperature. Degradation of deuterated nMOSFETs is shown to be only weakly dependent on temperature. Accurate prediction of the hot carrier lifetime then relies less on the precise knowledge of the operating temperature inside integrated circuits.

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