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***Abstract* – This work presents a comparative soft error evaluation of logic gates in bulk FinFET technology from 65- down to 32-nm technology generations. Single Event Transients induced by radiations are modeled with the MUSCA SEP3 tool, which explicitly accounts for the layout and the electrical properties of transistors. Good agreement between the calculated transient current, and TCAD mixed-mode simulations is demonstrated. This work allows for estimating the SER of such logic gates for ground applications, as well as for understanding the impact of voltage and drive strength through analysis of the sensitivity to soft errors.**

***Index Terms* – Soft error, bulk FinFET, MUSCA SEP3, VLSI design, supply voltage, soft error sensitivity.**

1. Introduction

In the last decade, the aggressive scaling of CMOS technology has posed formidable challenges in terms of electrostatic control of the channel, which is needed to sustain performance improvements and mitigate short-channel effects in down-scaled technology generations; leakage suppression and reduction of sub-threshold slope, as needed to maintain the standby power within reasonable limits; random variations, which need to be kept within reasonable bounds to avoid excessive yield degradation and sustain energy/performance improvements [1]-[7].

FinFETs/multi-gate devices have been introduced in industrial manufacturing processes, among the available options of devices that can address the above challenges and maintain compatibility with CMOS process. As main benefits, FinFETs exhibit smaller process variations, higher current drive per unit width and lower leakage current, compared to the bulk counterpart [1]-[7].

Operation at finer technologies tends to degrade robustness in many respects [8], as the technology scaling below 65 nm has introduced new issues, such as multi-collection and high Soft Error (SE) sensitivity induced by energetic particles coming from space and terrestrial radiations. Recent work showed that FinFET technology has attractive properties that limit the increase in the occurrence of soft errors [9], as its 3D configuration exposes small SE-sensitive areas.

From a design standpoint, the improvement of the reliability requires the accurate estimate of the SE susceptibility of FinFET standard cell libraries, in order to support the optimization of cells during the development of the library. This work presents a comparative Single Event Transient (SET) evaluation of logic gates for different layout styles in FinFET technology for different technologies. Because of lack of available experimental SE characterization of logic cells in FinFET technology, the simulation tool is an interesting alternative with the aim to anticipate the sensitivity trends. This evaluation is performed by the Monte-Carlo MUSCA SEP3 prediction platform [10]. In this work, a validation of the SET response evaluated by the predictive platform versus TCAD mixed-mode simulations is first presented, assuming in worst radiation location. TCAD mixed-mode simulations are here adopted as a reference to validate the accuracy of MUSCA SEP3 results. Analysis confirms that MUSCA SEP3 agrees very well with TCAD simulations as expected, while reducing the computational effort by several orders of magnitude compared to the latter (TCAD simulations would definitely be unfeasible for the exploration and the purpose of this work). The validation is performed for NOR and NAND logic gates in 65-nm bulk technology. Then, the analysis of the soft error susceptibility (sensitivity threshold, and SET characteristics) of NAND and NOR gates is presented for 65- down to 32-nm technology generations to provide a scaling perspective. Finally, the impact of the supply voltage and drive strength on the soft error sensitivity is studied for the above logic gates with the aim of deriving guidelines to reduce the soft error susceptibility.

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2. Device and layout description

The devices adopted in this work are based on basic structure of bulk FinFET technology, as presented in Fig. 1 [11], [12]. The physical dimensions of the structure have been summarized in Table 1. In this work, gate lengths L_{Fin} of 65 and 32 nm are considered.

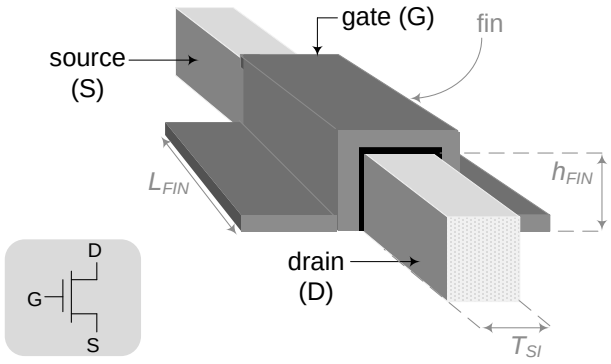


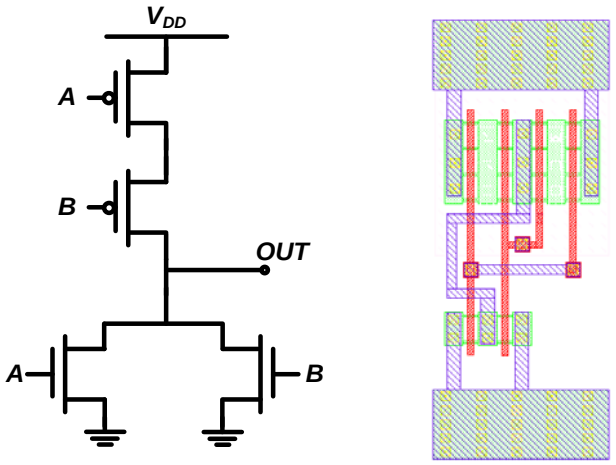
Fig. 1 Bulk FinFET transistor structure [12].

Table I. Summary of device and layout features [11]

FinFET Technology and Design Rules	Bulk Technology		
	65-nm	45-nm	32-nm
L_{Fin}	55 nm	45 nm	35 nm
T_{SI}	36 nm	30 nm	23 nm
h_{Fin}	72 nm	60 nm	46 nm
Fin pitch	170 nm	120 nm	80 nm
DR1 contact size	90 nm	60 nm	40 nm
DR2 min. metal gate spacing	90 nm	70 nm	54 nm

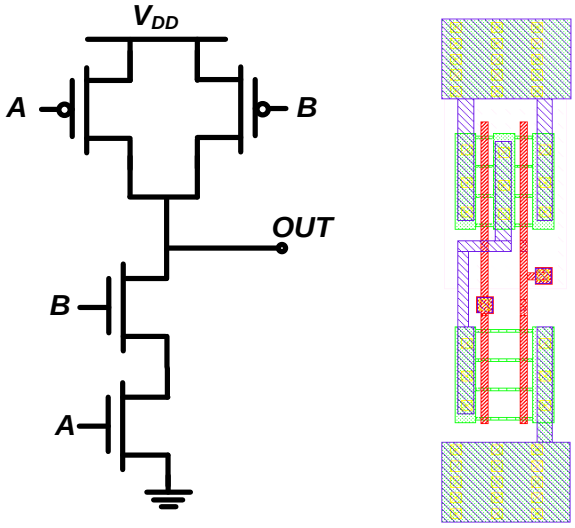
Figs. 2 and 3 show the layout view of NOR and NAND gates. The standard cell height H_{cell} is set to 14 tracks of M2 (metal 2) which correspond to 2.8 µm and for the 65-mn and 32-mn technology respectively. The ground and supply rails are 2.5-track tall, which correspond to 0.5 µm and 0.25 µm in 65 and 32 nm. According to Figs. 2b and 3b, the height H_p of the area where the p-MOS transistors are implemented is set to 1.5 times the height H_n of the area where the n-MOS transistors are implemented [12].

As a peculiar limitation of FinFETs, the freedom to choose the device drive strength is rather limited, especially for devices that are close to the minimum size. Indeed, the drive strength can only be improved by increasing the (discrete) number of fins. On the other hand, the drive strength is known to impact the SE sensitivity [13]. In this work different drive strengths are considered from 1X to 4X with the aim of investigate the impact of the soft error susceptibility of the selected logic gates.



(a) (b)

Fig. 2. a) Topology and b) layout of NOR2 gate in 32-nm Bulk FinFET technology



(a) (b)

Fig. 3. a) Topology and b) layout of NAND2 gate in 32-nm Bulk FinFET technology

3. Soft Error estimation in Bulk FinFET technology

3.1. Soft error prediction platform: MUSCA SEP3

The soft error estimation was performed through the MUSCA SEP3 tool, which was presented in previous papers [10][14] This tool is based on the modeling of the mechanisms that occur from the strike of a radiation particle into matter to the SE occurrence, as shown in Fig. 4. This tool can account for every kind of radiation particles: neutrons, protons, heavy ions, muons, and alpha particles. The 3D radial distribution of generated charges in the silicon is calculated for each incident particle [15] considering the back-End Of Line (BEOL) proposed by the ITRS roadmaps [1]. In this work, the soft errors induced by atmospheric neutrons are investigated.

The modeling of the charge diffusion accounts for the ambipolar diffusion mechanisms and recombination processes [16]. The modeling of the charge collection accounts for the dynamic transport and the multi-charge collection mechanisms (charge sharing, pulse quenching [10]), the bias voltage, the layout, the bipolar amplification, the shallow trench isolation (STI) and the fabrication process. The bipolar amplification model depends on two mechanisms. First, the model uses the equivalent access resistances of the tri-gate device to determine the triggering of the bipolar transistor. Second, the model takes into account the variability of the amplification of charge collection as a function of LET due to the Bulk FinFET technology. The charge collection of each transistor is calculated based on the Front-End-Of-the-Line (FEOL) information [12] extracted from the layout (in GDS format).

The modeled transient currents of each transistor (in this work, the whole circuitry) are injected at the circuit level and simulated with Spectre, taking into account the location of secondary ions compared to collection volumes [10]. The model cards of n-MOS and p-MOS FinFET transistors are derived from the predictive model cards provided by Arizona State University (ASU) [17].

3.2. Validation of SET responses by TCAD Mixed-Mode

Previous work [14] described in detail the capabilities of the prediction platform to model the charge collection induced by radiations in SOI FinFET transistors. In this work, the soft

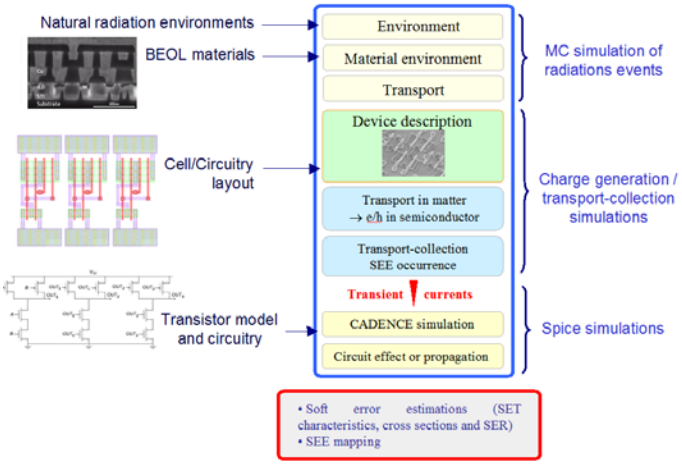


Fig. 4 Overview of the soft error prediction tool MUSCA SEP3 (applied to FinFET technology).

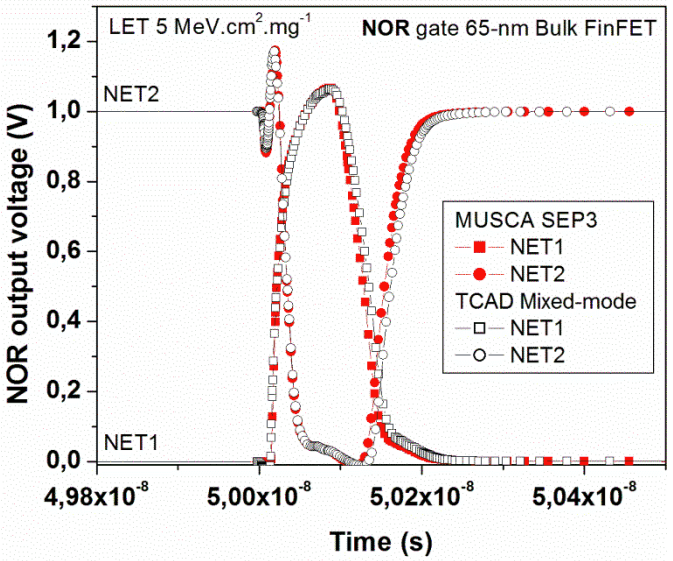


Fig. 5 Comparison of SET responses of 65-nm NOR cell evaluated through TCAD Mixed-Mode and MUSCA SEP3 for a secondary ion with a LET of 5MeV.cm^2.mg^{-1}. The figure shows excellent agreement of MUSCA SEP3 with TCAD Mixed-mode simulations.

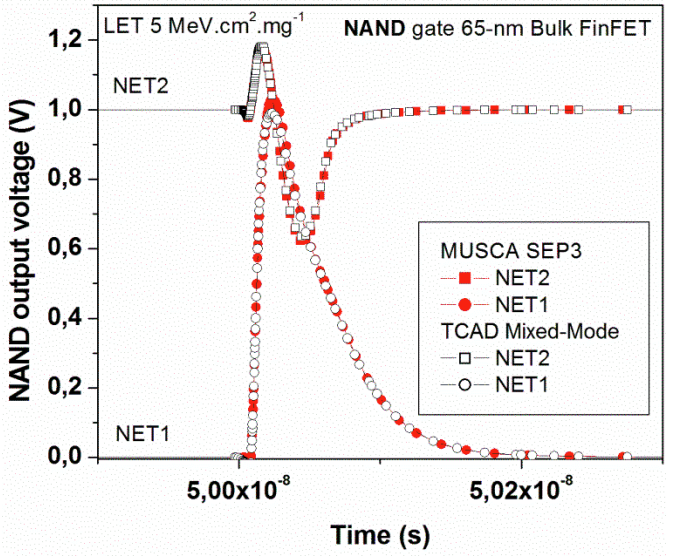


Fig. 6 Comparison of the transient responses of 65-nm NAND cell evaluated through TCAD Mixed-Mode and MUSCA SEP3 for a secondary ion with a LET of 5MeV.cm^2.mg^{-1}. The figure shows excellent agreement of MUSCA SEP3 with TCAD Mixed-mode simulations.

error sensitivity of NOR and NAND gates in bulk FinFET technology is investigated. In order to validate the charge collection modeling in logic gates, the transient response is simulated through TCAD mixed-mode simulation tool and MUSCA SEP3, for a ion with a LET (Linear Energy Transfer) of 5 MeV.cm^2.mg^{-1} as presented in Fig. 5 and Fig. 6 for the NOR and NAND gate in the worst case [13][14]. Low LET, i.e., less than 15 MeV.cm².mg^{-1}, has been considered in order to be representative of secondary ions induced by terrestrial neutrons or protons. Moreover, low LET limits the charge sharing effects, such as pulse quenching, at circuit level [18].

In order to perform these simulations, a chain of 10 NOR gates and 10 NAND gates are considered and simulated. The first gate is defined as the gate struck by the radiation particle while the whole logics chain is physically and electrically simulated [10]. NET1 and NET2 correspond to the outputs of the following two logic gates. In Fig. 5, which shows the transient at the occurrence of a SET, MUSCA SEP3 is shown to agree very well with the results of the TCAD mixed-mode simulations. Only a small difference divergence can be observed when the output voltage of NET1 and NET2 come back to their initial logic state, “0” and “1” respectively.

In Fig. 6, no SET is observed in MUSCA SEP3 and TCAD Mixed-Mode simulations. Actually, even if the output voltage of NET1 is modified, the SET amplitude and duration are both too small to induce the upset onto the NET2 output voltage. Once again, very good agreement is shown in this figure, with the exception of a small amplitude difference in NET1 when the output voltage of NET1 rises close to the supply voltage (1V).

3.3. Soft error evaluation of FinFET logic gates

Different parameters can be adopted as metrics to quantify the soft error sensitivity of logic gates. In this paper, the SET pulse width and the LET threshold are investigated. The LET threshold corresponds to the minimal quantity of charges induced by the radiation particle (due to the Coulomb interactions) that is necessary to induce a SET. In this work, only silicon secondary ions with a LETs under 15MeV.cm^2.mg^{-1} will be used in order to be representative of recoil ions induced by terrestrial neutrons.

Fig. 7 presents the LET threshold of NAND (in red) and NOR (blue) logic gates for technologies from 65-nm down to 32-nm bulk FinFET with a X2 drive strength. First, it is interesting to note that the NAND gates seem to be less sensitive than the NOR gates for both technologies. This sensitivity trend observed for the FinFET technology is in good agreement with previous work on conventional planar CMOS processes [19]. The NOR gate is 62% less sensitive than the NAND gate for the technologies. Another interesting fact is that the 32-nm technology has a lower LET threshold than the 65-nm node. Actually, the 65-nm technology is 38% less sensitive than the 32-nm technology. One reason for this is that the supply voltage of the 32-nm considered circuits is lower (i.e., 0.7V as compared to 1V for the 65-nm technology) [20]. More specifically, at lower voltages the probability to collect sufficient charge increases, hence SER is higher (this point is developed later in this work). In the rest of this work, results will be focus on the 32-nm and 65-nm technologies.

The soft error susceptibility of logic gates can also be analyzed by investigating the SET pulse width as a function of LET of secondary ions induced by atmospheric neutrons, as shown in Fig. 8. As expected, the SET pulse width increases with the LET of the secondary ions. The same sensitivity trend is observed for all LETs for the logic gates and the both technological node. It is interesting to note that the SET pulse width seems to saturate at higher LET.

Fig. 9 presents the SET cross sections of the NOR gate in 65-nm (black squares) and 32-nm (red circles) in bulk FinFET technology induced by atmospheric neutrons. The error bars represent the statistical error induced by the Monte-Carlo

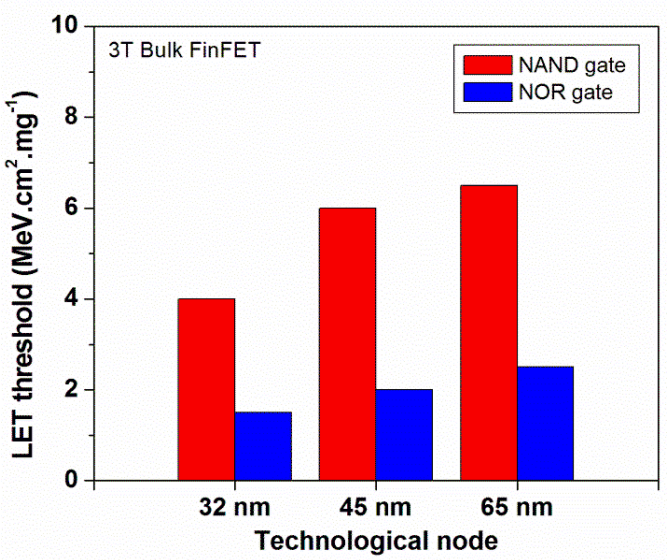


Fig. 7 LET threshold of SET occurrence for NAND and NOR gates in 32- and 65-nm bulk FinFET technology.

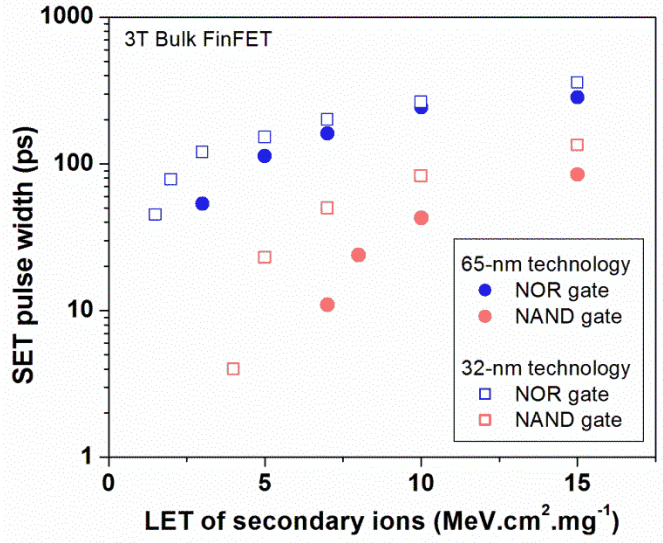


Fig. 8 Evolution of the SET pulse width as a function of the LET of secondary ions induced by neutrons in the NOR gate and NAND gate in 65-nm bulk FinFET.

simulation. The errors bars are defined as 1 divided by the square root of the number of SETs [10]. It is interesting to note that the 32-nm technology is less sensitive than the 65-nm node at high neutron energies. However, at low neutrons energy, an opposite sensitivity trend is observed. The crossing of SET cross sections requires the estimation of the Soft Error Rate (SER) at the ground level (atmospheric radiation environment). The SER is calculated by the convolution of the SE cross-section presented in Fig. 9 with the atmospheric neutron flux [21]. The calculated comic SER of 65-nm turns out to be 27% lower than the 32-nm node for the NOR gate in bulk FinFET technology. This estimation is in good correlation with the normalized soft error results presented in [20].

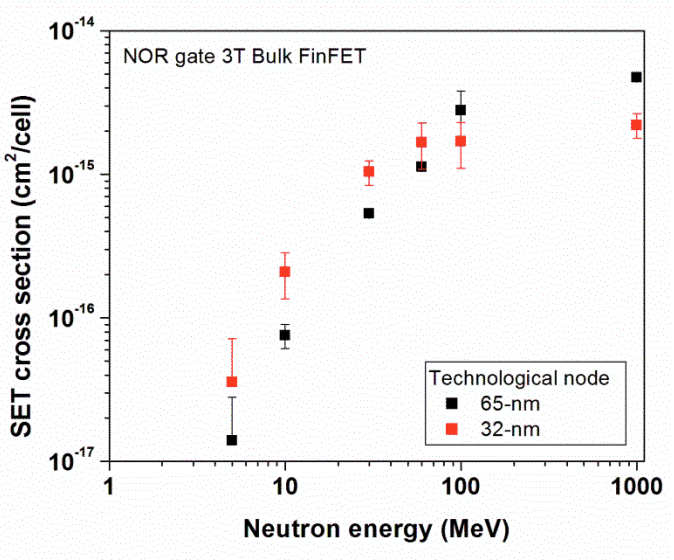


Fig. 9 SET cross sections of NOR gate in 65-nm (black squares) and 32-nm (red circles) in bulk FinFET technology induced by atmospheric neutrons.

4. Soft Error reduction in FinFET logic gates

4.1. Impact of the supply voltage on the susceptibility to soft errors

As discussed previously, the lower supply voltage is a critical parameter for the soft error sensitivity. Fig. 10 presents the impact of the supply voltage on the LET threshold of the NOR and NAND gate in 65-nm bulk FinFET technology. From this figure, the higher supply voltage in 65-nm technology (1V) reduces the SET susceptibility of both logic gates. In detail, the LET threshold is increased by 60% (38%) when increasing the supply voltage of the NOR (NAND) gate by 20%.

Fig. 11 shows the impact of the supply voltage on the maximal SET pulse width generated by atmospheric neutrons in NAND and NOR gates in 65-nm and 32-nm. This parameter

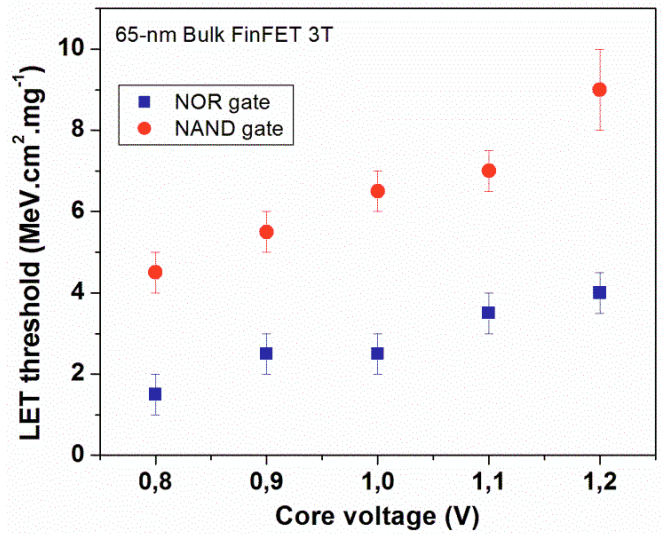


Fig. 10 Evolution of LET threshold as a function of the supply voltage of NOR and NAND gates in 65-nm bulk FinFET.

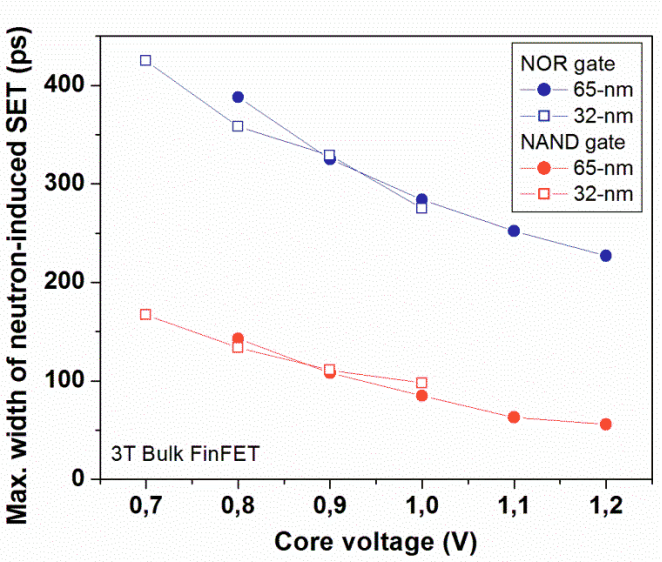


Fig. 11 Maximal width of neutron-induced SET versus supply voltage of NOR (colored symbols) and NAND gates (empty symbols) for the 65-nm (black squares) and 32-nm (red circles) bulk FinFET technology with a X2 drive strength.

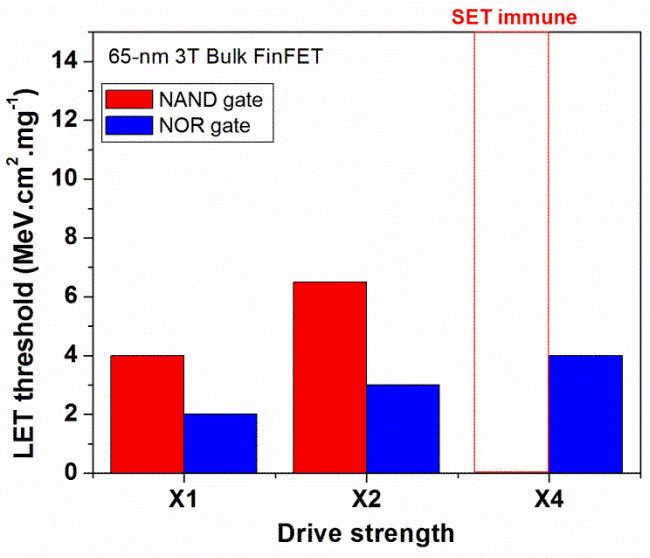


Fig. 12 Comparison of LET threshold of the SET occurrence of NAND and NOR gates for a range of drive strength from X1 to X4 in 65-nm 3T Bulk FinFET.

can be used as metrics to optimize the cell design and enhance the robustness of the cells against soft errors. In particular, the above metrics permits to relate the radiation constraint and the system specifications. The system frequency can induce temporal masking of SETs which reduces the soft error impact at system level [22]. Then, the designer of the system must use this metric parameter to find a compromise between performance and soft error robustness. For the 65-nm technology, the maximal SET pulse width can be reduced by 34% (20%) for the NAND (NOR) gate with a 20% increase in the supply voltage. For the 32-nm technology, the maximal SET pulse width can be reduced by 27% (23%) for the NAND (NOR) gate with a 25% increase in the supply voltage. This improvement in robustness against soft errors is obtained at approximately quadratic energy penalty, i.e. at the expense of a 40% (50%) energy increase in 65-nm (32-nm) technology.

4.2. Impact of the strength on the susceptibility to soft errors

The well-known mitigation technique is based on the increase of the drive current provided by the transistors p-MOS1 and p-MOS2 using a larger channel width. Fig. 12 shows the impact of the drive strength on the LET threshold of NAND (in red) and NOR (in blue) gate in 65-nm bulk FinFET technology for a range of drive strengths from X1 to X4. The SET sensitivity of both logic cells decreases with higher drive strength. This fact is in good agreement with previous results [13]. It is interesting to emphasize that X4 drive strength permits to make the NAND gate totally immune to SETs induced by atmospheric neutrons. Indeed, no SET is observed at any LET level of secondary ions induced by atmospheric neutrons. At the same time, the LET threshold of the NOR gate increases by 33% for the X4 drive strength. This enhancement in the robustness against soft errors is obtained at an approximately linear energy penalty, due to the increase of transistor parasitic capacitances.

Due to its higher soft error sensitivity, the dependence of the SET pulse width of the NOR gate on the LET of the ion is plotted in Fig. 13, assuming a 65-nm bulk technology, and drive strength ranging from X1 to X4. It is interesting to note that stronger transistors have reduced the SET pulse width, regardless of the LET of the secondary ions induced by atmospheric neutrons. At high LET, i.e., 15MeV.cm^2.mg^{-1}, the SET pulse width is reduced by 38% for the X4 drive strength. This trend is in good agreement with literature [13].

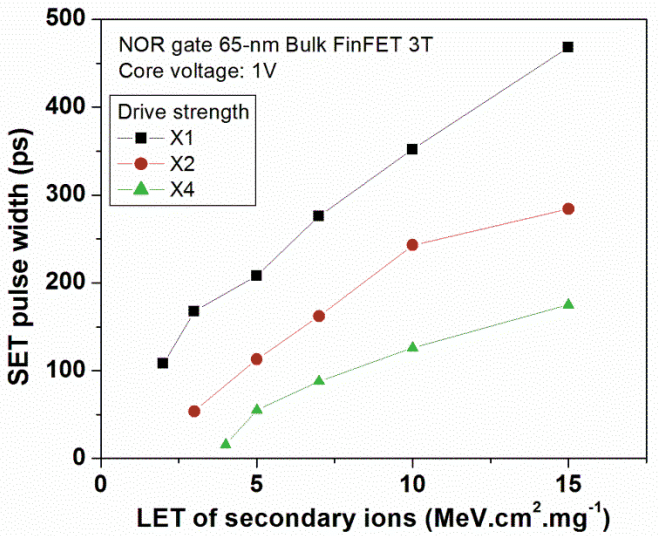


Fig. 13 Evolution of the SET pulse width as a function of LET induced in the NOR gate in 65-nm 3T Bulk FinFET for a range of drive strength from X1 to X4.

5. Conclusion

In this work, a comparative soft error evaluation of logic gates in bulk FinFET technology has been presented for a range of technologies from 65- to 32-nm. Because of lack of experimental SE characterization of logic cells in FinFET technology, the simulation tool is an interesting alternative

with the aim to anticipate the sensitivity trends. Single Event Transients induced by radiations are modeled by accounting for the layout and electrical properties of standard cells through the prediction tool MUSCA SEP3. Good agreement between the results obtained with this tool with TCAD mixed-mode simulation have been shown for NOR and NAND logic gates. This work allows for estimating the SER of such logic gates for ground applications. The estimated comic SER of 65-nm is 27% lower than the 32-nm node for the NOR gate in bulk FinFET technology.

This work studies and quantifies the benefits and the penalties brought by an increase in the supply voltage and the cell drive strength. Analysis shows that higher supply voltages can significantly reduce the SET susceptibility. As a representative example, the maximal SET pulse width is reduced by about 25% with a 25% increase in the supply voltage in 32-nm technology. This improvement in robustness against soft errors is obtained at the expense of a 40-50% energy increase. Accordingly, increasing the supply voltage can be effective, but leads to an energy penalty that is larger than the robustness benefit. Similarly, the transistor strength increase in a NOR gate can bring 40% improvement in the maximal SET pulse width for a 100% larger sizing for NOR, which entails the same dynamic/leakage energy increase. On the other hand, for a NAND gate, strengths of X4 or larger ensure completely SET free operation at ground level. Accordingly, for certain cells (e.g., NAND) the strength increase can be very effective, and hence preferable to voltage increase, thanks to its lower energy cost. For others (e.g., NOR), voltage increase improves SE robustness at lower energy cost, compared to strength increase. This motivates future investigations on energy-optimal hardening techniques that combine both SE-aware voltage scaling and sizing.

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