Investigation of the hot carrier degradation in power LDMOS transistors with customized thick oxide

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Abstract
In this paper, we report a combined experimental/simulation analysis of the degradation induced by hot carrier mechanisms, under ON-state stress, in silicon-based LDMOS transistors. In this regime, electrons can gain sufficient kinetic energy necessary to create interface states, hence inducing device degradation. In particular, the ON-resistance degradation in linear regime has been experimentally characterized by means of different stress conditions and temperatures. The hot-carrier stress regime has been fully reproduced in the frame of TCAD simulations by using physics-based models able to provide the degradation kinetics. A thorough investigation of the spatial interface trap distribution and its gate-bias and temperature dependences has been carried out achieving a quantitative understanding of the degradation effects in the device.

Keywords: Hot-carrier degradation, Interface trap, ON-state stress, LDMOS transistor, Modelling, Reliability

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1. Introduction

Nowadays, the lateral double-diffused MOS (LDMOS) power transistor represents the device of choice for smart power technologies because of its compatibility with CMOS technology [1, 2]. However, because of the complex lateral structure, the high fields at the silicon/oxide interface intensify the degradation mechanisms affecting the device reliability. In particular, when the device operates in ON-state regime, electrons can gain sufficient kinetic energy (hot carriers) necessary to create interface states followed by charge trapping causing the reduction of the device performance [3].

Being one of the most critical issues affecting the LDMOS reliability [3], various predictive models have been recently developed based on analytical relationships or suitable for TCAD investigations [4-6]. In [7], by taking into account the interaction of the hot carriers with interface molecules and the thermal-field interaction with the lattice, the hot carrier degradation has been predicted for an extended range of stress conditions and device geometries by using a TCAD tool. However, the LDMOS devices investigated in the previous works are mainly focused on architectures with a shallow-trench isolation (STI) since they are known to lead significant benefits in reducing chip size even if worsening R_{ON} degradation during reliability tests because of the high electric field occurring at the STI edges [8- 10].

In this paper, a hot carrier degradation analysis has been performed on medium rated voltage N-drift LDMOS transistors with customized thick oxide aimed at optimizing the SOA limitations coming from the STI architecture [11]. In particular, the ON-resistance degradation in linear regime has been experimentally investigated for an extended range of stress conditions and finely reproduced by means of TCAD simulations. Consequently, the spatial interface trap distribution has been evaluated and its gate bias dependence has been investigated.

2. Device Structure, Experimental Setup and TCAD Calibration

Medium rated voltage N-drift LDMOS transistors, fabricated on 200mm-wafers by STMicroelectronics [11], are considered and shown in Fig. 1.

The devices under investigation feature a gate width of 20 µm, a gate oxide thickness of 12 nm, and a customized thick oxide in the N-drift region, aimed at optimizing the SOA limitations of STI architecture [11], ranging between 200 nm and 400 nm.

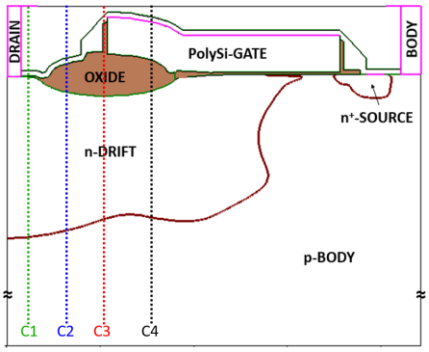

Fig. 1. Schematic of the medium rated voltage N-drif LDMOS with customized thick oxide realized on 200-mm silicon wafer by STMicroelectronics. It is wort noting that the source contact is on top of the n^+-SOURCE region. Cuts C1, C2, C3 and C4 represent the sections where interface (oxide/N-drift) trapped charge is monitored.

In order to investigate the device degradation due to hot carrier stress (HCS) and to spatially localize the interface trapped charge, experimental analyses combined with TCAD simulations have been performed.

The device degradation has been experimentally carried out on-wafer by adopting the conventional measure/stress/measure technique. Consequently, HCS induced degradation is evaluated by monitoring the R_{ON} shift in linear regime.

Finally, the simulated structure has been defined and calibrated in the frame of the Sentaurus TCAD simulator [12] considering the geometric characteristics and the material properties of the devices under test (DUT). In particular, process simulations have been used to define the doping profiles, the gate work-function has been tuned in order to attain same threshold voltage of the experimental device and a fine tuning of the low-field mobility dependence on the normal electric field (Enhanced Lombardi model [12]) has been carried out in order to obtain the good agreement between experimental and simulated I_DV_G transfer characteristics as shown in Fig. 2.

Moreover, in order to correctly reproduce the HCS conditions in ON-state, the heat transfer equation has been used and thermal resistances have been included at the contacts and calibrated against measured output characteristics in order to reproduce the self-heating effects in the device. Then, the VanOverstraeten impact-ionization model has been turned on with default parameter values allowing for an accurate prediction of the avalanche onset regime

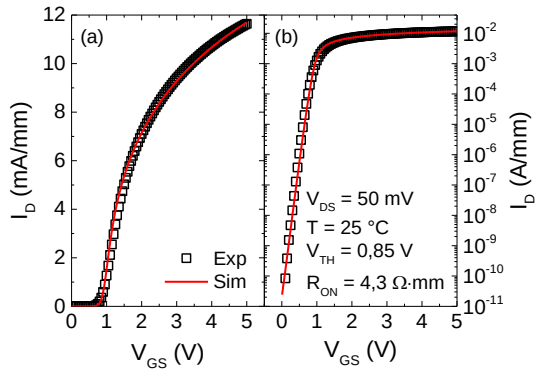

Fig. 2. Experimental (symbols) and simulated (line) I_DV_G transfer characteristics in linear (a) and semi-logarithmic (b) scale.

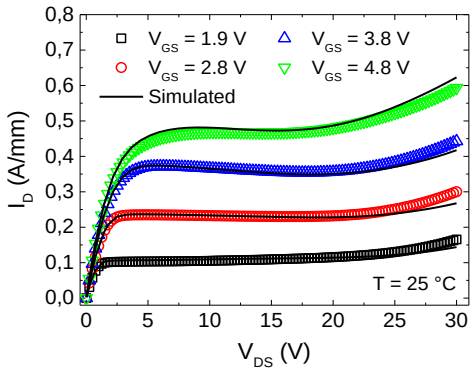

Fig. 3. Experimental (symbols) and simulated (line) I_DV_D characteristics as a function of the gate bias.

at larger V_{DS} (Fig.3). It is worth noting that, since for the adopted accelerated stress conditions the DUTs do not lead to very high temperature and electric field values, VanOverstraeten model is adequate and has been used instead of more recent ones such as UniBo impact-ionization model [13, 14], which typically differs at larger temperatures and fields.

3. Review of Hot-Carrier Stress (HCS) Degradation Model

HCS degradation model [7, 12] aimed at modelling the ON-resistance degradation occurring in n-channel LDMOS is adopted to numerically predict the effects of a high drain voltage applied during ON-state operation.

Different competing mechanisms such as single-particle (SP), multiple-particle (MP) and field-enhanced thermal interaction (TH) contribute to the de-passivation of the electrically inactive Si-H bonds at the silicon/oxide interface. The above mechanisms need to be accounted for to capture the physical description of the interface trap generation in different operating regimes [7, 15- 18].

SP-process is related to a single high energetic particle which can induce a bond-breakage event in a single collision.

MP-process is triggered by a series of colder carriers which subsequently impinge the interface causing the bond breaking [18].

TH-process is induced by thermal interactions with the lattice. In particular, due to high lattice temperature, phonons can excite the silicon interface molecules and eventually break them.

The SP-process is usually the dominant degradation mechanism in transistors stressed at high-drain low-gate voltages, whereas the MP-process is typically more evident in scaled MOSFET architectures stressed at lower drain voltages but larger gate biases [18]. Finally, the TH process is strongly dependent on the lattice temperature and thus becomes crucial in high power devices where the current rating induces relevant self-heating effects. Therefore, by considering that the devices under test are medium-rated N-drift LDMOS transistors with limited self-heating effects and the HCS degradation analysis mainly focused on the high-drain low-gate stress condition, the SP-process turns out to be the dominant degradation source, which is expected to give an interface-trap peak generation close to the source-side field-oxide edge. Consequently, the interface trap density generated during hot-carrier stress as a function of time and activation energy is given by [7]:

$$N_{it,SP}(r,t,E_{SP}) = P_{SP}\, N_0 \left[1 - e^{-k_{SP}(r,E_{SP})t}\right] \quad (1)$$

where P_{SP}, N_0, E_{SP} and k_{SP} (r, E_{SP}) are the probability for defect generation, the maximum number of interface bonds, the activation energy and the reaction rate for the SP process, respectively. This latter is given by the scattering-rate integral:

$$k_{SP}(r,E_{SP}) = \int_{E_{SP}}^{\infty} f(r,E)g(E)v(E)\sigma_{SP}(E)dE \quad (2)$$

where f(r, E), g(E) and v(E) are the carrier distribution function, calculated by solving the Boltzmann equation in the framework of the spherical harmonics expansion (SHE) method incorporated in the Synopsys tool, the total density of states and the carrier velocity, respectively.

Finally, σ_{SP} is the single-particle reaction cross-section given by:

$$\sigma_{SP}(E) = \sigma_{SP0}\left(\frac{E-E_{SP}}{k_B T}\right)^{p_{SP}} \quad (3)$$

where p_{SP} is an exponent characterizing the SP-process and σ_{SP0} is a fitting parameter. The scattering rate models were further modified in order to take into account the finite distribution of the activation energies for the Si/SiO2 bonds in a disorder medium like the amorphous SiO2 (bond-dispersion model [7]).

4. Results and Discussion

In order to understand which are the worst HCS conditions, the body current has been monitored because of its correlation with the impact ionization generation and hence with the number of carriers gaining enough energy to eventually generate interface traps. Fig. 4 shows the simulated body current (a) with the corresponding impact ionization generation term (b). The higher the impact ionization peak the higher the absolute body current. Moreover, the body-current characteristics reveal a strong increase of impact ionization with a first peak at V_{GS} about 1.9 V, which is usually adopted as a worst-case condition for the HCS investigations. This initial rise
is attributed to the steep increase of the channel current in the near-threshold regime, with carriers experiencing a region of high electric field close to the channel. By increasing the gate bias the impact ionization peak moves toward the drain (Figs. 4b and

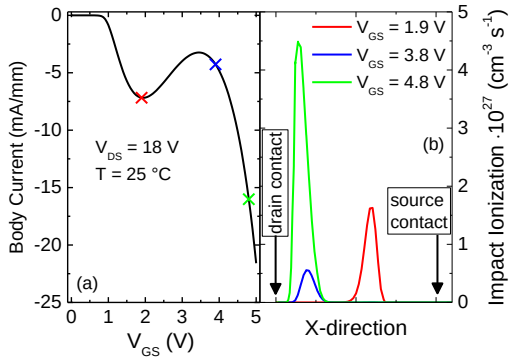

Fig. 4. Simulated body current (a) with the corresponding impact ionization generation term (b) occurring in the drift region at selected gate voltages. By increasing V_{GS} the impact ionization peak moves toward the drain (b). No x-axis is shown in (b) because of the information confidentiality.

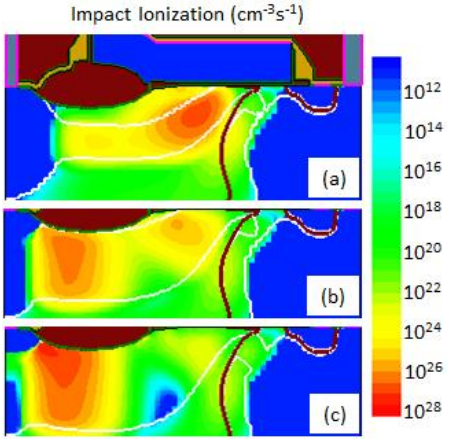

Fig. 5. Simulated impact ionization generation term at V_{GS} = 1.9 V (a), 3.8 V (b) and 4.8 V (c) with V_{DS} = 18 V and T = 25 °C. By increasing V_{GS} the impact ionization peak moves toward the drain.

5) and the body current rises again to larger values due to the Kirk effect at the drain edge.

It is worth noting that it was not possible to experimentally monitor the body current because body and source contacts are internally short-circuited in the real devices.

By considering the simulated body current in Fig. 4a, three different stress conditions have been chosen to verify the correlation between impact ionization (hot carrier) and device HCS degradation. In Fig. 6, the ON-resistance degradation extracted in linear regime for the three selected stress conditions is reported, showing a good correlation with the simulated body current (Fig. 4a).

In general, the large electric fields causing HCS damage are strongly localized in well-defined regions as shown by Figs. 4b and 5. In order to simulate the R_{ON} degradation, the HCS degradation model proposed in [7] has been adopted along with numerical solution of the Boltzmann transport equation implemented in [12]. However, since the HCS model was previously used for STI-LDMOS transistors, a first calibration procedure has been carried out on the structure under analysis. To this purpose, since for stress conditions at low V_{GS} the major role is played by the single-electron hot-carrier processes, the corresponding model has been incorporated first and calibrated according to ΔR_{ON} degradation experiments mainly referring to its magnitude and slope. More specifically, the maximum number of interface bonds (N_0), the fitting constant (σ_{SP0}) in the reaction cross-section and the probability for defects generation (P_{SP}) have been

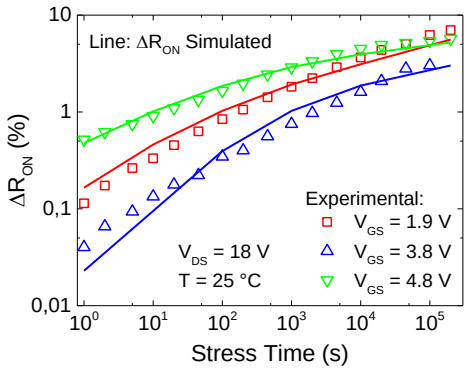

Fig. 6. Experimental (symbols) and simulated (line) R_{ON} degradation as a function of different stress conditions.

slightly tuned against experiments. The HCS model has been finally applied for different gate biases, providing an accurate agreement with experiments (Fig. 6) confirming that the single-electron HCS process is the most relevant one for this kind of devices. No relevant threshold voltage shift has been experimentally observed in stressed devices as shown in Fig. 7, thus indicating no degradation localized in the channel region and hence the negligible or absent field-enhanced thermal contribution also at large gate biases. Moreover, the maximum temperature due to self-heating has been monitored showing values below the threshold of the thermal degradation.

Fig. 8 shows the interface trap creation during the stress in the case of V_{GS} = 1.9 V (a) and V_{GS} = 4.8 V (b) with V_{DS} = 18 V and T = 25 °C. It is possible to note that: i) a huge and fast (lower than 100 ms) interface trap creation occurs close to drain

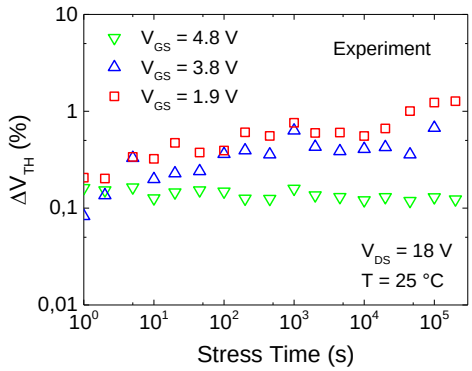

Fig. 7. Experimental V_{TH} degradation as a function of the gate stress conditions.

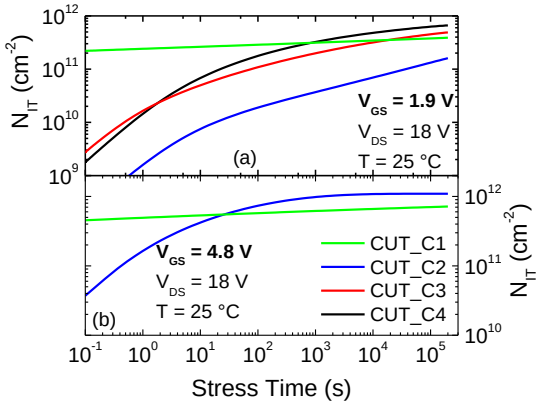

Fig. 8. Interface trap concentration versus the stress time in correspondence to the cuts shown in Fig.1 (C1 is the closest cut to the drain side) for the stress conditions V_{GS} = 1.9 V (a) and V_{GS} = 4.8 V (b) at V_{DS} = 18 V and T = 25 °C.

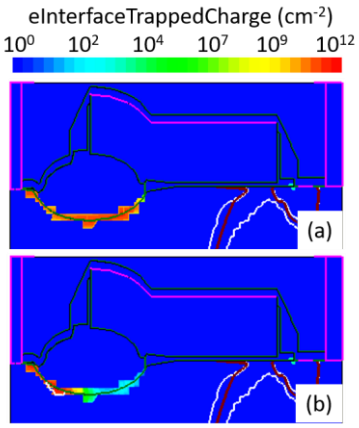

Fig. 9. Interface trapped charge after 20000 s of stress at V_{GS} = 1.9 V (a) and V_{GS} = 4.8 V (b) with V_{DS} = 18 V and T = 25 °C.

contact (cut C1, Fig. 1) independently of the applied gate bias. It is worth noting that at the stress time t = 0 s (fresh device) no trapped charge was considered at the Si/SiO2 interface. However, since the region below/around the drain contact is highly doped (not shown) in order to reduce the contact resistance, R_{ON} is insensitive to interface charge trapped in this region; ii) by observing cuts C3 and C4, the interface traps responsible for the R_{ON} degradation at low V_{GS} are created in the region of the thick oxide (selective LOCOS); iii) by increasing the gate bias (V_{GS} = 4.8 V) the trap creation moves toward the drain contact (cut C2, Fig 8b). This is well appreciable in Fig. 9 where the interface trapped charge is shown after

$2 \cdot 10^5$ s of stress at V_{GS} = 1.9 V (a) and V_{GS} = 4.8 V (b), V_{DS} = 18 V and T = 25 °C. The gate bias dependence of the spatial interface trap distribution is in agreement with the localized impact ionization peak shown in Fig. 5a and 5c. By increasing the gate bias the impact ionization peak, hence the region where electron feature high kinetic energy, moves toward the drain creating defects at the silicon/oxide interface (Figs. 8 and 9). It is worth noting that cuts C3 and C4 are not shown in Fig. 8b because the corresponding N_{IT}, as can be observed in Fig. 9b, is below 10^9 cm^{-2}, hence negligible.

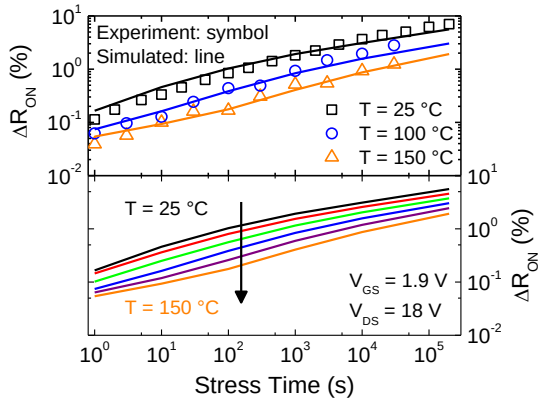

Fig. 10. Experimental (symbols) and simulated (line) R_{ON} degradation for V_{GS} = 1.9 V, V_{DS} = 18 V and different temperatures (from 25 to 150 °C with 25°C step).

Finally, in order to further validate the correct implementation of the HCS model, the device degradation has been characterized at different stress temperatures. Fig. 10 shows the ON-resistance degradation as a function of ambient temperature, both experiments (symbols, Fig. 10a) and simulation data (lines, Fig. 10) are reported. As expected for the single-electron hot-carrier process, by increasing the temperature during the stress, the ΔR_{ON} is reduced because of the phonon increase: the electron-phonon interactions tend to redistribute electrons from the high-energy tail to lower energies, thus reducing the HCS processes. As the HCS model in [7] accounted for the physical dependence on temperature, an agreement with experiments has been obtained.

5. Conclusions

In this work, we investigated the hot carrier degradation in medium rated voltage N-drift LDMOS transistors with a customized thick oxide instead of the conventional shallow-trench isolation one.

In particular, the HCS degradation has been experimentally characterized by means of different stress conditions. Then, by exploiting a preliminary device calibration, the ON-resistance degradation induced by HCS has been fully reproduced by TCAD simulations for an extended range of voltages and temperatures, highlighting the single high energetic particle as the dominant process inducing a bond-breakage event and hence device degradation.

Thanks to this approach, the charge trapping responsible for the R_{ON} degradation has been identified and spatially localized at the silicon/oxide interface of the selective LOCOS.

Finally, the TCAD analysis has been validated against experiments up to 150 °C.

Acknowledgements

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