Avalanche ruggedness of parallel SiC power MOSFETs

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Abstract

The aim of this paper is to investigate the impact of electro-thermal device parameter spread on the avalanche ruggedness of parallel silicon carbide (SiC) power MOSFETs representative of multi-chip layout within an integrated power module. The tests were conducted on second generation 1200 V, 36 A – 80 mΩ rated devices. Different temperature-dependent electrical parameters were identified and measured for a number of devices. The influence of spread in measured parameters was investigated experimentally during avalanche breakdown transient switching events and important findings have been highlighted.

1. Introduction

Power modules usually comprise of many chips connected in series and parallel in order to obtain higher voltage and current ratings for higher power applications. However, as a result of paralleling multi-chips within an integrated power module, derating rules usually need to be imposed to account for the impact of electro-thermal parameter spread within devices alongside other mismatches that may arise due to packaging related issues. Electro-thermal device parameters such as on-state resistance ($R_{DS,ON}$), threshold voltage (V_{th}), breakdown voltage (V_{BD}), trans-conductance (g_f) and thermal impedance (Z_{th}) as well as assembly layout related issues may result in significant thermal unbalances due to uneven current and power distribution within the power module during fast switching transient events (e.g. short-circuit and unclamped inductive switching). As a result of these mismatches, some devices would observe enhanced stress conditions as compared to others causing them to degrade faster and in some conditions, may also lead to premature destructive failure of the whole module [1, 2].

SiC is a wide bandgap semiconductor which possess high breakdown voltage, fast switching speed and excellent thermal conductivity which has subsequently resulted in rapid development of SiC Power MOSFET device technology over the past few years. As technology at discrete device level has substantially improved, extensive industrial and research efforts are being made to produce power modules for applications such as photovoltaic, electric vehicles and automotive industry. However, device parameter mismatch within devices going in the module should be contained to avoid unacceptable temperature gradients inside the module during transient conditions. Fig. 1 represents a bespoke SiC power MOSFET module which can be used as either a 3-phase single chip half-bridge type of switch, or as a single-phase half-bridge with parallel chips for higher current rating [3].

Fig. 1. Multi-chip layout of SiC MOSFET power module

Furthermore, in addition to the abovementioned reasons, mismatches and thermal unbalances within modules can also arise from the different cooling

techniques implemented by the end-user which is not down to the manufacturer. Such mismatches and device parameter spread usually introduce temperature gradients (10 – 15 °C) in the module during nominal conditions. Such levels of temperature gradient may be acceptable during nominal operating conditions, however, this temperature gradient alongside device parameter spread can be found to be really critical for device's robustness during fast transient switching conditions and therefore motivates the basis of this dedicated study on SiC MOSFETs. Various recent studies presented in [4 – 7] have investigated the effect of parameter spread during on-state and double-pulse switching performance but no studies seem to exist demonstrating current sharing during avalanche breakdown operation. Some recent studies on single discrete devices during SC and UIS detailing electro-thermal characterisation could also be found in [8 - 10].

2. Device parameter spread and experimental results during avalanche breakdown

2.1. Methodology and Device Parameter Spread

The study presented here focuses on unclamped inductive switching (UIS) of 1200 V, 36 A – 80 mΩ SiC power MOSFETs during paralleling operation. Circuit schematic used for paralleling devices is a modified double pulse test circuit to accommodate two devices in parallel as presented in Fig. 2. For this study, a total of 14 devices of same type were selected. The distribution of V_{th} values (case temperature; T_{CASE} = 25°C) for these 14 devices have been presented in Fig. 3. For example, in the worst case scenario, ΔV_{th} for two devices could easily be approximately up to 1 V. Even-though, the measured values are within the specified data-sheet range, such huge ΔV_{th} can be problematic when it comes to paralleling devices. Fig. 4 presents V_{th} variation versus temperature for two devices which shows that the parameter spread is not strictly constant over range of T_{CASE}. It is worth noting that ΔV_{th} at 25°C was 0.26 V which became 0.45 V at 150°C.

Spread of V_{BD} was also measured for T_{CASE} = 25°C which is presented in Fig. 5. Here, in the worst case scenario, ΔV_{BD} of two devices could easily be up to 50 V. Through examining the measured spread of the different parameters, experiments were designed to cover three different scenarios as presented in Table 1. As per the general trend observed here, the devices with lower V_{th} have higher V_{BD} and vice versa. However, this is not always the case as different scenarios that can occur are presented in Table 1.

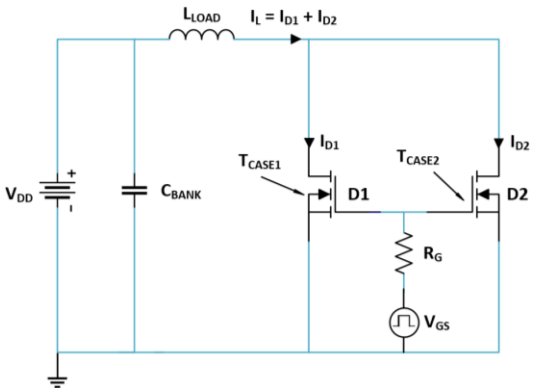


Fig. 2. UIS Circuit schematic for 2 parallel devices

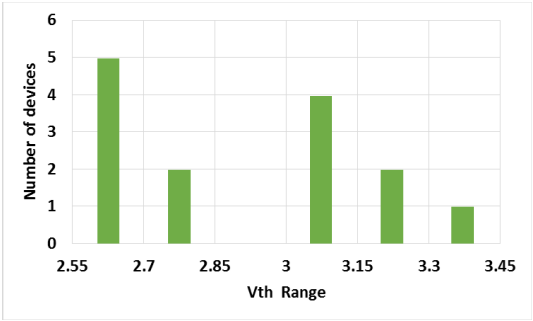


Fig. 3. Distribution of measured V_{th} for 14 device samples; T_{CASE} = 25°C; ΔV_{th} = 0.92 V for worst case scenario

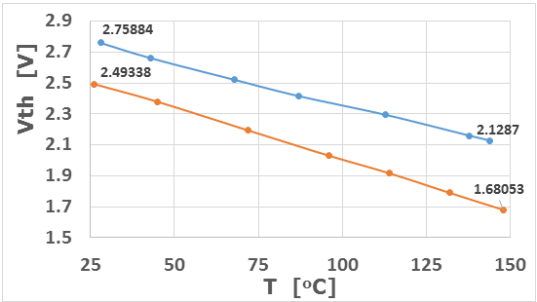


Fig. 4. V_{th} versus T_{CASE} for 2 devices showing V_{th} temperature variation

Table 1
Summary of different test scenarios

Scenario	D1	D2
S1	Higher V_{BD}; Lower V_{th}	Lower V_{BD}; Higher V_{th}
S2	Higher V_{BD}; Higher V_{th}	Lower V_{BD}; Lower V_{th};
S3	Same V_{BD}; Lower V_{th}	Same V_{BD}; Higher V_{th}

The scenarios discussed here were chosen carefully to investigate the impact of spread in each device parameter during UIS test condition. Moreover, all necessary efforts were made to ensure that the parasitic elements are kept to the minimal as well as balanced for each device since entirely, this investigation focuses on device parameter spread only.

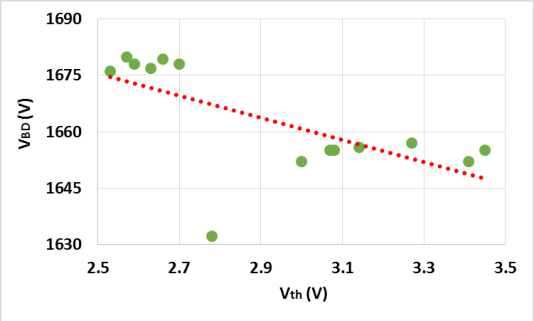


Fig. 5. Measured V_{BD} versus V_{th} for 14 device samples; ΔV_{BD} = 48 V for worst case scenario

2.2. Experimental Results

Some illustrative waveforms for scenario S1 are presented in Fig. 6 (a) – (c) showing a progressive shift of drain current (I_D) from the device with lower V_{BD} (Dev06) to the device with higher V_{BD} (Dev14). The summary of test conditions is presented in Table 2. The peak avalanche current (I_{AV}) in each device was controlled using input voltage (V_{DD}) and pulse width (t_{PULSE}) sent to both devices. Here, it is important to note that the current distribution within both devices tend to become a little uniform as I_{AV} and avalanche energy (E_{AV}) is increased for both devices. Due to heating up of the devices during avalanche breakdown, V_{BD} of the device with lower measured V_{BD} value tends to increase which progressively results in voltage level becoming equal to the V_{BD} value of the device with higher measured V_{BD} value thus explaining the progressive shift in drain currents. In the case of UIS, the energy dissipation during avalanche breakdown stage (E_{AV}) is calculated using equation 2. Moreover, the effect of spread in $R_{DS,ON}$ is also evident by the uneven current sharing during on-state device conduction prior to avalanche breakdown. To demonstrate the mismatch in V_{th}, a zoom-in of the drain currents for both devices turning off and subsequently entering avalanche phase is also presented in Fig. 7.

$$E_{AV} = \frac{1}{2} L_{LOAD} {I_{AV}}^2 \cdot \frac{V_{BD}}{V_{BD} - V_{IN}} \qquad (2)$$

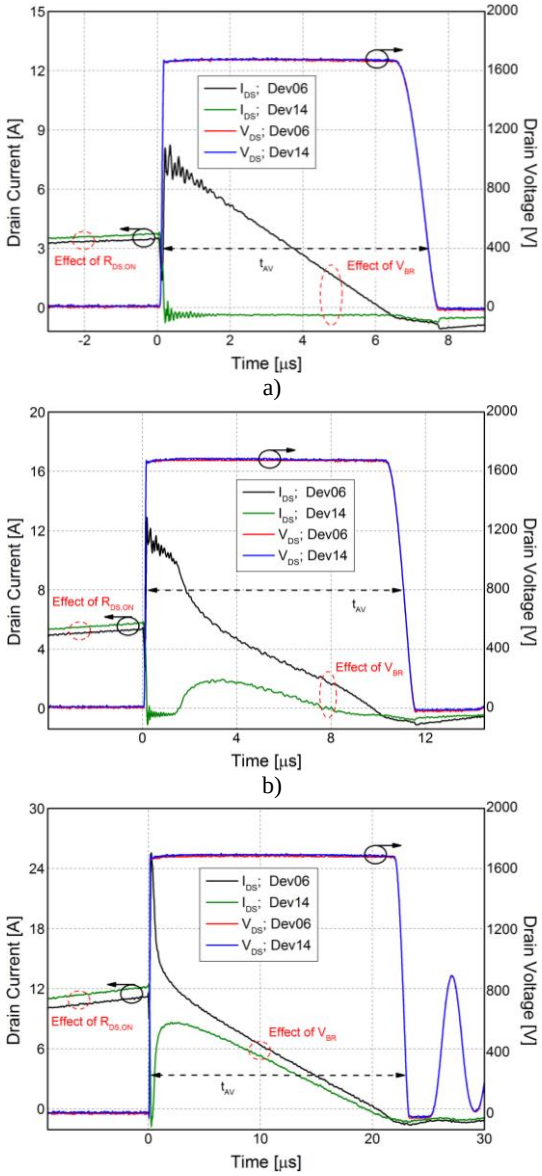


Fig. 6. Progressive shift of drain current during scenario S1, ΔV_{BD} = 28V;
a) - V_{DD} = 200 V, t_{PULSE} = 50µs; b) - V_{DD} = 300 V; t_{PULSE} = 50µs; c) - V_{DD} = 400V; t_{PULSE} = 82µs

Table 2
Summary of test results presented in Fig. 6; Scenario S1

Scenario	**D1 (Dev14)**	**D2 (Dev06)**
S1	V_{BD} = 1680 V; V_{th} = 2.57 V; $R_{DS,ON}$ = 80 mΩ	V_{BD} = 1652 V; V_{th} = 3.41 V; $R_{DS,ON}$ = 83 mΩ
T_{CASE1} = T_{CASE2} = 25 °C; L_{LOAD} = 1 mH; V_{GS} = 18 V; V_{DD} = 200 V – 400 V		

As can be seen, device having higher V_{th} (Dev06) turns-off first followed by the device with lower V_{th} (Dev14). Both of the devices start to turn off, however, the device with lower V_{BD} immediately goes into avalanche thus the drain current in that device increases taking up all the inductor current. Afterwards, the current sharing between the devices normally depends on how much the device with lower V_{BD} heats up creating a progressive shift in drain currents as demonstrated in Fig 6. Another example of scenario S1 is presented in Fig. 8 where a smaller load inductor (L_{LOAD}) was used to achieve a higher current being switched for the devices. The current being switched was increased to approximately 46 A. For this case, current sharing becomes even more uniform. In Fig. 8, another important observation to be made about the device with higher V_{BD} and lower V_{th} (Dev11) which doesn't attempt to fully turn-off (current does not go all the way to 0) and instead enter avalanche breakdown as a result of an increase of V_{BD} for Dev01 as it heated up. Increasing the peak avalanche currents and/or avalanche energies might further facilitate to uniformly distribute currents. However, it is really crucial that the current among devices connected in parallel become perfectly uniform well before the critical energy (i.e. failure) of the device with lower V_{BD} (since it is the 1st one to go into avalanche i.e. higher junction temperature (T_J) compared to the device with higher V_{BD}). In that case, when the current amongst devices connected in parallel is perfectly uniform, instead of premature failure, one of the device would fail randomly. The test conditions for results presented in Fig. 8 are summarised in Table 3. The results for Dev01 and Dev11 in Fig. 8 show no current unbalance during on-state prior to avalanche breakdown since their $R_{DS,ON}$ values were very close to each other as included in Table 3.

Table 3
Summary of test results presented in Fig. 8; Scenario S1

Scenario	**D1 (Dev11)**	**D2 (Dev01)**
S1	V_{BD} = 1678 V; V_{th} = 2.59 V; $R_{DS,ON}$ = 79 mΩ	V_{BD} = 1656 V; V_{th} = 3.14 V; $R_{DS,ON}$ = 80 mΩ
$T_{CASE1} = T_{CASE2}$ = 25 °C; L_{LOAD} = 50 µH; V_{GS} = 18 V; V_{DD} = 400 V		

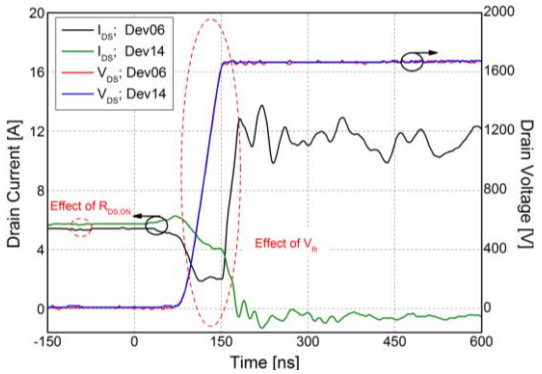


Fig. 7. Zoom-in for Fig. 6 (b); Effect of V_{th}; V_{th} = 0.84 V

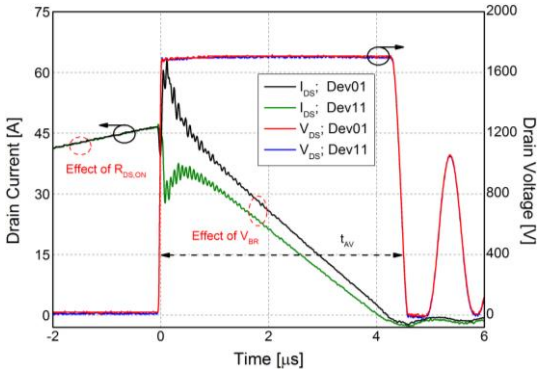
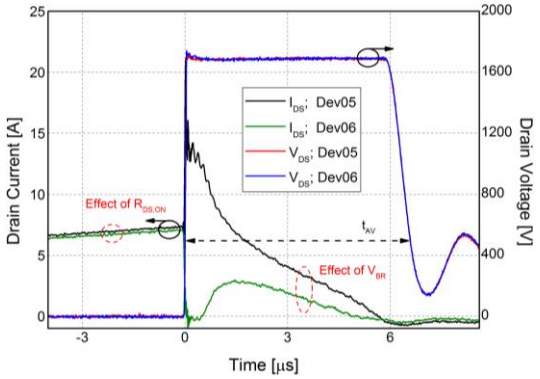
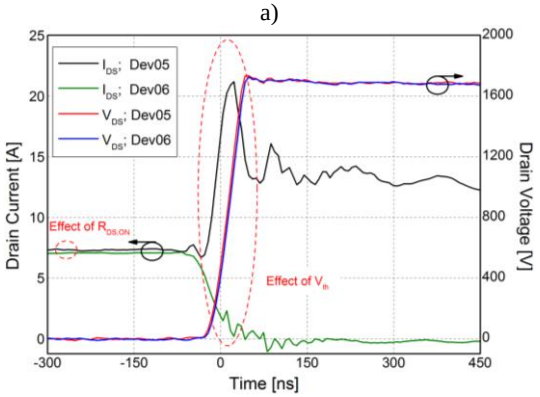


Fig. 8. Scenario S1; Results at higher switching current

Some experimental results representing scenario S2 are also presented in Fig. 9 (a) and (b). Here, the observation regarding the progressive shift in the drain current remains the same as illustrated in Fig. 6. An important point to be noted here is that the current sharing between any two devices for given test conditions would be different depending on how far apart the spread is between the device parameters. However, in this scenario (S2), the device turn-offs are particularly of great interest. Here, since device with lower V_{th} also has lower V_{BD} (Dev05), it straight away enters avalanche without a decrease in the drain current at turn-off (i.e device does not attempt to turn-off) as shown in Fig 9 (b). Another important point is that even when the device with lower V_{BD} heats up to balance the currents, current re-balancing is only partial which does not prevent uneven stresses and potential risk of failure. Moreover, non-uniform current sharing can also result in faster degradation of some devices as compared to others. The test conditions for results presented in Fig. 9 are summarised in Table 4.



a)



b)

Fig. 9. Scenario S2; a) - Uneven current sharing during avalanche; b) - Zoom-in; Effect of V_{th};

Table 4
Summary of test results presented in Fig. 9; Scenario S2

Scenario	**D1 (Dev06)**	**D2 (Dev05)**
S2	V_{BD} = 1652 V; V_{th} = 3.41 V; $R_{DS,ON}$ = 83 mΩ	V_{BD} = 1632 V; V_{th} = 2.78 V; $R_{DS,ON}$ = 84 mΩ
T_{CASE1} = T_{CASE2} = 25 °C; L_{LOAD} = 1 mH; V_{GS} = 18 V; V_{DD} = 200 V		

S3 dictates a scenario when current sharing between both devices would be nearly perfectly uniform. For curiosity, experiments for scenario S3 were also carried out and selected results are presented in Fig. 10. In scenario S3, effect of spread in V_{th} is still present, however, it is prevailed as a result of the devices having approximately the same V_{BD} values. Moreover, the spread in $R_{DS,ON}$ is clearly evident from the on-state conduction prior to avalanche state as illustrated in Fig. 10.

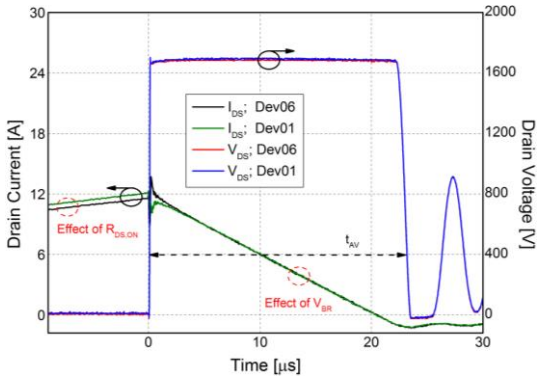


Fig. 10. Scenario S3; Results showing perfect current sharing among devices

Table 5
Summary of test results presented in Fig. 10; Scenario S3

Scenario	**D1 (Dev01)**	**D2 (Dev06)**
S3	V_{BD} = 1656 V; V_{th} = 3.14 V; $R_{DS,ON}$ = 79 mΩ	V_{BD} = 1652 V; V_{th} = 3.41 V; $R_{DS,ON}$ = 83 mΩ
T_{CASE1} = T_{CASE2} = 25 °C; L_{LOAD} = 1 mH; V_{GS} = 18 V; V_{DD} = 400 V		

Ideally, when it comes to paralleling devices, one would want devices without any spread in device electro-thermal parameters. However, this can hardly be the case since device manufacturing procedures would normally introduce some sort of imbalance giving rise to parameter spread. From the results presented here, SiC power MOSFETs show a wide spread in device parameters even though the values of these parameters are within their ranges provided on the datasheet. It is still needed that the spread in device electro-thermal parameters is contained as an effort at the device manufacturing level (i.e. bare-die device technology). Moreover, to overcome the spread in device parameters, devices should be selected after careful static device characterisation of bare dies prior to packaging of modules having devices connected in parallel. Finally, the failure mechanism of SiC power MOSFETs can be found in [11]. In [11], investigations have shown that the device fails as a result of thermal runaway. The interpretation of failure mechanism is beyond the scope of this paper.

3. Conclusion

An in-depth understanding of the influence of devices' electro-thermal parameter spread in SiC power MOSFET technology on the performance of the devices is essential to aid development of robust multi-chip integrated power modules. Effect of different device parameter spread such as V_{th}, V_{BD} and $R_{DS,ON}$ have been investigated as part of this study and important observations have been highlighted in this paper. Such investigations are crucial when it comes to paralleling bare-die devices within modules to ensure containment of parameter unbalances to minimize current unbalancing between devices. Moreover, bespoke device package development is also needed to ensure containment of parasitic inductance and thermal impedance unbalances within the module.

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