A lightweight write-assist scheme for reduced RRAM variability and power

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Abstract

Common problems with Oxide-based Resistive RAM are related to high variability in operating conditions and high programming currents during FORMING, SET and RESET operations. Although research has taken steps to resolve these issues, variability combined with high programming currents remains an important characteristic for RRAMs. In a conventional write scheme with fixed duration and amplitude, the programming current is not controlled, which degrades the cell performance (power consumption and variability) due to over-programming. In this paper, a self-adaptive write driver is proposed to control the write current. A feedback mechanism based on current comparison is used to switch off the write stimulus as soon as the preferred write current is reached. Compared to conventional write schemes, in the proposed write-assist circuit, the write energy per bit is reduced by 27% and the standard deviation of post-FORMING distributions is reduced by 57%.

1. Introduction

Emerging technologies such as Resistive RAMs (RRAMs) are attracting considerable attention due to their tempting characteristics such as high scalability, CMOS compatibility and non-volatility to replace current conventional memories [1] [2]. A typical RRAM device consists of two metallic electrodes that sandwich a thin dielectric layer serving as a permanent storage medium. A single RRAM bit-cell can be switched between two distinct states: High Resistance State (HRS) and Low Resistance State (LRS), representing the low ('0') and high ('1') states, respectively. The transition from HRS to LRS is referred to as SET, while the opposite transition from LRS to HRS is referred to as RESET (RST). Prior to performing SET or RST, a FORMING (FMG) step is required, which is achieved one time in the device life. The FMG step is a voltage-induced resistance switching from an initial virgin state with a very high resistance to a conductive state. High voltage is typically needed during FMG since it generates the prerequisite number of defect species within the thin dielectric layer to construct a Conductive Filament (CF) [3]. However, FMG increases power consumption and the high voltage can initiate thermal damage, if not controlled [4]. V_{fmg}, V_{rst} and V_{set} are the voltages required across the RRAM cell for its operation. In the rest of the paper, a FMG, SET or RST operations will be considered as a write operation. The read-out operation is performed with a low voltage, V_{read}, whose value is chosen to preserve the resistance state.

The conventional write scheme uses single pulse voltage with a fixed-pulse duration, resulting in over-SET and over-RST for fast RRAM cells. Consequently, power consumption is very high for such cells, especially after the resistance has been switched from HRS to LRS.

Write current control remains one of the main factors for improving key performance markers of RRAMs. Indeed, it has been demonstrated that high endurance

and retention are closely linked to the programming currents since excessive and insufficient currents can result in failure [5] [6]. In this context, programming algorithms and write assist circuits play a crucial role on performance and yield optimization [7]. Program-verify algorithms have been developed to ensure distinct resistance distributions; they adjust the write signal (pulse number, width or amplitude) until the cell resistance reaches the target resistance state. However, in this scheme, the writing is interrupted periodically to allow for the read operations to verify that switching has occurred, which increases the write-time significantly.

An alternative to avoid the use of read operations is to implement a write-termination scheme at the memory driver level where the write current pulse is cut-off right after the resistance transition completes. This prevents wasted write energy but introduces an important area overhead. For instance, in [8], such a scheme is implemented using an op-amp, a differentiator and additional capacitors and resistors.

In this paper, we propose a cost-efficient self-terminated write driver based on write current control. Instead of detecting the resistance state transition, the driver compares the memory cell current with a reference current during write operations and terminates the write operation when the RRAM cell current matches the reference current, which is chosen high enough to ensure that write operation is complete. In addition, the reference current can be adjusted to allow a full control of the write energy. No read operation is involved in the process and no RRAM reference cells are needed. Moreover, the self-terminated write driver area overhead is very low compared to state-of-the-art write drivers. To the authors' knowledge, this is the first work which presents the integration of a compact self-adaptive write driver with a minimal area overhead (i.e. a dozen of transistors). Section 2 presents the Write-Assist Scheme. In section 3, simulation results are provided. Section 4 concludes the paper.

2. Proposed Scheme

2.1. Current Sensor

Fig. 1 shows the circuit diagram of the built-in current sensor incorporated in the write driver design. The current sensor is inserted in series between the memory cell and GND to sense the memory cell current, I_{cell}. The sensor is in fact a current comparator inspired from Built-In Current Sensor (BICS), extensively used for I_{ddq} testing [9]. It consists of a current differential amplifier (M2, M3) and two current mirror pairs (M1, M2 and M3, M4). The n-MOS current mirror (M1, M2) is used to mirror the current from a constant current source delivering a reference current, I_{ref}. The current mirror (M3, M4) is used to mirror and amplify the current difference (I_{cell}-I_{ref}) to the output inverter. The differential pair (M2, M3) calculates the difference between the reference current I_{ref} and the cell current I_{cell}. Hence, the current through M3 is equal to I_{cell}-I_{ref}. If (I_{cell}-I_{ref}) > 0, then I_{cell} flows throw M2 and no current flows through M3. The inverter input *A* is set high and the comparator output *out_comp* is set to low. When I_{cell} just exceeds I_{ref}, a current start to flow through M3. This current is amplified and the inverter input *A* is grounded. As a result, the comparator output *out_comp* switches from a low level to a high level. At this point, the current through the cell is equal to I_{ref}. In normal operating conditions, the constant reference current is set to the desired FMG, SET or RST current. In the present work, I_{ref} nominal value is set to 100µA.

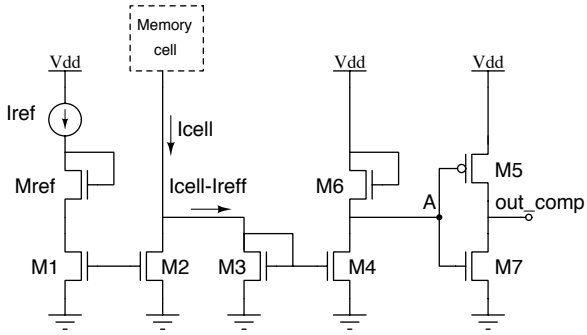

Fig. 1. Built-in current comparator

Before its integration at a memory array level, the current comparator ability to detect a specific current is evaluated. For a set of I_{ref} current values in the range [60µA–160µA], the cell current detection accuracy is evaluated by monitoring the comparator output. In Fig. 2, the relative current difference, ΔI, is plotted versus I_{ref} when *out_comp* switches from low to high. If I_{ref} current nominal value is considered (i.e. 100 µA), the detection precision is less than 0.1 %. For I_{ref} variation in the range [60µA-160µA] with a 10uA step, the detection precision is in the range [-1.46%–0.94%] which demonstrates the ability of the comparator to accurately detect specific I_{cell} values.

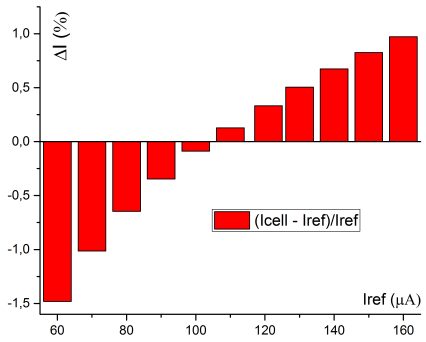

Fig. 2. Current comparator evaluation

2.2. Write Assist Circuit

Fig. 3 presents a part of the RRAM memory array, considered in this work, which is composed of a word line driver to select the active row (WLx), a bit line driver to select active bit lines (BLx) during a SET operation and a source line driver to select a specific source line (SLx) to reset a whole memory word. Sense amplifiers are used to convert the cell current into a logical value at the circuit output during a read operation. The 1T/1R memory cell (one MOS transistor in series with one resistor) is considered. Memory cells are usually grouped into 8, 16 or 32 bits to form a memory word. The memory cell is modelled by an Oxide-based RRAM model fully calibrated on silicon for a *TiN/Ti/HfO$_2$/TiN* RRAM stack [10].

Either DC or pulse stress can be used to carry out a write operation. In a practical memory application, pulse programming is preferred, while DC operations are ideal for studying the switching mechanism. Thus, a pulse generator is used to operate memory cells.

The memory array presented in Fig. 3 comes together with the proposed write driver presented in Fig. 4. For clarity, the write driver is associated with a single memory cell. Before any write operation, the bit line driver is enabled by setting the RS latch. If the memory cell is selected and a write '1' operation is performed (i.e. *ADR* and *DATA* signals set High), voltage pulses coming from the pulse generator, "Pulse Gen", are applied without any interruption and the cell current is measured while the write pulse is being applied. The current comparator detects whether the cell current I_{cell} reaches the reference current I_{ref} and turns off the pulse generator. At this point, *out_comp* signal goes High and resets the RS latch, which in turn disables the bit line driver (via Q signal) and turns off the pulse generator (via $\bar{Q}$ signal). At the same time, the write driver is disconnected. The next write operation starts when the RS latch is set.

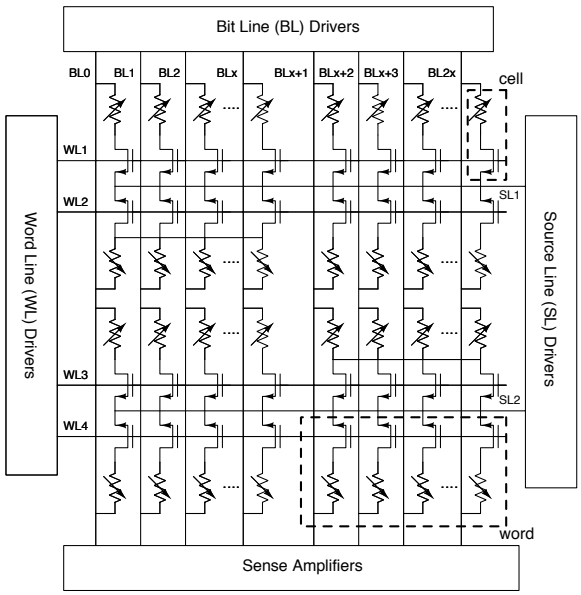

Fig. 3. Elementary memory array used for simulations

This scheme allows a strict control of the write current, which is highly desirable. Indeed, the transition from the HRS to the LRS during a FMG/SET operation requires current compliance to prevent destruction. As current flows, the cell resistance is reduced, and as such, more current flows as write pulses are applied. This positive feedback mechanism causes large currents to flow, which can cause permanently open or shorted cells. Therefore, current compliance in the FMG/SET direction is a requirement at the circuit level.

During a RST operation, as the current flows, the resistance of the cell increases, causing current to reduce. Therefore, the RST operation is a negative feedback mechanism and a current compliance during a RST operation is not mandatory. However, having compliance in the RST direction allows an upper limit to be placed on the amount of current delivered to the cell, which is useful for power monitoring or when sizing an access device for a 1T1R architecture. The presented write scheme can be easily applied during a RST operation; the write operation is performed by biasing the memory cell in the opposite polarity. RST pulses are applied to the memory cell bottom electrode via the select transistor through the source line driver and the other terminal of the cell is connected to the current comparator.

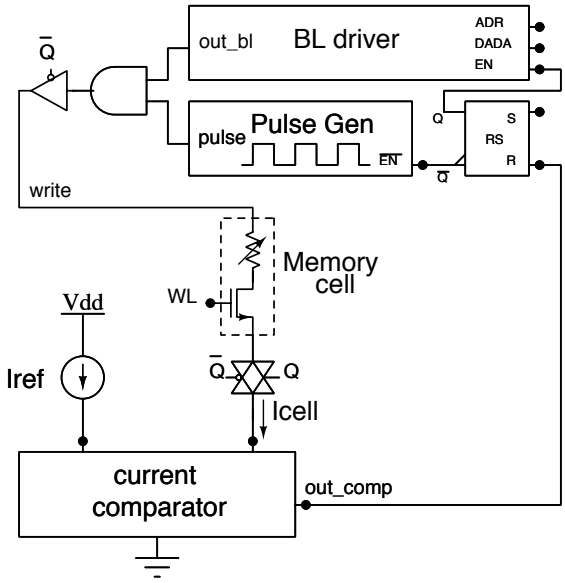

Fig. 4. Write assist circuit FMG/SET operation

3. Simulation Results and Discussion

3.1. Transient Simulation Results

We implemented the circuit in Fig. 4 using a 0.13µm High Voltage CMOS technology with a 3.5V supply voltage. As already mentioned, high voltages are needed during the FMG step, which is the first and most critical operation as it involves high currents and determines the switching characteristics during the future operation of the memory cell. To verify the operation of the write scheme, SPICE simulations are performed using the *Eldo* simulator.

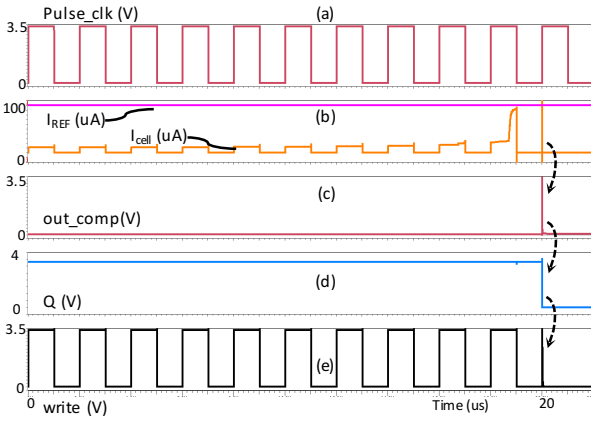

Fig. 5. Transient simulation results

Fig. 5 shows transient simulation results. Write pulses *Pulse_clk* (Fig. 5a) are generated without any interruption and the cell current I_{cell} is measured and compared to the reference current I_{ref} (Fig. 5b). As the number of pulses increases, the cell resistance decreases which in turn increases the cell current. When the cell current reaches the reference current value set to 100µA (Fig. 5b), *out_comp* signal switches from a low to a high level (Fig. 5c). The *out_comp* signal resets the RS flip-flop (Fig. 5d). As a result, RS flip-flop output Q goes low ($\bar{Q}$ goes high) finishing the pulse write operation (Fig. 5e).

3.2. Monte Carlo Simulations Results

In HfO_2-based RRAM, considered in this study, variability remains a concern since it is intrinsic to the nature of the resistive switching process [11] [12]. The exact location and size of the CF (Conductive Filament) formation and rupture cannot be reproduced from cycle to cycle or from device to device. To assess the impact of the write scheme on variability, a Monte Carlo (MC) analysis is conducted. As a result, the CF distribution size obtained from the OxRAM model is extracted. The CF size parameter is considered as a key parameter as the CF construction/destruction sets all the other parameters of the memory cell (resistance, current, etc.) [13].

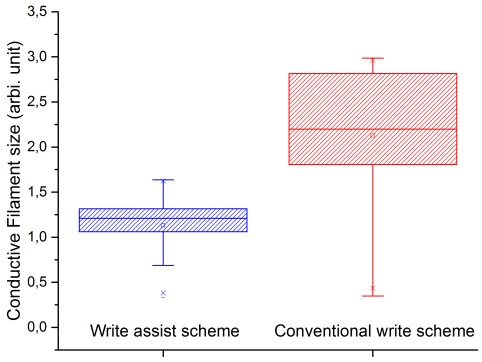

Fig. 6. Transient simulation

Two configurations are considered. The first one takes advantage of the write assist circuit during the write operation. The second one uses a conventional program scheme with a fixed number of programming pulses which is set to 10. This number is extracted from Fig.5e, which corresponds to the number of pulses needed to get a 100µA write current for a nominal memory cell. Since cell variability is generated based on a targeted technology (i.e. model calibrated and featuring a variability dependency) only actual possible variations are reported [10]. Fig. 6 presents the impact of the memory cell variability

on post-FMG distributions after 500 MC simulation runs, using a box-plot.

Several observations can be made. The median value of the CF is more important for the conventional scheme compared to the write assist scheme. This is explained by the voltage headroom reduction seen across the cell in the write assist scheme configuration. Indeed, the voltage drop across the current comparator reduces the write efficiency. Therefore, the CF size is more important in the conventional write configuration (i.e. larger conductivity). Regarding the distribution spreads, the write assist configuration clearly tightens the CF distribution spread (by 57%) and demonstrates the capability of the write assist scheme to reduce variability. Regarding the power consumption, the maximum current observed after 500 MC runs is 221µA for the conventional configuration and 100µA for the write assist configuration. The average power consumption during the entire write operation is 15.1µA for the conventional configuration and 11µA for the write assist. Simulation results are summarized in Table I.

TABLE I. SIMULATION RESULTS

	Conv. scheme	**Proposed scheme**	**Δ(%)**
MC runs number	500	500	
Minimum CF size	0.348	0.331	
Maximum CF size	2.986	1.636	
Mean CF size	2.129	1.130	
Max. current (µA)	221	100	**54.7%**
Std. deviation	0.715	0.306	**57%**
Avg. current µA)	15.1	11.0	**27.1%**

4. Conclusion

The current work provides a simple and feasible solution to two of the most challenging issues in filamentary-based RRAM devices related to the control of the consumption current and the stochastic nature of the resistive switching mechanism during write operations. The presented write scheme can be used as a powerful tool for process variability and current consumption reduction during RRAM circuit operation. The write circuit is exclusively based on current control during write operations to ensure that write operations are complete for a targeted write current. The write energy per bit is reduced by 27% and the standard deviation of post-FMG distributions is reduced by 57%.

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