Introduction to the special issue on SMACD 2012

Welcome to the Special Issue devoted to the 2012 edition of the International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD). This is the XIIth edition of the conference, and it was held on 19–21 September 2012 in Seville, Spain. SMACD originated from a specialized workshop in 1991 in Paris and since 1992 it became a biannual event. Throughout this 20 past years, the conference has been organized at various locations in Europe (Italy, Spain, Belgium, Germany, Portugal, Romania and Poland) and, in 2010, in Tunisia.

During the past few years, the conference has increased in size and has been adapting its scope to become a reference forum for design methods and tools for analog, mixed-signal, radiofrequency and multidomain integrated circuits and systems. SMACD 2012 received a total of 113 submissions from 30 different countries. The Technical Programme Committee and the Technical Programme Chairs, supported by 45 external reviewers, had a tough work selecting 52 papers for oral presentation and 12 papers for poster presentation. Plus, SMACD 2012 hosted a student competition where students competed with their best ideas, methodologies, flows and tools with a unique challenging goal: improve design automation of integrated circuits and systems. The winner of this competition is also included in this Special Issue.

This Special Issue of the Analog Integrated Circuits and Signal Processing Journal consists of the expanded and carefully revised versions of a selection of papers presented at SMACD 2012. This selection was based on quality criteria and they reflect the various topics highlighted during the conference. After the assessment of the reviewers, eleven papers have been accepted for publication. Selecting only these papers was a challenging task and we are aware that we probably missed excellent contributions. We, however, believe we did our best at putting together a special issue as complete as possible. All contributions were subject to the standard journal peer-review process of the Journal.

The first paper, by J. Martín-Martínez et al. describes RELAB, a new simulation tool for circuit reliability evaluation. This tool allows considering MOSFETs threshold voltage shifts (due to process variability and/or degradation mechanisms) and gate leakage current increase after dielectric breakdown during the SPICE circuit simulation and it is based on physical models of the phenomena with experimentally determined parameters.

The second paper, by Javier Sieiro et al. presents a bisection algorithm for the synthesis of planar inductors that uses a fast electromagnetic analysis algorithm. Both algorithms are based on a set of heuristic and physical rules obtained from the study of the electromagnetic behavior of these planar devices. This allows keeping the number of iterations moderately low and speeding up the analysis without compromising accuracy. The proposed solution is demonstrated through the development of an inductor library for a LTCC technology.

M. Kotti et al. introduce, in the third paper, a key enabler in the success of design methodologies for radiofrequency circuits: the early availability of feasible trade-offs between inductance, quality factor, self-resonance frequency and area. This is done by first generating a Pareto-optimal performance front of integrated inductors and, second, creating a surrogate model of this performance front. Experimental results in a 0.35-lm CMOS technology are provided.

The fourth paper, by P. Pereira et al. considers the challenging task of on-chip LC tank design for LC-VCO circuits. The work presents a model-based optimization approach that uses a set of analytical models describing each circuit element performance in the oscillator. Through a set of working examples for a 130-nm process, the potential of genetic algorithms in yielding accurate and timely efficient oscillator designs is demonstrated and validated against HSPICE/RF simulations.
The following paper, by Piet Callemeyn et al. presents a framework to co-optimize the circuit and the layout parameters of fully integrated inductive DC-DC converters. The optimization in this framework is speeded up by using active learning sample selection and evolutionary optimization techniques. A fully-integrated DC-DC boost converter in a 130-nm CMOS process is used to validate the solution proposed in this paper, with significant improvements in power loss and efficiency when compared to a fully-integrated DC-DC boost converter with a regular inductor topology.

In the sixth paper, Ricardo Martins et al. provide a multi-objective multi-constraint routing approach integrated in an analog integrated circuit layout generator based on template descriptions and evolutionary computation techniques. This approach puts special emphasis to the reusability of expert design knowledge and to the efficiency on retargeting operations. Analog demonstration examples (in a 130-nm CMOS process) are provided.

Ahmet Unutulmaz et al. present, in the seventh paper, a declarative language (LDS) intended to code analog layout templates that can be used for layout-aware circuit synthesis. Typical analog layout constraints such as alignment, abutment, and symmetry can be efficiently handled by this language. A Capture tool (by which a template can be extracted from an expert-drawn layout) is also described.
The work described in this paper allows for a simpler and more efficient way to facilitate the always complex creation of analog layout templates.
The eighth paper, by Adam Cooman et al. describes a method to determine the dominant source of non-linear distortion in two-stage op-amps. This method combines the best linear approximation (BLA) technique with a classical noise analysis in this paper. The analysis described in the paper pinpoints the non-linear hot-spots in an efficient way, without the use of special simulations, manual analytical calculations or modified transistor models.
A novel identification technique for the extraction of lumped circuit models of general distributed or stray devices is presented in the ninth paper, written by Antonio Luchetta et al. This technique is based on two multi-valued neuron neural networks used in a joined architecture able to extract hidden parameters.

In the tenth paper, Michael Zwerger et al. deal with the problem of automatically and reliably detecting floating nodes, a clearly not straightforward problem because numerical simulation is often not trustworthy in the presence of floating nodes. The paper presents a method for the verification of the power-down mode of analog circuits by using a voltage propagation approach based on the circuit structure. Experimental results demonstrate the effectiveness and efficiency of the presented method as well as common pitfalls of numerical simulation.

Muralikrishna Sathyamurthy et al. winners of the student competition, present in the last paper a methodology for verifying mixed-signal smart-sensor systems using the Universal verification methodology (UVM), as well as a novel solution for estimating the power consumption of the digital sub-system using application-specific randomactivity patterns generated during UVM testbench runs.

As guest editors of this special issue, we sincerely thank the authors for their valuable contributions and the responsiveness to the reviewers' comments and suggestions. We would like to specially thank all these anonymous reviewers for their feedback, providing many useful comments and constructive criticism helping ensuring a hight quality of the papers.

Finally, we are very grateful to Professor Mohamed Ismail for giving us the opportunity to lead this special issue. We also wish to express our personal gratitude to the Springer personnel for all the outstanding and efficient support we received; this special issue was made possible only with their professional help.

We hope you enjoy this Special Issue and find the contributions informative, useful and full of new insights.