

Abdulfattah AN, Tsimenidis CC, Yakovlev A.

Ultra-low power *m*-sequence code generator for body sensor node applications.

Integration, the VLSI Journal 2017

Copyright:

© 2017. This manuscript version is made available under the [CC-BY-NC-ND 4.0 license](#)

DOI link to article:

<https://doi.org/10.1016/j.vlsi.2017.10.004>

Date deposited:

13/12/2017

Embargo release date:

12 October 2018



This work is licensed under a

[Creative Commons Attribution-NonCommercial-NoDerivatives 4.0 International licence](#)



Contents lists available at ScienceDirect

INTEGRATION, the VLSI journal

journal homepage: www.elsevier.com/locate/vlsi

Ultra-low power m -sequence code generator for body sensor node applications

Ahmad N. Abdulfattah*, Charalampos C. Tsimenidis, Alex Yakovlev

School of Electrical and Electronic Engineering, Newcastle University, NE1 7RU Newcastle upon Tyne, England, United Kingdom

ARTICLE INFO

Keywords:

m -sequence code
LFSR
Sub-threshold
Power consumption
CMOS technology scaling

ABSTRACT

In this paper, a design of low power m -sequence code generator is proposed. The efficiency of producing the code sequence within the region of sub-threshold voltage is investigated using 90 nm technology and verified using the auto-correlation and eye diagram characterizations. A further method of power saving in addition to voltage reduction is carried out by scaling the technology node from 90 to 65 nm. A comparison of power consumption and maximum attainable frequency between both technologies is performed. The ratio of power saving while using 65 nm technology is ranging from 45% to 55% for the three different code lengths investigated.

1. Introduction

Body sensor nodes (BSNs) are used in many areas due to the development of wireless communication techniques. Recently, BSNs have been deployed in medical applications to improve and monitor human health as it can be placed in/on the human body, as shown in Fig. 1. In medical sensor nodes, the transceiver design is faced with numerous challenges in terms of power dissipation, size restrictions and power supply [1]. The use of large power supply (battery) will cause the node to be uncomfortable to wear, unlike the little battery, which obliges regular changing and decreases patient compliance. Energy harvesting is an alternative technique to power node transceivers with continuous energy by converting the ambient energy to electrical energy [2]. However, the performance of energy harvesting technique varies based on the type of the harvester, which, in general provides relatively low power. Thus, the need for an ultra-low power wireless transceivers becomes essential to overcome the limitations of conventional batteries and to be within the capabilities of existing harvesters.

Spread spectrum is one of the common transmission techniques used in transceiver design to enhance the link quality by spreading the user's data to a wider bandwidth and to improve jamming resistance. Pseudo-noise (PN) codes have been used to spread the information signal by multiplying the PN code by the user data [3]. However, the transceivers that deploy spread spectrum have a complex system structure and tend to consume large power. Thus, designing a low-power and complexity PN code generator can lead to enhanced efficiency. Moreover, the use of CMOS electronic circuits in such

applications has boosted their performance and reduced their size and power consumption [4]. Therefore, it is essential to analyze the power dissipation of CMOS implementations to investigate the effect of variations of the supply voltage and switching frequency on power consumption.

Recent trends on power reduction have led designers to investigate various approaches. Scaling the supply voltage is one of the successful methods, which significantly reduces the overall power consumption [5]. Operating the digital circuits within the region of sub-threshold voltage is an extreme case of voltage scaling. It has previously been observed that the minimum power consumption can be achieved by operating the circuit in the sub-threshold region [6,7]. Although the circuit switching speed might be slower at this region, however, it remains acceptable for medium performance and low power applications such as wireless sensors and biomedical applications. Owing to this, our digital circuit will be examined at sub-threshold region and implemented using 90 nm CMOS technology to analyze the impact of voltage scaling on the circuit performance with regards to power consumption and maximum achievable frequency.

One additional improvement in power consumption can be achieved by scaling the CMOS technology node. Technology scaling on digital circuits is of interest because it enables power consumption reducing, transistor switching enhancement and geometric reduction [8]. A primary concern of scaling down the technology is the leakage current, a problem which was solved in this research work by using transistors of low threshold voltage to enhance the performance at the sub-threshold region. 65 nm CMOS technology will be used besides 90 nm to demonstrate the possibility of scaling the technology along

* Corresponding author.

E-mail address: a.n.abdulfattah1@newcastle.ac.uk (A.N. Abdulfattah).

<http://dx.doi.org/10.1016/j.vlsi.2017.10.004>

0167-9260/ © 2017 Elsevier B.V. All rights reserved.

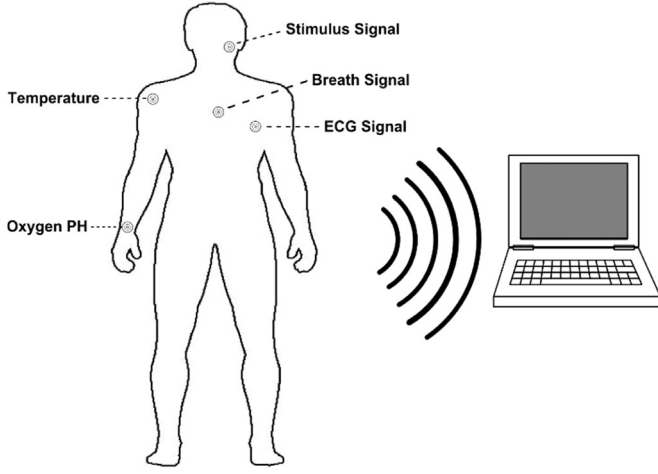


Fig. 1. Examples of medical applications of BSNs.

with variable supply voltages without affecting the functionality of the circuit.

Maximum-length sequence (m -sequence) is one of the PN code types that plays a key role in many communication technologies such as spread spectrum systems. Numerous digital circuits have used m -sequence code due to its simplicity in the design and stability in generating the code using a linear feedback shift register (LFSR) [9].

In this paper, we focus on the design and implementation of an m -sequence code generator circuit at a transistor level to operate at ultra-low power consumption that can be used in conjunction with a spread spectrum transceiver.

The contributions of this paper can be summarized as follows:

- 1) We design a low power consumption m -sequence code generator circuit that can produce a code within the region of sub-threshold voltage. This reduces the power consumption by 14%. This novelty is very important not only because it increases battery life but also reduces radiation through the patient which can potentially have serious side effects.
- 2) We modify the conventional flip-flop to be used for the code generator circuit and to provide low power consumption, small cell size, and satisfactory performance.
- 3) Through the comparison between the 65 nm and 90 nm technologies, we show that a 45–55% power reduction can be made. This is very significant as it shows the necessity of using the 65 nm technology in spite its cost as this big power reduction is of most importance to the patient health.
- 4) The feasibility of the design is verified by measuring the power dissipation and maximum achievable frequency. This is done by implementing the layout of the code generator circuit using 65 nm technology.
- 5) We provide a comprehensive analysis of the power consumption at a transistor level through extensive simulations and comparisons. This is very useful for future researchers because it shows the typical values of the supply voltage, frequency and power dissipation in each case of the three code length generators.

The remainder of the paper is structured as follows: Section 2 illustrates the design specifications and Section 3 presents the principles of m -sequence generation. In Section 4, the circuit design and its implementation are introduced, while the measurement results are given in Section 5. Scaling implications on power consumption are analyzed in Section 6. Finally, the paper is concluded in Section 7.

2. Design specifications

The m -sequence generator is a key part of any spread spectrum transceiver system [10]. At the transmitter, the baseband signal is produced by spreading the data with a sequence code to be handled thereafter by the modulator. On the other side, the same sequence is used at the receiver for de-spreading. The ability of the receiver to detect and analyze the signal depends on of the quality of the m -sequence code. Therefore, generating a sequence with high performance and high correlation is highly desirable. Practically, the m -sequence generator is commonly utilized when good auto-correlation properties is required [11]. Due to the use of transceiver in medical applications as it can be implanted inside the human body, so the m -sequence generator should be built with low power dissipation and small cell size. Consequently, the challenge in this work is to build a practical m -sequence generator that can produce a high quality code even within the sub-threshold voltage region.

The patterns of m -sequence codes used in this work have the same characteristics of power-saving pseudonoise (PSPN) code. It is approved that the use of PSPN code in correlation with spread spectrum system can achieves 14% power consumption reduction [12]. Toggle rate is an important parameter that can explore whether the code is a power saving code or not and this example of 15-bit code illustrates how the toggle rate can be calculated. Consider the code is 011011110001000, it is easily recognized that there are six toggles in one period of the code. Based on that, the toggle rate is $6/15 = 0.4$. In ultra-low power systems, a low toggle rate is highly recommended for the sake of less transition activity which in turn leads to less power consumption. The recommended toggle rate for spread spectrum systems should not exceed the value of 0.45 as high power consumption is expected upon this value. According to that, the m -sequence pattern is carefully selected in this paper to match the PSPN characteristics as the toggle rate is calculated for the code lengths of 7, 31 and 511 bits to be 0.428, 0.387 and 0.44, respectively.

In this paper, the m -sequence generator is designed to suit the spread spectrum transceiver, which operates at a frequency of 402–405 MHz Medical Implant communication Service (MICS) band, in which the transmitted power is limited to -16 dBm EIRP [13]. The transceiver is assumed to be dedicated for a single-user operation. The scenario of the application is shown in Fig. 2.

According to the above scenario, the threshold transmit power of the proposed system is found to be -23.6 dBm. This includes the processing gain of the 31-bit m -sequence code, according to the following equation

$$P_t = P_r + P_{path\ loss} - P_G, \quad (1)$$

where P_t is the transmitted power, P_r is the received power, $P_{path\ loss}$ is the path loss power of 65.4 dB [14], which includes both losses inside and outside the body, and P_G is the processing gain of 7 dB for the 31- m -sequence code. The received power, P_r , was found to be -112 dB, since the required SNR at the receiver to achieve a 10^{-3} bit error rate (BER) ratio is 8 dB, and the noise power is -120 dB.

The following are the specifications of the proposed m -sequence generator. The code length is 31-bits, with a pattern of 001001111001111000110111011100 and a supply voltage of 0.4 V. The toggle rate for this pattern is approximately 0.38 which guarantees

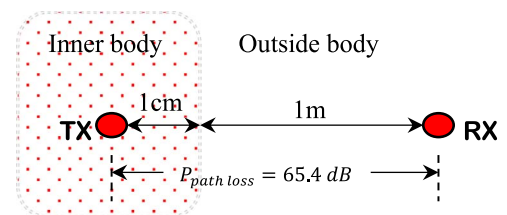
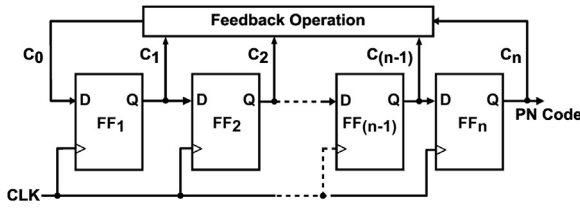


Fig. 2. Proposed scenario of the application.

Fig. 3. Schematic of m -sequence code generator.

power saving. Moreover, the CMOS is 65 nm technology with a MOSFET transistor type, and a power consumption of 1.1 μ W.

The specifications of the proposed transceiver, which uses the above mentioned m -sequence generator specifications, are as follows. The technique is spread spectrum, with a supply voltage of 0.4 V corresponding to a frequency of 403 MHz. A total bandwidth of 300 kHz is utilized with binary phase shift keying (BPSK) modulation. Furthermore, the data rate is 75.9 kbps and the receiver sensitivity is -95 dB m.

3. The m -sequence principles

The m -sequence codes are cyclic sequence which consists of binary numbers of 1's and 0's in a pseudo-random way [15]. In practice, they are generated using flip-flop (FF) based LFSRs. Among the different FF types, the D-FF is used in this paper, where registers are connected linearly to form a shift register. The outputs of the FFs of the shift register are combined using an exclusive-OR (XOR) gate to provide feedback to input of the first FF, as shown in Fig. 3. Additionally, a clock distribution network is required that activates the FFs. The length of the resulting code depends on the number, N , of shift registers. A maximum code length of $L = 2^N - 1$ bits can be generated if the feedback connections are selected based on a primitive polynomial [16].

There are two feedback shift register configurations for the m -sequence generator. For high-speed systems, XOR gates are placed between the FFs, while for low-speed systems, the XOR gates are in the feedback loop [3]. The second architecture is the method of choice due to its low power consumption. This selection does not affect the design as the m -sequence generator is placed before the modulator in the transmitter. Moreover, for small polynomials, this does not make a significant difference.

The initial state of the LFSR, referred to as the *seed*, controls the code phase [15]. All initial states are allowed, except the all-zero state, as it leads to an all-zero bit sequence. Table 1 shows feedback tap connections for different length sequences.

4. Circuit design and implementation

In this section, a CMOS circuit design for an m -sequence code generator is proposed. The power consumption for different code

Table 1
Some feedback taps of LFSR [3].

Number of stages N	Code length $L = 2^N - 1$	No. of possible codes	Feedback polynomials (octal form)
3	7	2	13
4	15	2	23, 37
5	31	6	45, 75
6	63	6	103, 155
7	127	18	211, 217
8	255	16	435, 551
9	511	48	1021, 1131
10	1023	60	2011, 2415
11	2047	176	4005, 4445
12	4095	144	10123

lengths and switching frequencies is investigated and analyzed at transistor level. For investigation purposes, three m -sequence code generators are implemented for code lengths of 7, 31 and 511 bits. The m -sequence code generators can be represented in terms of polynomials of variable X such that

$$13_8 \equiv 1011_2: f_1(x) = x^3 + x + 1, \text{ for } N = 3, \quad (2)$$

$$45_8 \equiv 100101_2: f_2(x) = x^5 + x^2 + 1, \text{ for } N = 5, \quad (3)$$

$$1021_8 \equiv 1000010001_2: f_3(x) = x^9 + x^4 + 1, \text{ for } N = 9, \quad (4)$$

where N is the number of FFs and the subscripts 8 and 2 denote octal and binary number representations of the primitive polynomials. In this paper, three different stages of LFSR are implemented by Cadence simulator using 90 nm CMOS technology. As shown in Table 1, different number of feedback taps can be used to build the feedback operation of the generator. However, in spread spectrum systems, the number of feedback connections of LFSR can vary from one system to another based on the application requirements. In this work, we have assumed that the transceiver is dedicated for a single-user operation in contrast to the major aim of many applications that use spread spectrum technique for multiple users. Therefore, no need for long codes with high degree polynomial as the chance of interfering between users is nonexistent. According to that, two feedback taps are used as only one intermediate delay is utilized to build the feedback operation. In addition, a small number of feedback paths is highly desirable to restrict the power consumption and the cell size. As well as, adding more paths means more traces to implement in hardware which in turn leads in limiting the maximum frequency.

4.1. Flip-flop CMOS design

In VLSI systems, FFs might dissipate a power up to 60% of the total circuit power dissipation [17]. Therefore, an efficient FF design may significantly enhance the circuit power consumption. In literature, various circuits of D-FFs are proposed and investigated for low power application, each of which has its own pros and cons [18–22]. For comparison purposes, a performance analysis is carried out on several FF designs and presented in Tables 2–4. For precise results, all designs are simulated under the same conditions and tested within the sub-threshold voltage region. Because this work is intended to be used in biomedical applications, so all FF designs are tested at a frequency of 403 MHz. Power dissipation results shown in Table 2 reveal that the transmission gate-based FF (TGFF) has the lowest power consumption at all scaled voltages whereas some designs fail to operate below 0.5 V.

The propagation delay of each FF is illustrated in Table 3 and captured at each voltage within the sub-threshold region. It is worth noting here that the delay of the DPTDFF design is slightly lower than the TGFF. However, the DPTDFF consumes more power comparing to TGFF.

Optimal D-FF designs must achieve a trade-off between the power consumption, the number of transistors (circuit size) and the perfor-

Table 2
Power dissipation of various FF designs at sub-threshold voltages.

Design name	Power consumption (nW) at			
	0.3 V	0.4 V	0.5 V	0.6 V
TGFF	20	34	57	86
DETFF [18]	25	41	64	93
DPTDFF [21]	119	210	323	456
LPDFF [22]	Failed	30	48	71
Push-pull DFF [22]	Failed	Failed	104	150
TSPC [18]	Failed at the required frequency			
CPEPTFF [22]	Failed at the required frequency			

Table 3
Propagation delay of various FF designs at sub-threshold voltages.

Design name	Propagation delay (ns) at			
	0.3 V	0.4 V	0.5 V	0.6 V
TGFF	0.6	0.2	0.08	0.03
DETFF	0.7	0.35	0.15	0.04
DPTDFF	0.4	0.1	0.05	0.02
LPDFF	Failed	1.5	1.5	1.3
Push-pull DFF	Failed	Failed	1.4	1.34
TSPC	Failed at the required frequency			
CPEPTFF	Failed at the required frequency			

Table 4
Power delay product of various FF designs.

Design name	PDP (10^{-18} J)				No. of transistor
	0.3 V	0.4 V	0.5 V	0.6 V	
TGFF	12	6.8	4.56	2.58	16
DETFF	17.5	8.2	9.6	3.72	20
DPTDFF	47.6	21	16.15	9.12	16+4 cap
LPDFF	Failed	45	72	92.3	16
Push-pull DFF	Failed	Failed	145.6	201	16
TSPC	Failed at the required frequency				7
CPEPTFF	Failed at the required frequency				19

mance (delay) at ultra-low voltage supply. Therefore, the power delay product (PDP) based metric is used for comparative analysis and in particular for low power systems.

The PDP computations results shown in Table 4 indicate that TGFF has highest figure of merit as it has the lowest PDP among other FF designs. Consequently, a positive edge-triggered TGFF is utilized to construct the shift register. The suggested FF consists of two latches that are connected in cascade.

The schematic diagram of the modified transmission gate (TG)-based D-FF is shown in Fig. 4. The suggested design is based on conventional TG FF with major additions to the basic structure. Two more inputs PRESET and CLEAR are added to the conventional circuit as these inputs are needed to load each FF in the m -sequence generator with an initial bit (seed bit).

The PRESET input is used to get high voltage on the output Q regardless of the value of the input D , and it can be activated by a logic 0. Moreover, the CLEAR input is used to get a low voltage on the output Q regardless of the value of the input D , and can also activated by a logic 0. To demonstrate the effect of PRESET and CLEAR on the output waveform, the transient response of the modified FF is illustrated in Fig. 5. The results were obtained via simulation carried out in Cadence at a clock frequency of 200 MHz and a VDD voltage of 500 mV.

Conserving chip area while operating the circuit at ultra-low supply voltage is achieved by appropriately dimensioning the transistors using

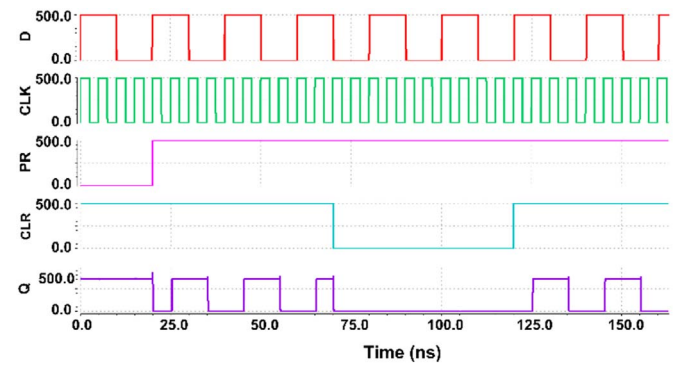


Fig. 5. Transient response of the modified FF, the magnitude of all waveforms is in (mV).

matching conditions. To this end, the same channel length is selected for all transistors, so that matching can be achieved by designing the width of the pMOS transistor to be two to four times the width of the nMOS transistor. Furthermore, the minimum width of the later is one and a half times the size of the channel length [23]. Matching the transistors leads to improved dynamic performance of the circuit since the low-to-high, (t_{PLH}), and high-to-low, (t_{PHL}), propagation delays are equalized. The numerical values next to the transistors shown in Fig. 4 represent the optimized channel width of each transistor.

4.2. Exclusive-OR CMOS design

Two input XOR gates are required to perform the feedback operation of the m -sequence generator. In this paper, different designs of XOR circuits are compared and evaluated in terms of propagation delay and power consumption [24–27]. In Fig. 6(a), a pass transistor logic style is characterized by its low power consumption at low supply voltages, however, it produces a very poor output for some input combinations. A static inverter has been used in another design presented in Fig. 6(b). Although the existence of a static inverter results in a good driving capability, the output waveform exhibits a poor logic 1 when the input pattern changes to 01, and a large delay when the input pattern is 00. Fig. 6(c) shows a TG-based design that surpasses other designs in terms of low power consumption and good delay characteristics over all supply voltages, however, due to the use of an inverter, it requires larger circuit area. In Fig. 6(d), a design using 8 transistors is shown with a good output level at low voltages, however, the output deteriorates at higher voltages. In addition, it consumes more power than the other designs due to the availability of two static inverters.

To overcome the problem of poor output level, a design of 6 transistors and good output level with driving capability is proposed in [26] and shown in Fig. 6(e), however, it is not efficient in terms of power and delay specifically at low voltages. Another design of 4 transistors based on pass style is presented in [27] and shown in

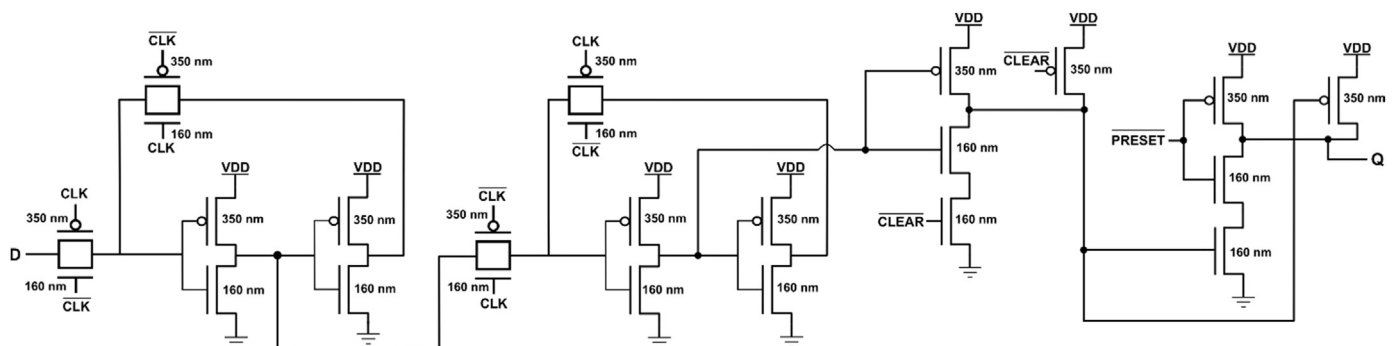


Fig. 4. Modified TG-based D-FF with PRESET and CLEAR.

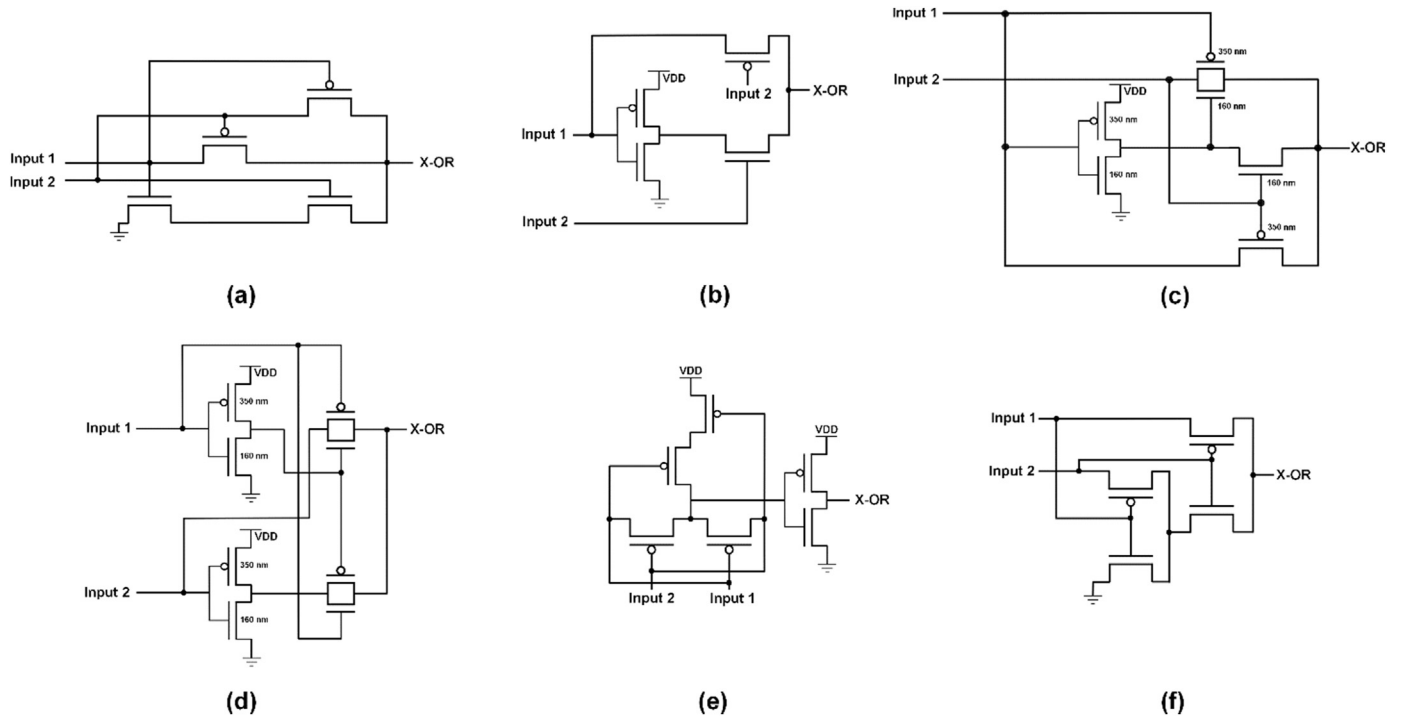


Fig. 6. Power consumption of different XOR designs.

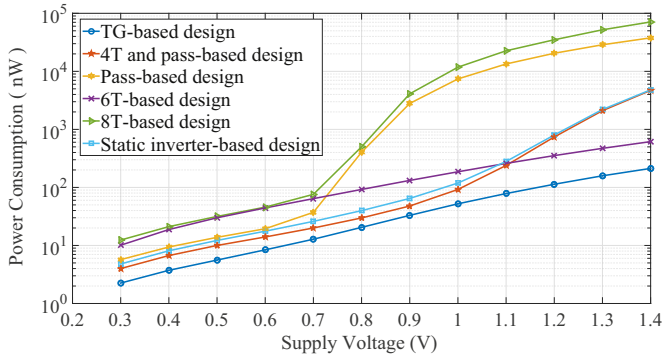


Fig. 7. Different XOR designs.

Fig. 6(f), which is an efficient design in terms of power, nonetheless, it suffers from the same problem of poor delay characteristics due to its limited driving capability. The power consumption of each design shown in Fig. 6 is computed by Cadence simulator and a comparison between them is illustrated in Fig. 7, where we can clearly see that the TG-based design shown in Fig. 6(c) is consuming significantly less power than other designs for varying supply voltages. Furthermore, as Fig. 7 shows, when the supply voltage is between 0.3 and 0.7 V, the power consumption increases linearly with the supplied voltage for all the different designs. However, as the supplied voltage goes beyond 0.7 V, only the TG-based and 6T-based designs maintain this linearity, while the remaining designs fail to do so. Since the TG-based design requires the least amount of power consumption, it has chosen to be included in our work as a feedback function for the m -sequence generator.

4.3. Architecture of 7-bit m -sequence generator

To generate a 7-bit m -sequence code, a 3-stage of LFSR are used as shown in Fig. 8 [28]. According to the feedback polynomial described in (2), the activated feedback taps are c_1 , and c_3 . The phase of the generated code depends on the initial seed of the LFSR. The seed value can be determined using PRESET and CLEAR, where both of them can

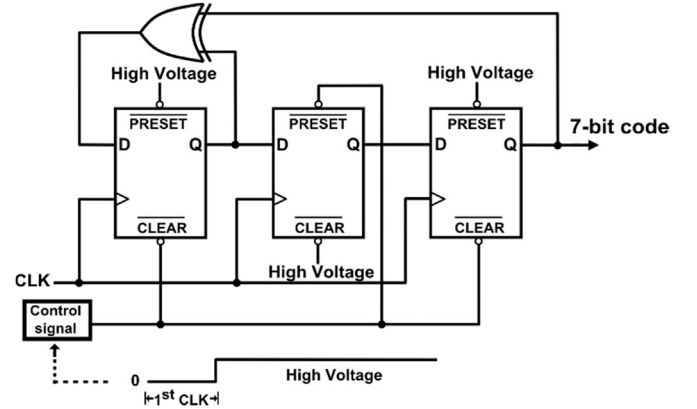


Fig. 8. 7-bit m -sequence code generator producing the code 1001110.

be activated with low voltage. Control and high voltage signals are used to activate or deactivate the PRESET and CLEAR of each FF. The control signal is used to activate the PRESET and CLEAR, and to load the FF with a logic 1 or 0, respectively. The control signal consists of two states; the low voltage state is used for one clock period for activation purposes, while the high voltage state is utilized for deactivation.

Fig. 8 illustrates how to load the FFs with a seed of 010. The control signal needs to be connected to CLEAR of the first and third FF, and to the PRESET of the second FF to generate the code 1001110.

In Fig. 8, the modular design approach is used which requires the FF to have identical circuits. More importantly, when the code changes, the initial conditions of the FFs must be changed, and therefore, all the FFs need both PRESET and CLEAR terminals. This can be achieved by changing the connections to all the FFs from hard wire to a programmable structure. i.e., the hard wires in Fig. 8 are for illustration only.

For analysis purposes, further code generators are required to determine the effect of the switching frequency and supply voltage on the power consumption of the circuit. Therefore, two more m -sequence generators of 31 and 511-bit code lengths are implemented to assess the reliability of the codes produced as a function of the aforementioned

tioned constraints.

5. Simulation and results

5.1. Auto-correlation

The property of auto-correlation of an m -sequence code is one of the reliable methods to assess the quality of our generators. The sample auto-correlation function of a discrete sequence $x(n)$ is mathematically defined as

$$R(\tau) = \sum_{n=0}^{L-1} x(n)x(n+\tau), \tau = \pm 1, \pm 2, \dots \quad (5)$$

The auto-correlation values for distinct correlations lags are presented as follows

$$R(\tau) = \begin{cases} L, & \text{when } \tau = 0 \\ -1, & \text{when } \tau \neq 0 \end{cases} \quad (6)$$

The resulted auto-correlation has an impulse shape with a peak amplitude proportional to the code length L at Zero lag. We successfully tested the output of the three designed generators at different voltages and frequencies. However, we only present the output result of the 9-stage code generator. Fig. 9 (top) shows a single period of the 511-bit code generated at a clock speed of 130 MHz using a supply voltage of 0.3 V. Although the used clock speed was the maximum frequency that achieved when the supply voltage is 0.3 V, the output sequence still retains its characteristics within the sub-threshold region. The sample auto correlation of the complete 511-bit code is shown in Fig. 9 (bottom) demonstrating the reliable detection of the generated code.

5.2. Eye diagram

Further analysis using the eye diagram is introduced to assess the quality of the output sequence. The results of eye diagrams did not show any significant noise in all produced codes of each generator. The output eye diagrams depicted in Fig. 10 are extracted from the 511-bit code and measured at 0.3 V using the Cadence simulator and reveal a narrowing of the eye openings at high frequencies. However, the eye opening still permits the detector to distinguish clearly between logic 1's and 0's at ultra-low voltages and high frequencies.

One unanticipated finding is the asymmetry in the eye opening as the crossing point is marginally closer to the logic 1 voltage. The asymmetry problem is due to amplitude distortion as shown in Fig. 9 (top), where the logic 1 pulse duration is longer than its logic 0 equivalent.

5.3. Power consumption and frequency analysis at 90 nm

In order to validate the performance of the design, three m -sequence code generators, i.e. for 7, 31 and 511 bit codes, are analyzed

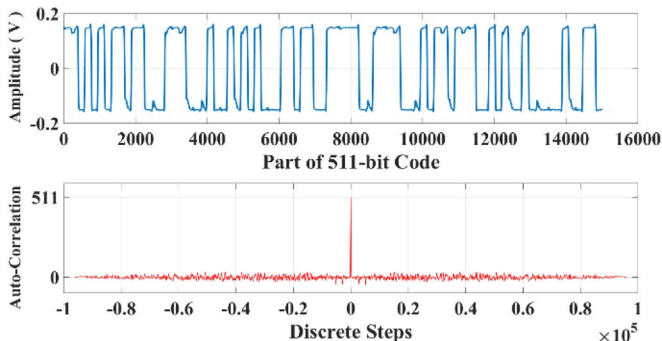


Fig. 9. 511-bit m -sequence code and its auto-correlation function.

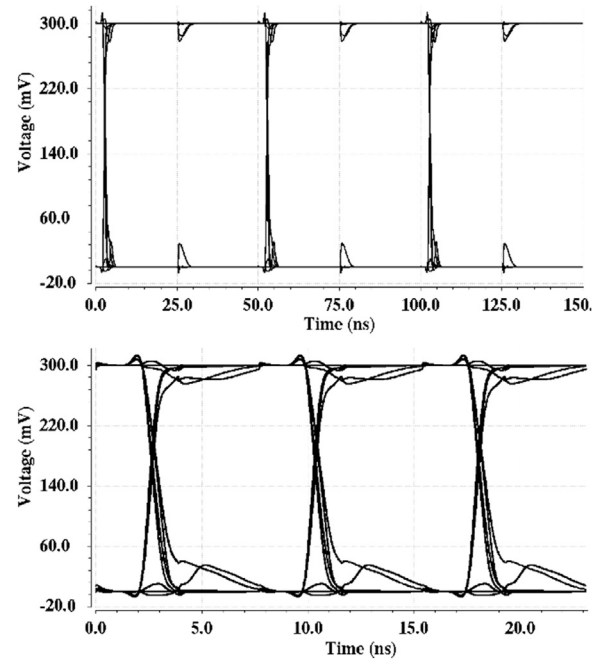


Fig. 10. The top eye diagram is measured at 20 MHz whereas the bottom eye is measured at 130 MHz.

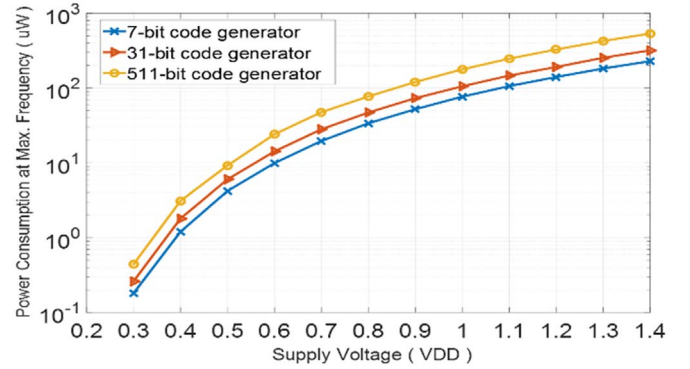


Fig. 11. Variation of power consumption with VDD for three m -sequence code generators.

and compared using Cadence IC simulator. The simulation is carried out using 90 nm CMOS technology. For comparison purposes, a unified transistor size is utilized for all FFs and XOR gate in each generator. In Fig. 11, the average power consumption P_{avg} of the three code generators is measured at the maximum achievable code frequency and for different supply voltages. The measured power consumption includes the static and dynamic powers, denote as P_s and P_d , respectively, defined as [23]

$$P_{avg} = P_d + P_s, \quad (7)$$

where P_s refers to the consumed power in the absence of transistor switching and depends on V_{dd} and leakage current $I_{leakage}$, i.e.

$$P_s = I_{leakage} V_{dd}, \quad (8)$$

where $I_{leakage}$ is attributed to the parasitic elements of the CMOS transistors. From Fig. 11, it is obvious that the code generators show an increasing power consumption with the increase of supply voltage and code length. This is attributed to the fact that the dynamic power consumption P_d of CMOS digital circuits depends quadratically on the supply voltage V_{dd} , and linearly on the capacitance load C_L and switching frequency f , that is

$$P_d = f C_L V_{dd}^2. \quad (9)$$

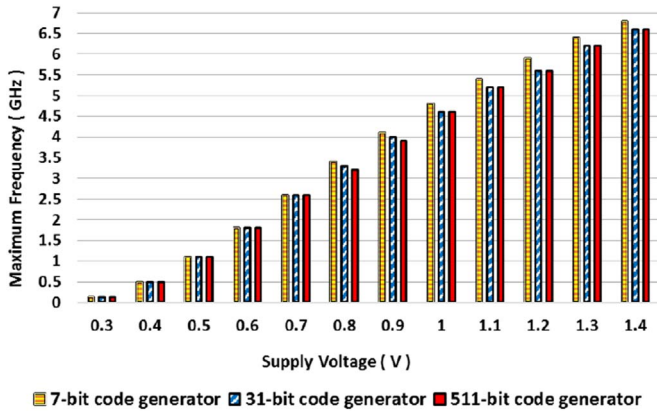


Fig. 12. Maximum achievable frequency of three m -sequence code generators implemented by 90 nm technology.

Therefore, optimizing the voltage level can significantly mitigate the power consumption of CMOS circuit.

Further analysis is performed by measuring the maximum frequency of each code generator, where the circuit can produce the output sequence without any flipped sign chips. It is interesting to note that the maximum obtained frequencies, shown in Fig. 12, for the three generators have the same values as the supply voltage in the range between 0.3 and 0.7 V. However, the 7-bit code generator exhibits higher switching frequency over the other code generators at a supply voltage ≥ 0.8 V due to lower number of FFs required, which in turn enables faster operation at the same power supply voltage level.

The code generators will be used in conjunction with spread spectrum-based BSNs, so it is profoundly advantageous to investigate the effect of generators heat out, produced from the consumed power, on the human body. The temperature difference ΔT between the code generator and the human body is computed using the relationship of heat flow [29], that is,

$$\Delta T = \frac{Q \times L}{K \times A}, \quad (10)$$

where ΔT is calculated as a function of the power $Q(W)$ consumed by the code generator at maximum achievable frequency, the distance $L(m)$ between the code generator device and the human body, the physical dimensions of the device $A(m^2)$ and the thermal conductivity $K(W/m^\circ C)$ of water in $37^\circ C$. In our calculations, $K = 0.629$ and we assumed that the dimensions of the generator is 0.5 cm^2 and the distance $L = 1 \text{ cm}$.

Fig. 13 shows that increasing the supply voltage from 0.3 to 1.4 V for the three code generators is safe for the human health as it does not exceed the temperature raising limit of $1^\circ C$ recommended by International Commission on Non-Ionizing Radiation Protection (ICNIRP) [30].

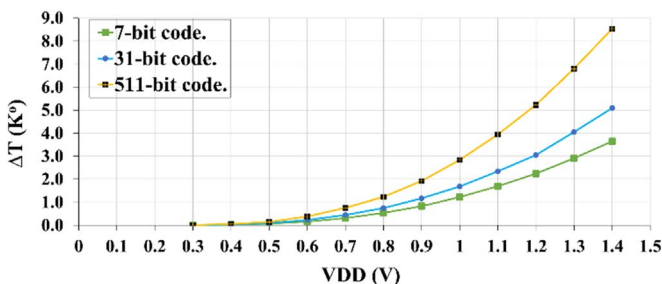


Fig. 13. The effect of using different code lengths on ΔT over a range of VDD values.

6. Scaling implication on power consumption

The operating of CMOS devices in the region of sub-threshold voltage is conducted to be an effective way to reduce the dissipated power while maintaining good performance. Furthermore, CMOS technology scaling exhibits a favorable impact on digital circuits in term of lower power consumption, boosting of operating frequency as well as geometric reduction [8]. In this research, as the m -sequence code generator is used to design the transceiver for monitoring human health and will be placed in/on the human body, so scaling the technology node from 90 nm to 65 nm will be beneficial for this purpose and will enhance the performance of our digital circuit.

6.1. Power consumption and operating frequency at 65 nm

One of the solutions to minimize the total power consumption, in addition to lowering the supply voltage, is by scaling the technology node. In this research, the technology node is scaled from 90 to 65 nm, and the three m -sequence code generators for code lengths of 7, 31 and 511 bits are re-implemented by Cadence IC simulator using 65 nm technology. Moreover, the 90 nm circuit design is reused to evaluate the 65 nm node in addition to the modified TG-based FF and TG-based XOR circuit. The total power consumption and maximum operating frequency are studied within a supply voltage range from 0.3 V to 1.4 V.

Using transistors of low threshold voltage to carry out the code generator efficiently at very low supply voltages is important especially with the associated increase in the leakage current due to technology scaling. The measurements (see Figs. 14–16) show that a tradeoff can be achieved between the maximum frequency, at each VDD, and its corresponding power consumption. These measurements are obtained by carrying out the simulation of the schematic view without taking parasitic effects into account.

For the 7-bit code generator, the maximum achievable frequency is measured along the variation of VDD from 0.3 to 1.4 V. In Fig. 14, the results demonstrate the ability of the generator to produce a robust and reliable code at the sub-threshold region of 0.3, 0.4 and 0.5 VDD with capability of high operating frequency reach to 130, 500 and 1200 MHz, respectively. According to Eq. (7), the power consumption is measured at the maximum achievable code frequency and for different supply voltage.

To verify the reliability of the circuit design at 65 nm technology, two more m -sequence code generators are built to produce two different lengths of 31 and 511-bit codes.

For 31-bit code generator, it is the same circuit design of FF and XOR used to generate the 7-bit code except that two more FFs are added to generate the 31-bit code. Fig. 15 shows the amount of consumed power to produce the 31-bit code at maximum operating frequency at different supply voltages. It can be inferred that the code generated efficiently within the sub-threshold region without compro-

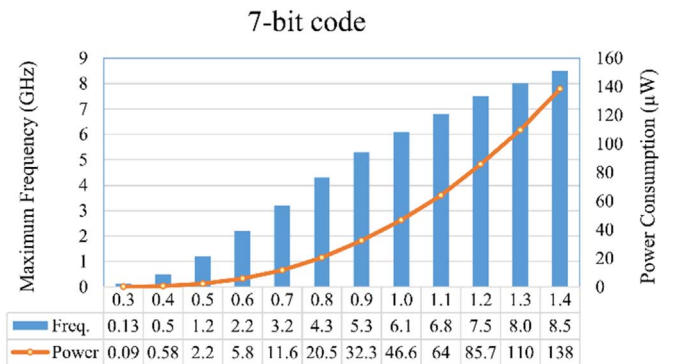


Fig. 14. Variation of achievable frequency and corresponding power consumption with VDD.

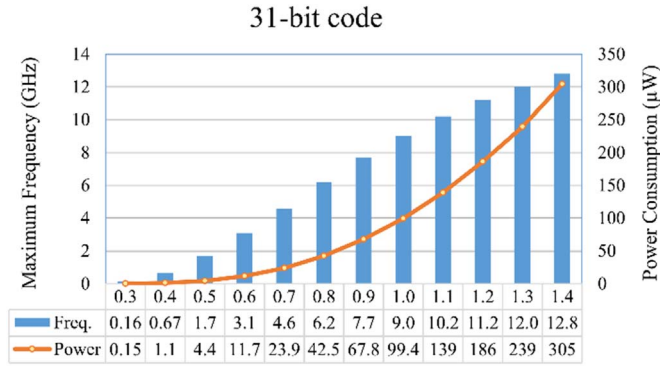


Fig. 15. Maximum achievable frequency and corresponding power consumption with regards to VDD.

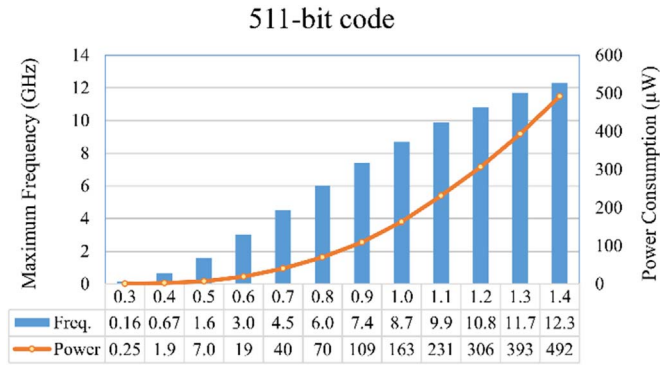


Fig. 16. Achievable frequency at each VDD and corresponding power consumption for 511-bit generator.

mizing the functionality of the circuit even at maximum operating frequency.

Further analysis is carried out for the 511-bit code generator and depicted in Fig. 16. From that figure, it is clearly shown that scaling down the supply voltage leads to clocking frequency reduction. Nevertheless, a considerable frequency is achieved at sub-threshold region as it approaches 160, 670 and 1600 MHz at 0.3, 0.4 and 0.5 VDD, respectively. Comparing to 31-bit generator, additional power is consumed to generate the 511-bit code although both of them have about the same maximum achievable frequency. Owing to Eq. (9), this extra consumption is attributed to the high capacitance load as four additional FFs are added to generate 511-bit code.

6.2. Comparison of measurements made on 65 and 90 nm technology

After conducting robust analysis on different lengths of m -sequence code using two different technologies, i.e. 65 and 90 nm, a comparison between them is made and depicted in Table 5. From that table, it can be seen that a significant power saving is achieved while using 65 nm for the three different code lengths. Furthermore, higher operating frequency is observed when using the 65 nm technology too.

Table 5 reveals that the consumed power to generate a code using the 65 nm technology is approximately 50% of the consumed power to generate the same code at the same frequency in 90 nm technology. Fig. 17 illustrates that the ratio of reducing the power consumption while using the 65 nm technology is ranging from 45% to 55% for the three different code lengths and along the variation of operating frequency.

Based on its efficiency compared to the 90 nm implementation, the layout of the 65 nm technology is selected in this research to be implemented on the code generator for the purpose of design verification.

6.3. Layout design and verification of 65 nm technology

The layout stage is an implementation the circuit in the schematic that is used for fabrication purposes. The layout of the three code generators, 7, 31 and 511-bit code are drawn and implemented by Cadence Virtuoso 6.1.6 with a 65 nm CMOS technology. A low threshold voltage transistor, namely, SPLVT is used in designing of the FF and XOR circuits, which is sized properly to compensate the leakage current to get low power dissipation and high performance. Furthermore, the same channel length of 65 nm is applied for all transistors and the width of all nMOS and pMOS transistors is optimized to be 130 and 260 nm, respectively.

Physical verification is one of the common procedures to validate the layout of the implemented circuit and to ensure that the implementation is functional and manufacturable. Design rule checking (DRC) is the first stage of verification to guarantee that the layout is manufacturable. The second stage uses layout vs schematic (LVS) tool to match the layout with the schematic by extracting all devices and connectivity from the layout to create netlist to compare with the schematic. To ensure accuracy and pragmatic results, the final stage is completed by extracting all parasitic elements using the parasitic extraction (PEX) tool to calculate the parasitic resistances, capacitances and inductances resulting from the layout to be included in the measurements. All the physical verification stages are executed by Calibre skill interface.

The layout of the TG-based FF and XOR circuits are shown in Figs. 18 and 19, respectively. After building the layout with a successful passing of all physical verification stages, the parasitic elements are extracted to examine its impact on the circuit behavior in term of power consumption and maximum achievable frequency. In order to assess the effect of parasitics and for more accuracy, repeated measurements are used on the three different lengths of code generators.

It is observed that the performance of the produced code from the layout execution is high in all three code generators. Figs. 20–22 demonstrate the results obtained from the simulation of the schematic and layout designs demonstrating the impact of parasitics on the maximum operating frequency by testing the 7-bit (respectively 31-bit and 511-bit) code generator at various voltages and recording the achievable frequency.

A comparison of the two results reveal the effect of the parasitic elements on the frequency behavior as the maximum achievable frequency executed by the layout is lower than for schematic. However, the layout achieved frequencies at sub-threshold region is still sufficient and high enough for our application.

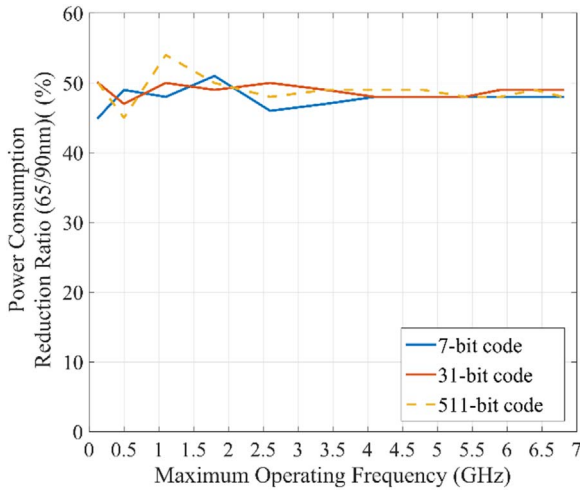
7. Conclusion

The need for reducing the power consumption necessitates the designers to scale the supply voltage down to the sub-threshold region. In this research, a design of low power m -sequence code generator was proposed using a modified TG-based FF. We demonstrated that the proposed generator design produces a code with high performance within the region of sub-threshold voltage. Three generators of different code lengths were implemented and their performance was assessed at a transistor level. The circuit of the code generator was simulated by Cadence and implemented using 90 nm CMOS technology. The power consumption analysis of the proposed design demonstrated the significant implications for the understanding of how to achieve a critical balance between the power consumption and the code length. Furthermore, the output of each code generator was evaluated using the auto-correlation and eye diagram metrics to demonstrate the quality and reliability of the code. It was shown that all three generators can achieve approximately the same maximum allowable switching frequency within a supply voltage region between 0.3 V and 0.7 V. Thus, a balance must be achieved between the power consumption and the length of the generated code. The preference of one code

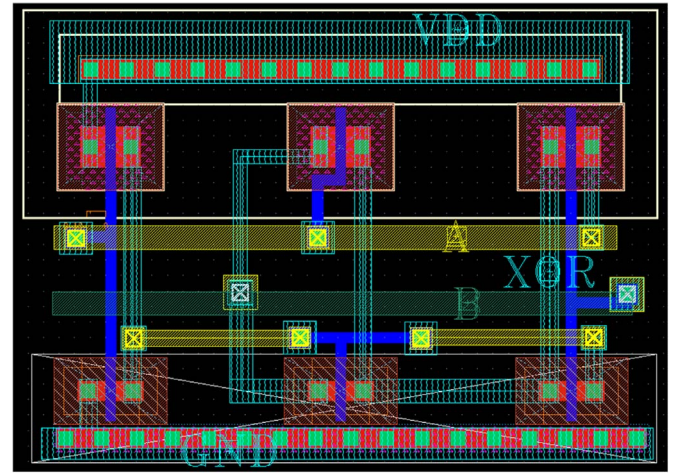
Table 5

Comparison of 65 and 90 nm technology in term of maximum operating frequency and power consumption.

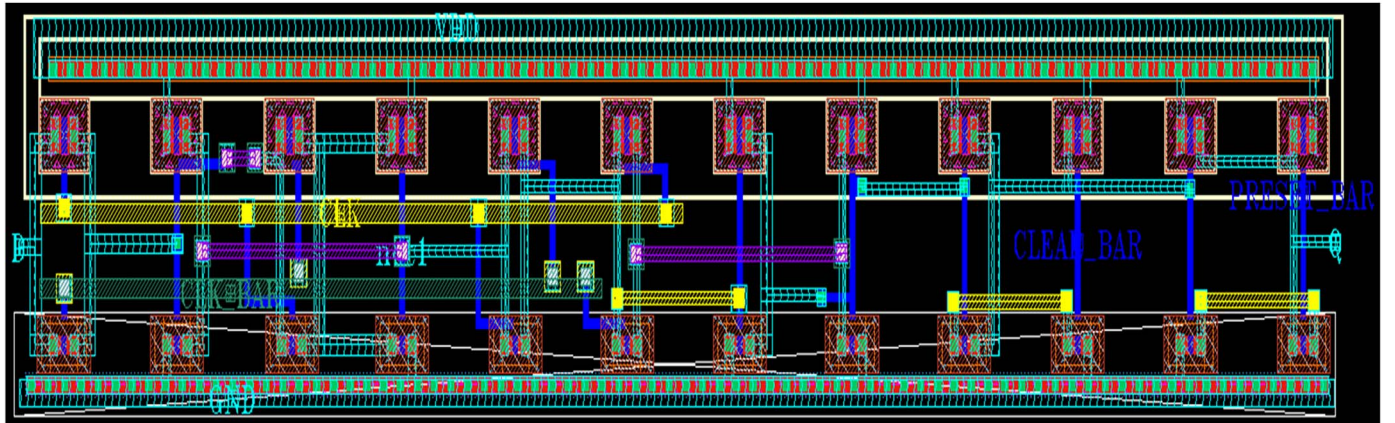
VDD	7-bit code				31-bit code				511-bit code			
	65 nm		90 nm		65 nm		90 nm		65 nm		90 nm	
	f GHz	P_{av} μ W	f GHz	P_{av} μ W	f GHz	P_{av} μ W	f GHz	P_{av} μ W	f GHz	P_{av} μ W	f GHz	P_{av} μ W
0.3	0.13	0.09	0.13	0.2	0.16	0.15	0.13	0.26	0.16	0.25	0.13	0.44
0.4	0.5	0.58	0.5	1.2	0.67	1.1	0.5	1.8	0.67	1.9	0.5	3.1
0.5	1.2	2.2	1.1	4.2	1.7	4.4	1.1	6.0	1.6	7.0	1.1	9.2
0.6	2.2	5.8	1.8	9.9	3.1	11.7	1.8	14.2	3.0	19	1.8	24.1
0.7	3.2	11.6	2.6	19.6	4.6	23.9	2.6	28.1	4.5	40	2.6	47.6
0.8	4.3	20.5	3.4	33.8	6.2	42.5	3.3	47.1	6.0	70	3.2	77.3
0.9	5.3	32.3	4.1	52.2	7.7	67.8	4.0	73.3	7.4	109	3.9	120.8
1.0	6.1	46.6	4.8	76.8	9.0	99.4	4.6	105.7	8.7	163	4.6	178.5
1.1	6.8	64	5.4	106.5	10.2	139	5.2	147.2	9.9	231	5.2	248
1.2	7.5	85.7	5.9	140.8	11.2	186	5.6	191.7	10.8	306	5.6	329
1.3	8.0	109.7	6.4	183	12.0	239	6.2	254.8	11.7	393	6.2	427.7
1.4	8.5	138.4	6.8	229.4	12.8	304.5	6.6	320.3	12.3	492	6.6	537

**Fig. 17.** Ratio of power consumption reduction in 65 nm.

generator over another is adhered to the detection efficacy, error rate, power consumption and immunity to channel changes. The longest the code generator leads to highest detection rate, power consumption and immunity to channel changes achieving thus the lowest chip error rate. For ultra-low power transceivers, a supply voltage of 0.3, 0.4, and 0.5 V can be used as the maximum achieved frequency at these low voltages is 130 MHz, 500 MHz, and 1.1 GHz, respectively. In addition to voltage reduction, a further method of power saving was achieved in this research by scaling the technology node from 90 to 65 nm. We

**Fig. 19.** Layout of TG-based XOR.

validated the design by comparing both technologies and evaluating the performance in term of power consumption and maximum achievable frequency. It was shown that utilizing the 65 nm boosted the operating frequency and reduced the power consumption of about 45–55% compared to the 90 nm technology. Consequently, the layout was implemented using the 65 nm technology and the results revealed the ability of generating the m -sequence code within the sub-threshold region. The maximum clocking frequency was determined by considering the parasitic elements of the layout.

**Fig. 18.** Layout of TG-based FF.

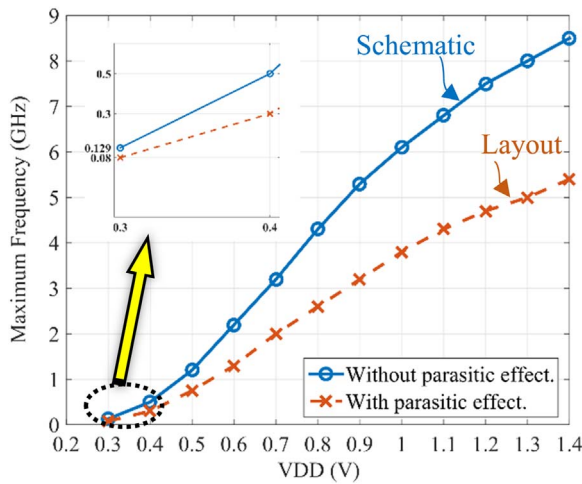


Fig. 20. Effect of parasitics on the maximum operating frequency of a 7-bit code.

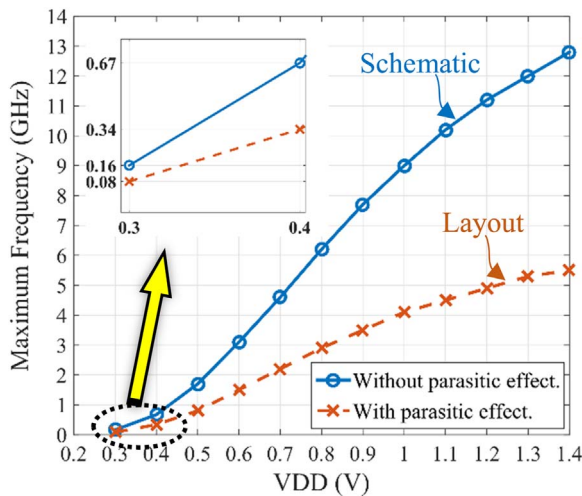


Fig. 21. Effect of parasitic elements on the maximum operating frequency of a 31-bit code.

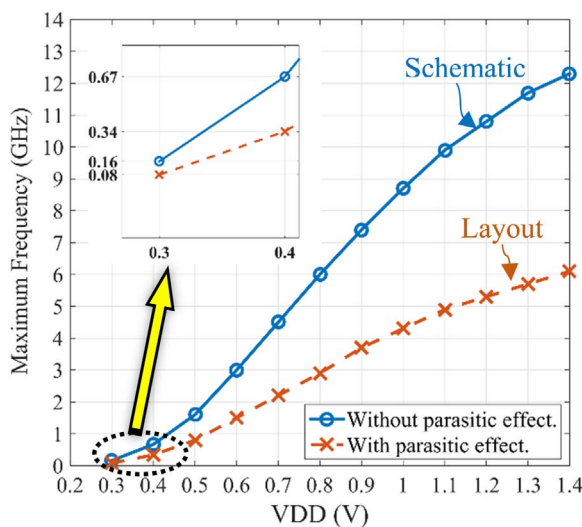


Fig. 22. Effect of parasitic elements on the maximum operating frequency of a 511-bit code.

References

- [1] Q. Zhang, P. Feng, Z. Geng, X. Yan, N. Wu, A 2.4-GHz energy-efficient transmitter for wireless medical applications, *IEEE Trans. Biomed. Circuits Syst.* 5 (2011) 39–47.
- [2] S. Kim, R. Vyas, J. Bito, K. Niotaki, A. Collado, A. Georgiadis, M.M. Tentzeris, Ambient RF energy-harvesting technologies for self-sustainable standalone wireless sensor platforms, *Proc. IEEE* 102 (2014) 1649–1666.
- [3] R.E. Ziener, Fundamentals of spread spectrum modulation, *Synth. Lect. Commun.* 2 (2007) 1–79.
- [4] H. Alrudainy, A. Mokhov, A. Yakovlev, A scalable physical model for nano-electro-mechanical relays, in: *Power and Timing Modeling, Optimization and Simulation (PATMOS)*, 2014 24th International Workshop on, 2014, pp. 1–7.
- [5] C. Chen, M. Sarrafzadeh, Simultaneous voltage scaling and gate sizing for low-power design, *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.* 49 (2002) 400–408.
- [6] R. Vaddi, S. Dasgupta, R. Agarwal, Device and circuit co-design robustness studies in the subthreshold logic for ultralow-power applications for 32 nm CMOS, *IEEE Trans. Electron. Devices* 57 (2010) 654–664.
- [7] H. Ni, J. Hu, Near-threshold sequential circuits using improved clocked adiabatic logic in 45 nm CMOS processes, in: *Proceedings of the 2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, IEEE, 2011, pp. 1–4.
- [8] S. Henzler, *Power Management of Digital Circuits in Deep Sub-micron CMOS Technologies* 25, Springer Science & Business Media, 2006.
- [9] S. Brueckner, K. Schubert, J. Fahlbusch, J. Schoebel, Generation of wideband m-sequences: a low-cost approach, in: *Proceedings of the 2014 IEEE International Conference on Ultra-WideBand (ICUWB)*, 2014.
- [10] V.P. Ipatov, *Spread Spectrum and CDMA: Principles and Applications*, John Wiley & Sons, 2005.
- [11] T.F. Wong, *Spread spectrum & CDMA, Multi-user Detect.* (2001).
- [12] M.-L. Wu, K.-A. Wen, C.-W. Haung, Efficient pseudonoise code design for spread spectrum wireless communication systems, *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.* 48 (2001) 606–613.
- [13] A. Ba, M. Vidjokovic, K. Kanda, N.F. Kiyani, M. Lont, X. Huang, X. Wang, C. Zhou, Y.-H. Liu, M. Ding, A 0.33 nJ/bit IEEE802.15.6/proprietary mics/ism wireless transceiver with scalable data rate for medical implantable applications, *IEEE J. Biomed. Health Inform.* 19 (2015) 920–929.
- [14] H.W. Pflug, H.J. Visser, N.F. Kiyani, G. Dolmans, K. Philips, K. Kanda, M. Hamaminato, S. Masui, Radio channel characterization for 400 MHz implanted devices, in: *Proceedings of the Wireless Communications and Networking Conference (WCNC)*, 2014 IEEE, 2014, pp. 293–298.
- [15] A. Goldsmith, *Wireless Communications*, Cambridge university press, 2005.
- [16] R.N. Mutagi, Pseudo noise sequences for engineers, *Electron. Commun. Eng. J.* 8 (1996) 79–87.
- [17] P. Zhao, J. McNeely, W. Kuang, N. Wang, Z. Wang, Design of sequential elements for low power clocking system, *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* 19 (2011) 914–918.
- [18] S. Naik, R. Chandel, Design of a low power flip-flop using CMOS deep sub micron technology, in: *Recent Trends in Information, Telecommunication and Computing (ITC)*, 2010 International Conference on, IEEE, 2010, pp. 253–256.
- [19] I.A. Khan, D. Shaikh, M.T. Beg, 2 GHz low power double edge triggered flip-flop in 65 nm CMOS technology, in: *Signal Processing, Computing and Control (ISPC)*, 2012 IEEE International Conference on, 2012, pp. 1–5.
- [20] Y. Berg, High speed ultra low-voltage differential D flip-flop for low-voltage CMOS design, in: *Faible Tension Faible Consommation (FTFC)*, 2013 IEEE, 2013, pp. 1–4.
- [21] U. Ko, P.T. Balsara, High-performance energy-efficient D-flip-flop circuits, *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* 8 (2000) 94–98.
- [22] G.M. Rao, S. Rajendar, Design of low power pulsed flip-flop using sleep transistor scheme, in: *Advances in Electrical Engineering (ICAEE)*, 2013 International Conference on, IEEE, 2013, pp. 335–340.
- [23] A.S. Sedra, K.C. Smith, *Microelectronic Circuit*, Fifth edition, Oxford university press, New York, 2004.
- [24] J.-M. Wang, S.-C. Fang, W.-S. Feng, New efficient designs for XOR and XNOR functions on the transistor level, *IEEE J. Solid-State Circuits* 29 (1994) 780–786.
- [25] A.M. Shams, T.K. Darwish, M.A. Bayoumi, Performance analysis of low-power 1-bit CMOS full adder cells, *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* 10 (2002) 20–29.
- [26] C.-H. Chang, J. Gu, M. Zhang, Ultra low-voltage low-power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits, *IEEE Trans. Circuits Syst. I: Regul. Papers*, 51 (2004) 1985–1997.
- [27] H.T. Bui, A.K. Al-Sheraidah, Y. Wang, New 4-transistor XOR and XNOR designs, in: *ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE Asia Pacific Conference on, IEEE, 2000*, pp. 25–28.
- [28] A.N. Abdulfattah, C.C. Tsimenidis, A. Yakovlev, Subthreshold-based m-sequence code generator for ultra low-power body sensor nodes, in: *Power and Timing Modeling, Optimization and Simulation (PATMOS)*, 2016 26th International Workshop on, IEEE, 2016.
- [29] R.G.C. Artus, Measurements of the novel thermal conduction of a porphyrinic heat sink paste, *IEEE Trans. Compon. Packag. Manuf. Technol.: Part B* 19 (1996) 601–604.
- [30] I. Guideline, Guidelines for limiting exposure to time-varying electric, magnetic, and electromagnetic fields (up to 300 GHz), *Health Phys.* 74 (1998) 494–522.