# A Functional Block Decomposition Method for Automatic Op-Amp Design

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## Abstract

This paper presents a method to decompose an op-amp into its functional blocks. The method is able to recognize functional blocks on a high level of abstraction as loads or amplification stages which have a large set of possible structural implementations. The paper presents a hierarchical library of functional blocks. With every hierarchy level, the structural representation of the functional blocks becomes more variable while its function emerges. We use the hierarchical order to automatically compute the functional decomposition of an op-amp given as a flat netlist. Experimental results illustrate the method. The functional block decomposition enables a comprehensive formalization of design knowledge for computer-aided design of op-amps. Applications to circuit sizing and structural synthesis of op-amps are presented.

*Keywords:* Analog design automation, CMOS, operational amplifiers, structure analysis

## 1. Introduction

Operational amplifiers are the fundamental building blocks of analog/mixedsignal circuits. They mean to analog design, as some say, what inverters mean

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to digital design. While inverters and the complete library of cells for digi-

- tal circuits are designed almost fully automatically, op-amps are still designed mostly manual till now. This work presents a new approach to the old, but yet unsolved problem of a complete structural and functional representation of opamps. As confirmed in [1], op-amp stage recognition is a hard task. To tackle this problem, a new hierarchical representation of functional blocks in op-amps
- <sup>10</sup> is developed in this paper. The method achieves a complete recognition of all stages in an op-amp, their loads, transconductances and biases. The formalized computer-oriented description of the op-amp structure allows a development of new approaches on major parts on analog design automation (e.g., sizing [2], structural synthesis [3]).
- Many types of structural libraries were invented to automate the analog design process. They consist of whole topologies of basic analog circuits [4, 5, 6], predefined modules of, e.g., amplification stages or bias circuits having a certain transistor structure [7], or basic building blocks being either single devices with additional self connections as in [8, 9] or transistor structures as, e.g., current
  mirrors, differential pairs [10, 11, 12, 13]. The libraries were developed for
- different purposes. Some are used for topology synthesis [5, 8, 9, 12, 13, 6]. Other were developed to generate constraints for sizing and layout [11] or to synthesize layouts [7].
- The libraries come with disadvantages. As there exist thousands of topology variants for op-amps, libraries containing structural defined topologies or modules as in [4, 5, 7, 6] do not support all variants. Adding topologies or modules to the libraries often comes with a high set-up effort. Basic building block libraries, e.g., [8, 9, 12, 13, 11] comprise topology variations. However, used for circuit synthesis, they include impractical and redundant topologies in
- the process taking up unnecessary computation time. When they are used for sizing and layout generation not all necessary constraints are generated. The methods, e.g. [11], are not able to recognize the load of a first stage, making the usage of other methods necessary [14]. To include more building blocks being important for op-amp design in basic libraries, attempts were made using un-

<sup>35</sup> supervised learning algorithms [15, 16]. However, these methods are still fragile and might not recognize all building blocks correctly.

In this paper, a method is presented which tackles the described disadvantages. It fills in the gap between libraries based on basic building blocks [10, 11, 12, 13] and libraries containing whole topologies [5, 4]. We achieve this

- <sup>40</sup> by capturing all building blocks the full way up to a complete op-amp. In the frequently cited papers [10, 11], the so-called sizing rules method systematically captured the structures and constraints from differential pairs and current mirrors up to a differential stage. This work additionally captures the load, transconductance and bias of amplification stages as well as the amplification
- stages themselves and their bias. A new approach on describing building blocks in op-amps is developed, giving them a well-defined functional and structural description. While the structure of a current mirror was relatively easy to establish, capturing the structure of loads, biases and amplification stages is much more complicated. In particular, while the function of these building blocks is well known they are implemented by a large variety of structures.

With the new method on formalizing existing structural knowledge of opamps presented in this paper, new approaches to sizing and structural synthesis of op-amps are developed (Sec. 9, detailed information [2, 3]). Due to the complete recognition of relevant structures in op-amps, the new methods are

- <sup>55</sup> able to capture op-amp design knowledge presented in a large number of design books, e.g., [17, 18, 19, 20, 21] to a new extent of completeness using a new systematic presentation making it usable for computer-aided op-amp design. The design methods are positioned between classical design methods with more or less fixed design plans [22, 23, 24, 25, 4, 26], which have to be set up for each
- new op-amp, and simulation-based numerical optimization approaches [27, 28, 29, 14, 30, 31, 32], which need a CAD tool setup and value seeding for each netlist. It is also positioned between optimization-based structural synthesis approaches [12, 33, 34, 13, 8] that create a large number of variants some of them being impractical or redundant, and approaches without involvement of
- optimization that investigate only a very small number of variants [35, 5].

HL 5	Op-amp	1	
HL 4	Amplification stage (a), circuit bias (b <sub>0</sub> ), compensation capacitor ( $c_C$ ), load capacitor ( $c_L$ )	Functional abstraction	
HL 3	Transconductance $(tc)$ , load $(l)$ , stage bias $(b_S)$ ,		
HL 2	Voltage bias (vb), current bias (cb), current mirror (cm), differential pair (dp), analog inverter (inv)	<ul> <li>Structura</li> <li>refineme</li> </ul>	
HL 1	Normal transistor (nt), diode transistor (dt), capacitor (cap),		¥

Figure 1: Hierarchical library of functional blocks in op-amps

The remainder of the paper is organized as follows: Sec. 2 gives a general overview of functional blocks in op-amps. Detailed explanations of the individual functional block are given in Secs. 3 - 6. The algorithms to recognize the blocks in an op-amp are presented in Sec. 7. In Sec. 8, we discuss the corresponding experimental results. Sec. 9 shows the application of the functional block decomposition method on circuit synthesis and sizing. A conclusion and an outlook on future work are presented in Secs. 10.

## 2. Functional Blocks in Op-Amps

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An op-amp can be hierarchically decomposed into functional blocks. Fig. 1 <sup>75</sup> shows this decomposition. Starting with one functional block at the highest hierarchy level (HL 5), the number of functional blocks per level increases till on the lowest level (HL 1) every device of the circuit forms a functional block of its own. On HL 1, every functional block is represented by one uniquely definable device composition. However, this level does not give any information about the

<sup>80</sup> functional task a device fulfills in the op-amp, e.g. amplification, stabilization, biasing. This functional assignment is given at HL 3 and HL 4. At these levels, the function of every functional block is uniquely definable. However, the structural description is not unique as e.g. different types of amplification stages exist. On HL 2, neither the structural nor the functional definition of the

functional blocks is unique. However, their structural complexity is less then those of the functional blocks of HL 3 and HL 4.

Fig. 2 shows as an example the functional blocks in a symmetrical opamp. For HL 1 and HL 2 (Fig 2a), all functional blocks of the same type have similar device compositions. This is different for HL 3 and HL 4 (Fig 2b). The



Figure 2: Symmetrical op-Amp with high PSRR [18] (Definitions of abbreviations in Fig. 1)

<sup>90</sup> composition of the first stage  $a_1$  differs highly from the composition of the other stages. On HL 1, HL 3, and HL 4, all devices can only be part of one functional block on a level.  $N_5$  is a normal transistor  $nt_2$  on level 1, a stage bias  $b_{2,1}$  on level 3 and part of an amplification stage  $a_{2,1}$  on level 4. On HL 2, a device can be part of more than one functional block. On this level,  $N_5$  is a current bias <sup>95</sup>  $cb_2$ , part of a current mirror  $cm_2$  and part of an analog inverter  $inv_1$ .

We define the set of functional blocks  $\mathcal{X}$  in an op-amp as:

$$\mathcal{X} = \{ x_k | k = 1, 2, ..., |\mathcal{X}| \}$$
(1)

A functional block  $x_k$  in a circuit consists either of a basic device  $d_k$  of type  $d_k.type \in \{t, c\}$ , where t is referring to transistors and c to capacitors, or of other functional blocks  $x_{k,1}, ..., x_{k,n}$  of individual types  $x_{k,l}.type \in \{dt, nt, cap, vb, cb, cm, dp, inv, g, l, b, a, c_L, c_C\}$  (see Fig. 1):

$$\forall_{x_k \in \mathcal{X}} \ (x_k = \{d_k\} \lor x_k = \{x_{k,1}, .., x_{k,n}\})$$
(2)

The subset  $\mathcal{X}_j \subseteq \mathcal{X}$  contains all functional blocks  $x_k \in \mathcal{X}$  with  $x_k.type = j$ .

To describe the connections between functional blocks, every functional block  $x_k$  is assigned a set of pins  $P_{x_k}$ , which are connected to the nets of the circuit:

$$P_{x_k} = \{x_k . p_l | l = 1, 2, .. | P_{x_k} | \}$$
(3)



Figure 3: Functional blocks on level 1

As all functional blocks consist at the end of devices, the pins  $P_{x_k}$  of a functional block  $x_k$  refer to certain device pins.

A connection of two functional blocks  $x_k, x_l$  over any net with the pins  $x_k.p_y, x_l.p_z$  is described by:

$$x_k.p_y \leftrightarrow x_l.p_z \tag{4}$$

To describe that two pins  $x_k p_y, x_l p_z$  are not allowed to be connected by any net, the following notation is used:

$$x_k.p_u \nleftrightarrow x_l.p_z \tag{5}$$

 $x_k \cdot \Phi$  denotes the substrate type of a functional block  $x_k$ , with following naming convention:

$$x_k \cdot \Phi \in \{\Phi_n, \Phi_p, \Phi_u\}, \text{ for n-, p-, or mixed-doping}$$
(6)

A functional block  $x_k$  has mixed-doping if it consists of transistors with different doping.

In the following, structural and functional definitions will be given for all functional block types in Fig. 1. Please note that all examples shown for NMOS transistors, hold analogously for PMOS transistors.

## 3. Functional Blocks on Hierarchy Level 1

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Fig. 3 shows three different device level functional blocks. In addition to capacitors, we define and use two different functional block types for transistors:

## 3.1. Normal Transistor

Function: A normal transistor  $nt_k$  establishes a relation between the the voltage potential  $v_g$  at the gate of the transistor and the current at the drain  $i_d$ of the transistor. Either  $v_g$  or  $i_d$  is the control factor.

Structure: A normal transistor  $nt_k$  is a transistor  $d_k$  without any self connections.

$$x_{k} = \{d_{k}\} \land d_{k}.type = t \land d_{k}.d \nleftrightarrow d_{k}.s \land d_{k}.d \nleftrightarrow d_{k}.g$$

$$\land d_{k}.g \nleftrightarrow d_{k}.s \Leftrightarrow x_{k}.type = nt$$

$$(7)$$

#### 3.2. Diode Transistor

Function: A diode transistor dt converts its drain-source current  $i_d$  into a stable gate-source voltage  $v_{gs}$ .

Structure: A diode transistor  $dt_k$  is a transistor  $d_k$ , whose drain  $d_k.d$  is connected to its gate  $d_k.g$ :

$$x_k = \{d_k\} \land d_k.type = t \land d_k.d \leftrightarrow d_k.g \land d_k.d \nleftrightarrow d_k.s \Leftrightarrow x_k.type = dt$$
(8)

## 4. Functional Blocks on Hierarchy Level 2

The majority of the functional blocks on HL 2 consist of transistor stacks. Typical transistor stacks are shown in Fig. 4, 5. A transistor stack  $ts_k$  is a set of 1-3 transistors having the same doping and a drain-source connection i.e., the drain of a lower transistor in the stack  $x_{k,m}.d$  is connected with the source of the next higher transistor  $x_{k,m+1}.s$ . Higher transistor gates are not allowed to be connected to drains of lower transistors. Drains of higher transistors are not allowed to be connected to lower transistor sources.

$$\begin{aligned} x_{k} = & \{x_{k,1}, ..., x_{k,n} | n = |x_{k}| \land n \leq 3\} \land x_{k} \subset (\mathcal{X}_{nt} \cup \mathcal{X}_{dt}) \land x_{k,m}.d \leftrightarrow x_{k,m+1}.s \\ & \land x_{k,m}.\Phi = x_{k,m+1}.\Phi \land x_{k,m+1}.g \nleftrightarrow x_{k,m}.d \land x_{k,m+1}.d \nleftrightarrow x_{k,m}.s \\ & \Leftrightarrow x_{k}.type = ts \end{aligned}$$

(9)



Figure 4: Voltage bias and variants with stacks of 1 or 2 transistors (dashed lines: optional pins and functional blocks)

The usual number of transistors in a stack is 1-2. For the pins in a transistor 115 stack, the following naming convention will be used. The source not connected to any drain in the stack  $ts_k s_1$  is the source  $ts_k s_1$  of the transistor stack. The drain not connected to any source of the stack  $ts_k.d_n$  is the drain  $ts_k.d$  of the transistor stack. If all drains or sources of the stack must be considered, numbering will be used. The definition of the transistor stack is in the following 120

## 4.1. Voltage Bias

used to describe the functional blocks in detail.

Function: A voltage bias  $vb_k$  converts its drain current  $i_d$  into a stable gatesource voltage  $v_{qs}$  applied to a gate of a current bias.

Structure: A voltage bias  $vb_k$  (Fig. 4) consists of a transistor stack  $x_k, x_k.type = ts$ , with the gates of its devices  $x_k.g_l$  connected to gates of a current bias  $cb_v$  with same doping as  $vb_k$ . Additionally, the drain of the stack  $x_k d = x_{k,n} d$  must be connected to a gate  $cb_v g_m$  of  $cb_v$ . For every gate  $x_k g_j$  in the stack, exactly one gate-drain connection with another transistor  $x_y \in (\mathcal{X}_{nt} \cup \mathcal{X}_{dt})$  of same doping exists. This transistor  $x_y$  must be part of a voltage or current bias  $x_z \in (\mathcal{X}_{vb} \cup \mathcal{X}_{cb})$  but not necessarily of  $vb_k$  or  $cb_v$  itself.

$$\begin{aligned} x_{k} &= \{x_{k,1}, \dots, x_{k,n} | n = |x_{k}|\} \land x_{k}.type = ts \land \exists_{cb_{v}} [cb_{v}.\Phi = x_{k}.\Phi \land x_{k,n}.d \\ \leftrightarrow cb_{v}.g_{m} \land \forall_{x_{k}.g_{l}} [x_{k}.g_{l} \leftrightarrow cb_{v}.g_{i}]] \land \forall_{x_{k}.g_{j}} [\exists !_{x_{y} \in (\mathcal{X}_{nt} \cup \mathcal{X}_{dt})} [(x_{y}.\Phi = x_{k}.\Phi \quad (10) \\ \land x_{y}.d \leftrightarrow x_{k}.g_{j}) \longleftrightarrow \exists !_{x_{z} \in (\mathcal{X}_{vb} \cup \mathcal{X}_{cb})} x_{y} \in x_{z}]] \Leftrightarrow x_{k}.type = vb \end{aligned}$$



Figure 5: Current bias and variants with stacks of 1 or 2 transistors (dashed lines: optional)

#### 125 4.2. Current Bias

Function: A current bias  $cb_k$  converts the voltage potential  $v_g$  applied at its gates into a drain current  $i_d$ .

Structure: A current bias  $cb_k$  (Fig. 5) consists typically of a stack of normal transistors, which might have a gate connection. In rare cases, the normal transistor at the bottom is exchanged by a diode transistor. The gates of a current bias  $cb_k.g_l$  are connected to a gate or the upper drain of a voltage bias  $(vb_v.g_l \vee vb_v.d)$ . The voltage bias must have the same doping. The drain of the upper transistor of a current bias  $cb_{k,n}.d = cb_k.d$  must not be connected to any gate of a voltage bias  $vb_y.g_z$  with same doping.

$$\begin{aligned} x_k &= \{x_{k,1}, .., x_{k,n} | n = |x_k|\} \land x_k.type = ts \land \exists_{vb_v} [vb_v.\Phi = x_k.\Phi \land \forall_{x_k.g_l} [x_k.g_l \\ \leftrightarrow (vb_v.g_l \lor vb_v.d)] \land \not\exists_{vb_y} [vb_y.\Phi = x_k.\Phi \land x_{k,n}.d \leftrightarrow vb_y.g_z]] \Leftrightarrow x_k.type = cb \end{aligned}$$

$$(11)$$

#### 4.3. Current Mirror

*Function:* A current mirror  $cm_k$  provides a current by the current bias, <sup>130</sup> specified by the devices sizes and the current of the voltage bias.

Structure: Fig. 6 shows the structural definition of a current mirror and examples. To form a current mirror  $cm_k$ , voltage bias  $vb_k$  and current bias  $cb_k$ must have equal doping and a source connection. The gates of the voltage bias  $vb_k.g_l$  must be connected to the gates  $cb_k.g_l$  of the current bias. The uppermost drain of the voltage bias  $vb_k.d$  must be connected to a gate of the current bias  $cb_k.g_m$ . All gates of the voltage bias  $vb_k.g_j$  with exception of the upper most



Figure 6: Current mirror and examples (dashed lines: optional)

one  $vb_k g_{|vb_k|}$  must have a connection to a drain of either voltage or current bias  $x_y d_z|_{x_y \in \{vb_k, cb_k\}}$ .

$$x_{k} = \{vb_{k}, cb_{k}\} \wedge vb_{k}.\Phi = cb_{k}.\Phi \wedge vb_{k}.s \leftrightarrow cb_{k}.s \wedge (vb_{k}.g_{l} \leftrightarrow cb_{k}.g_{l})|_{l \leq |vb_{k}|}$$

$$\wedge \exists_{cb_{k}.g_{m}}[cb_{k}.g_{m} \leftrightarrow vb_{k}.d] \wedge \forall_{vb_{k}.g_{j} \in P_{vb_{k}} \setminus \{vb_{k}.g_{|vb_{k}|}\}} [\exists!_{xy.d_{z} \in P_{xy}|_{xy \in \{vb_{k},cb_{k}\}}]$$

$$[vb_{k}.g_{j} \leftrightarrow x_{y}.d_{z}]] \Leftrightarrow x_{k}.type = cm$$

$$(12)$$

## 4.4. Differential Pair

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Function: A differential pair  $dp_k$  converts the voltage potentials at the gates of its two input transistor into amplified drain currents. Equal voltages lead to equal drain currents. Depending on the structure, higher amplification gains can be obtained. Cascode versions with four transistors have a higher amplification gain than a simple version with two transistors.

*Structure:* Fig. 7 shows the structure of a differential pair. The basic structure is the simple differential pair, which can also stand alone.

A simple differential pair  $dp_k$  consist of two normal transistors  $nt_{k,1}, nt_{k,2}$ connected only at their sources. This common source  $dp_k$  must be connected to a current bias drain  $cb_l.d$ . The two normal transistors and the current bias



Figure 7: Differential pair and examples (dashed lines: optional)

must have equal doping.

$$x_{k} = \{nt_{k,1}, nt_{k,2}\} \land nt_{k,1}.\Phi = nt_{k,2}.\Phi \land nt_{k,1}.s \leftrightarrow nt_{k,2}.s \land nt_{k,1}.d/g$$

$$\Leftrightarrow nt_{k,2}.d/g \land \exists_{cb_{l}}[nt_{k,1}.s \leftrightarrow cb_{l}.d \land nt_{k,1}.\Phi = cb_{l}.\Phi] \Leftrightarrow x_{k}.type = dp$$
(13)

For the cascode version of the differential pair  $vdp_k$ , a simple differential pair  $dp_k$  is connected with its drains to the sources of a gate connected couple  $gcc_k$ . These are two normal transistor with same doping connected at their gates:

$$x_{k} = \{nt_{k,1}, nt_{k,2}\} \land nt_{k,1}.\Phi = nt_{k,2}.\Phi \land nt_{k,1}.g \leftrightarrow nt_{k,2}.g \land nt_{k,1}.d/s \leftrightarrow nt_{k,2}.d/s \Leftrightarrow x_{k}.type = gcc$$
(14)

The structural definition of the cascode version of the differential pair  $vdp_k$  is:

$$x_{k} = \{dp_{k}, gcc_{k}\} \land (dp_{k}.d_{l} \leftrightarrow gcc_{k}.s_{l})|_{l=1,2} \land dp_{k}.s/g_{1,2} \nleftrightarrow gcc_{k}.g/d_{1,2}$$

$$\Leftrightarrow x_{k}.type = vdp$$
(15)

Two types of cascode variants exist having different doping characteristics. In the *folded cascode differential pair*  $fcdp_k$ ,  $dp_k$  and  $ggc_k$  have opposite doping:

$$vdp_k = \{dp_k, gcc_k\} \land dp_k.\Phi \neq gcc_k.\Phi \Leftrightarrow vdp_k.type = fcdp$$
(16)



Figure 8: Analog inverter and examples (dashed lines: optional)

In the cascode differential pair  $cdp_k$ , they have equal doping:

$$vdp_k = \{dp_k, gcc_k\} \land dp_k.\Phi = gcc_k.\Phi \Leftrightarrow vdp_k.type = cdp$$
(17)

## 4.5. Analog Inverter

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*Function:* An analog inverter inverts and amplifies an input voltage applied at one of its gates.

Structure: An analog inverter  $inv_k$  (Fig. 8) consists of two normal transistor stacks  $ts_{k,1}, ts_{k,2}$  differing in doping. The stacks are connected at their drains  $ts_{k,1}.d, ts_{k,2}.d$ . The two sources  $ts_{k,1}.s, ts_{k,2}.s$  are connected to the supply voltage rail that corresponds to the doping type. Gate-gate, gate-drain and source-source connections between transistors are not allowed.

$$\begin{split} x_{k} &= \{ts_{k,1}, ts_{k,2}\} \land (ts_{k,1} \cup ts_{k,2}) \subset \mathcal{X}_{nt} \land ts_{k,1}.d \leftrightarrow ts_{k,2}.d \land ts_{k,1}.\Phi = \Phi_{p} \\ \land ts_{k,2}.\Phi &= \Phi_{n} \land ts_{k,1}.s \leftrightarrow VDD \land ts_{k,2}.s \leftrightarrow GND \\ \land \forall_{nt_{i},nt_{j} \in (ts_{k,1} \cup ts_{k,2})} [nt_{i}.g \nleftrightarrow nt_{j}.g \land nt_{i}.d \nleftrightarrow nt_{j}.g \land nt_{i}.s \nleftrightarrow nt_{j}.s] \\ \Leftrightarrow x_{k}.type = inv \end{split}$$

## (18)

## 4.6. Multiple Assignments of Transistors to Functional Blocks

Hierarchy level 2 is the only level which allows transistors to be part of more than one functional block. An example are current mirrors. According



Figure 9: Relevant multiple assignments

to (12), every transistor in a current mirror  $t_k \in cm_k$  is at the same time part of a voltage or current bias  $t_k \in (vb_k \cup cb_k)$ . We distinguish between relevant, irrelevant and false multiple assignments.

Relevant multiple assignments are circuitry-wise correct and obtain additional information needed to find other functional blocks. These are the above <sup>150</sup> mentioned double assignments in current mirrors, different current mirrors with the same voltage bias but different current biases forming a current mirror bench, and the two cases shown in Fig. 9. Fig. 9a shows a gate connected couple (14)  $gcc_1$  in two current biases  $cb_1, cb_2$ . The gate connected couple must be part of a cascode version of a differential pair  $vdp_1$  (15). The transistors

 $N_3, N_4$  are therefore part of  $gcc_1, vdp_1$  and  $cb_1$  or  $cb_2$ . Fig. 9b shows an analog inverter with a transistor stack  $ts_1 = \{P_2\}$  that is also part of a current mirror  $cm_1$ . Thus,  $P_2$  is part of  $inv_1, cm_1$  and the current bias  $cb_1$  in  $cm_1$ .

Irrelevant multiple assignments are circuitry-wise correct but do not obtain any additional information to the functional behavior as the functional blocks the transistor is in are of the same type. An example is a simple current mirror in a cascode current mirror (Fig. 10a). The simple current mirror does not obtain any additional information to the cascode current mirror. To avoid such irrelevant multiple assignments of transistors following rule is used:

$$\forall_{x_k \in \mathcal{X}_{min}} [\exists_{x_l \in \mathcal{X}} (x_k \subset x_l \land x_k.type = x_l.type)] \Leftrightarrow x_k \text{ is irrelevant}$$
(19)



Figure 10: Irrelevant (a) and false (b) multiple assignments

 $\mathcal{X}_{min}$  contains all functional blocks which are potential irrelevant. These are all current mirrors, voltage and current biases.

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False multiple assignments are circuitry-wise incorrect, e.g., two transistor stacks in a differential pair with current bias (Fig 8). With suitable transistors connected at the drain of the differential pair, these false transistor stacks might form analog inverters. By suppressing the recognition of these transistor stacks, the false recognition of analog inverters is omitted.

#### <sup>165</sup> 5. Functional Blocks on Hierarchy Level 3

On HL 3 are the functional block types that form the amplification stages (HL 4) of an op-amp, i.e., transconductance, load and stage bias.

## 5.1. Transconductance

*Function:* A transconductance converts a voltage potential applied at its gates into an (amplified) current.

Structure: Fig. 11 shows the structural definition of a transconductance  $tc_k$  as well as examples. Two different types of transconductance exist, non-inverting and inverting.

A non-inverting transconductance  $tc_{ninv}$  consists of 1 or 2 differential pairs. <sup>175</sup> We further define three different types having three different structures:



Figure 11: Transconductance (Transcond.) and examples (dashed lines: optional)

A simple transconductance  $tc_s$  is a transconductance consisting of one differential pair, having no gate connection to any other differential pair.

$$x_k = \{dp_k\} \land \not\exists_{dp_i} \ (dp_k.g_y|_{y=1,2} \leftrightarrow dp_l.g_z|_{z=1,2}) \Leftrightarrow \ x_k.type = tc_s$$
(20)

A complementary Transconductance  $tc_c$  consists of two differential pairs with opposite doping and connected at both gates

$$x_{k} = \{dp_{k,1}, dp_{k,2}\} \land (dp_{k,1}.g_{l} \leftrightarrow dp_{k,2}.g_{l})|_{l=1,2} \land dp_{k,1}.\Phi \neq dp_{k,2}.\Phi$$

$$\Leftrightarrow x_{k}.type = tc_{c}$$
(21)

A common-mode feedback (CMFB) transconductance  $tc_{CMFB}$  consists of two differential pairs with equal doping connected at one of the two gates:

$$x_{k} = \{dp_{k,1}, dp_{k,2}\} \land \exists !_{dp_{k,1}.g_{m}, dp_{k,2}.g_{n}} [dp_{k,1}.g_{m} \leftrightarrow dp_{k,2}.g_{n}] \land dp_{k,1}.\Phi = dp_{k,2}.\Phi \Leftrightarrow x_{k}.type = tc_{CMFB}$$

$$(22)$$

A inverting transconductance  $tc_{inv}$  consists of a transistor stack  $ts_k$  of m normal transistors, with the source  $ts_k.s$  connected to a supply voltage rail. No gate-gate and gate-drain connection of the transistors in the stack is allowed. The gate of the bottom transistor in the stack  $ts_k.g_1$  is connected to the output of another transconductance  $tc_v.out_p$  or to the output of a load  $l_w.out_q$ . The



Figure 12: Load (dashed lines: optional)

drain of the stack  $ts_k.d$  is connected to the output of a stage bias  $b_{s,y}.out_z$ .

$$x_{k} = \{ts_{k}\} \land ts_{k} \subset \mathcal{X}_{nt} \land \operatorname{net}(ts_{k}.s) \in \mathcal{N}_{supply} \forall_{nt_{i},nt_{j} \in ts_{k}} (nt_{i}.g/d \nleftrightarrow nt_{j}.g/d) \land [\exists_{tc_{v}}[tc_{v}.out_{p} \leftrightarrow ts_{k}.g_{1}] \lor \exists_{l_{w}}[l_{w}.out_{q} \leftrightarrow ts_{k}.g_{1}]] \land \exists_{b_{s,y}}[b_{y}.out_{z} \leftrightarrow ts_{k}.d] \Leftrightarrow x_{k}.type = tc_{inv}$$

$$(23)$$

The definition of the load is given in the next section. The definition of the stage bias is given in Sec. 5.3.

## 5.2. Load

*Function:* A load converts a current into a voltage. It influences the gain generated by the connected transconductance.

Structure: Fig. 12 shows the structure of a load  $l_k$ . A load  $l_k$  consists of one or two load parts  $l_{p,k,l}$  of type  $l_p$ . The parts are connected at their drains and have different substrate types. If a gate connected couple  $gcc_j$  is in one of the load parts, its sources  $gcc_j.s_y$  are connected to the output of a transconductance  $tc_w$  of type  $tc_{ninv}$ . Otherwise, if no gate connected-couple is in one of the load



Figure 13: Different types of biases (dashed lines: optional)

parts, the outputs of the load  $l_k.out_v$  are connected to  $tc_w.out_v$ .

$$x_{k} = \{x_{k,1}, ..., x_{k,n} | n = |x_{k}| \land n \leq 2\} \land x_{k} \subseteq \mathcal{X}_{l_{p}} \land [n = 2 \rightarrow [x_{k,1}.\Phi \neq x_{k,2}.\Phi \land (x_{k,1}.d_{l} \leftrightarrow x_{k,2}.d_{l})|_{l=1,2}]] \land [\exists_{gcc_{j} \in x_{k}} [(gcc_{j}.s_{y} \leftrightarrow tc_{z}.out_{y})|_{y=1,2,tc_{z}.type=tc_{ninv}}] \\ \oplus (x_{k}.out_{v} \leftrightarrow tc_{w}.out_{v})|_{v \leq |x_{k,1}|, tc_{w}.type=tc_{ninv}}] \Leftrightarrow x_{k}.type = l$$

$$(24)$$

A single load part  $l_{p,k,l}$  consists of one or two transistor stacks, which have gate-gate connections. A transistor stack in a load part is either of type voltage or current bias. If no gate connected-couple is in the load part, the sources must be connected. The doping of the transistor stacks is equal.

$$x_{k} = \{x_{k,1}, \dots, x_{k,n} | n = |x_{k}| \land n \leq 2\} \land x_{k} \subset (\mathcal{X}_{vb} \cup \mathcal{X}_{cb}) \land (x_{k,1}.g_{l} \\ \leftrightarrow x_{k,n}.g_{l})|_{l \leq |x_{k,1}|} \land \not \exists_{gcc_{l} \in x_{k}} [x_{k,1}.s \leftrightarrow x_{k,n}.s] \land x_{k,1}.\Phi = x_{k,n}.\Phi \Leftrightarrow x_{k}.type = l_{p}$$

$$(25)$$

5.3. Stage Bias

*Function:* A stage bias  $b_s$  supplies a transconductance with defined currents. Structure: A stage bias  $b_s$  is a subtype of the type bias b (Fig. 13). Two different types exist.

A bias with voltage output  $b_v$  consists of m voltage and n current biases with m > n. Its input  $b_{v,k}$  in is the drain of a voltage bias. The outputs  $b_{v,k}$  out<sub>1</sub>, ...,  $b_{v,k}$  out<sub>i</sub> are gates of voltage biases, which are connected to gates of other functional blocks. All current biases in  $b_{v,k}$  must have a drain-drain connection to a voltage bias with opposite doping and a gate-gate connection to a voltage bias with equal doping in  $x_k$ .

$$\begin{aligned} x_{k} &= \{x_{k,1}, ..., x_{k,l} | l = |x_{k}|\} \land \{x_{k,1}, ..., x_{k,m}\} \subset \mathcal{X}_{vb} \land (l \neq m \rightarrow \{x_{k,l-m}, ..., x_{k,l}\} \subset \mathcal{X}_{cb}) \land \exists_{vb_{k,i} \in x_{k}} [vb_{k,i}.g_{j} \leftrightarrow x_{z}.g_{y}|_{x_{z} \in \mathcal{X} \backslash x_{k}}] \land \forall_{cb_{k,q} \in x_{k}} [cb_{k,q}.d \leftrightarrow vb_{k,v}.d \land vb_{k,v} \in x_{k} \land cb_{k,q}.\Phi \neq vb_{k,v}.\Phi \land (cb_{k,q}.g_{s} \leftrightarrow vb_{k,w}.g.s)|_{s \leq |cb_{k,q}|} \land vb_{k,w} \in x_{k} \land cb_{k,q}.\Phi = vb_{k,w}.\Phi] \Leftrightarrow x_{k}.type = b_{v} \end{aligned}$$

$$(26)$$

A bias with voltage output  $b_{v,k}$  is a stage bias, iff it consists of exactly one voltage bias  $vb_k$ , which is connected with its drain  $vb_k.d$  to the output of a transconductance of type inverting:

$$b_{v,k} = \{vb_k\} \land \exists_{tc_i}[tc_i.type = tc_{inv} \land vb_k.d \leftrightarrow tc_i.out] \Leftrightarrow b_{v,k}.type = b_s \quad (27)$$

In all other cases, if a bias with voltage out consists of more than one voltage bias or if it is not connected with its input pin to a transconductance, it is the circuit bias  $b_O$  (Sec. 6.2)

A bias with current output  $b_c$  consist of n current biases. Its inputs  $in_1, ... in_m$  are the gates of the current biases. The outputs  $out_1, ..., out_n$  are the drains of the current biases, which must be connected to the source or output of a transconductance.

$$x_{k} = \{cb_{k,1}, .., cb_{k,n} | n = |x_{k}|\} \land x_{k} \subset \mathcal{X}_{cb} \land \forall_{cb_{k,l} \in x_{k}} [cb_{k,l}.d$$

$$\leftrightarrow (tc_{z}.s|_{tc_{z}.type=tc_{ninv}} \lor tc_{z}.out_{y}|_{tc_{z}.type=tc_{inv}})] \Leftrightarrow x_{k}.type = b_{c}$$

$$(28)$$

A bias with current output is always a stage bias:

$$\forall_{b_k \in \mathcal{X}_b} [b_k.type = b_c \to b_k.type = b_s] \tag{29}$$



Figure 14: Amplification stage (dashed lines: optional)

## 6. Functional Blocks on Hierarchy Level 4

The functional block types on HL 4 are the amplification stage, the circuit <sup>190</sup> bias, the compensation and load capacitor.

## 6.1. Amplification Stage

Function: Two functional types of amplification stage exist: the  $n^{th}$  amplification stage of an op-amp  $a_n$  and the common-mode feedback stage  $a_{CMFB}$ . The  $n^{th}$  amplification stage  $a_n$  amplifies the input signal for the  $n^{th}$  time. A common-mode feedback (CMFB) stage  $a_{CMFB}$  amplifies the output signals of a fully differential op-amp while comparing them to a reference voltage and feeds them back to the amplifier.

Structure: Fig. 14 shows the general composition of the amplification stages of an op-amp. Every amplification stage has at least two inputs and one output. It has a source connection to both supply voltage rail. Two structural types of amplification stages exist, non-inverting and inverting amplification stages. Non-inverting amplification stages are the first stage of an op-amp and the CMFB stage. Inverting stages form the further stages of an op-amp  $(n \ge 2)$ . In the following, both types are described in detail. A non-inverting amplification stage  $a_{ninv}$  consists of a transconductance  $tc_k$ , a load  $l_k$  and a stage bias  $b_{s,k}$ . The transconductance must be of type noninverting and the stage bias must have a current output connected to the sources of the transconductance. The load outputs or the sources of a gate connected couple in the load must be connected to the outputs of the transconductance.

$$x_{k} = \{tc_{k}, l_{k}, b_{s,k}\} \wedge tc_{k}.type = tc_{ninv} \wedge b_{s,k}.type = b_{c} \wedge [\exists_{gcc_{i} \in l_{k}}[(gcc_{i}.s_{j} \leftrightarrow tc_{k}.out_{j})|_{j=1,2}] \oplus \forall_{l_{k}.out_{v} \in P_{l_{k}}}[l_{k}.out_{v} \leftrightarrow tc_{k}.out_{w}]]$$

$$\wedge (tc_{k}.s_{l} \leftrightarrow b_{s,k}.out_{l})|_{l \leq |tc_{k}|} \Leftrightarrow x_{k}.type = a_{ninv}$$

$$(30)$$

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Non-inverting amplification stages are classified into three types: simple first stage  $a_s$ , complementary first stage  $a_c$ , and CMFB stage  $a_{CMFB}$ . The types differ in the transconductance types and the doping characteristics of its functional blocks.

A simple first stage  $a_s$  has a transconductance of type  $tc_s$ . The transconductance and the stage bias have the same substrate type, while the load has either the opposite doping or mixed doping.

$$a_{ninv} = \{tc_k, l_k, b_{s,k}\} \land tc_k.type = tc_s \land (tc_k.\Phi = b_{s,k}.\Phi) \in \{\Phi_n, \Phi_p\}$$
  
$$\land tc_k.\Phi \neq l_k.\Phi \Leftrightarrow a_{ninv}.type = a_s$$
(31)

A complementary first stage  $a_c$  has a transconductance of type  $tc_c$ . Transconductance, load and stage bias have all mixed doping.

$$a_{ninv} = \{tc_k, l_k, b_{s,k}\} \wedge tc_k.type = tc_c \wedge tc_k.\Phi = b_{s,k}.\Phi = l_k.\Phi = \Phi_u$$
  
$$\Leftrightarrow a_{ninv}.type = a_c$$
(32)

A common-mode feedback stage  $a_{CMFB}$  has a transconductance of type  $tc_{CMFB}$ . Transconductance and stage bias have the same substrate type, while

the load has opposite doping.

$$a_{ninv} = \{tc_k, l_k, b_{s,k}\} \wedge tc_k.type = tc_{CMFB} \wedge (tc_k.\Phi = b_{s,k}.\Phi) \in \{\Phi_n, \Phi_p\}$$

$$\wedge tc_k.\Phi \neq l_k.\Phi|_{l_k.\Phi \in \{\Phi_n, \Phi_p\}} \Leftrightarrow a_{ninv}.type = a_{CMFB}$$
(33)

A inverting amplification stage  $a_{inv}$  consists of a transconductance  $tc_k$  and a stage bias  $b_{s,k}$  with opposite doping connected at their outputs. The transconductance must be of type inverting. The stage bias consists either of one voltage bias or one current bias.

$$a_{k} = \{tc_{k}, b_{s,k}\} \wedge tc_{k}.type = tc_{inv} \wedge b_{s,k}.type \in \{b_{c}, b_{v}\} \wedge |b_{s,k}| = 1$$

$$\wedge tc_{k}.out_{1} \leftrightarrow b_{s,k}.out_{1} \wedge tc_{k}.\Phi \neq b_{s,k}.\Phi \Leftrightarrow a_{k}.type = a_{inv}$$
(34)

Note, that all inverting stages can occur twice in an op-amp, e.g., two second stages. It appears when the op-amp is fully differential or a symmetrical op-amp (Fig. 2, with  $a_{2,1}, a_{2,2}$ ).

Differentiating between an inverting stage with a stage bias with current output and an inverting stage with a stage bias with voltage output allows to give a more precise definition of inverting amplification stages:

A inverting stage with stage bias with current output  $a_{inv_c}$  must also fulfill the type definition of an analog inverter to be a valid inverting amplification stage:

$$a_{inv,k} = \{tc_{inv,k}, b_{s,k}\} \land b_{s,k}.type = b_c \land a_{inv,k}.type = inv \Leftrightarrow a_{inv,k}.type = a_{inv_c}$$
(35)

<sup>215</sup> Note, that not all analog inverters are inverting stages, as the constraints for a transconductance (23) and stage bias (28) must hold.

A inverting stage with stage bias with voltage output  $a_{inv_v}$  only occurs in symmetrical OTAs, which are op-amps with a characteristic first stage and two second stages (Fig. 2). The first stage  $a_1$  must be a simple first stage  $a_s$  having a load consisting of two voltage biases  $vb_{l,1}, vb_{l,2}$  with same doping. Both voltage biases must have a gate-gate connection to a transconductance in a second stage of type  $a_{inv}$ . One second stage  $a_z$  must be of type  $a_{inv_c}$ . The other second stage  $a_y$  must have a voltage bias as stage bias, which has a gate-gate connection to the stage bias of  $a_z$ :

$$a_{inv,k} = \{tc_{inv,k}, b_{s,k}\} \land b_{s,k}.type = b_v \land \exists_{a_1} \left[a_1.type = a_s \land \exists_{l_1 \in a_1} [|l_1| = 1 \land \exists_{l_{1,1} \in l_1} [\{vb_{l,1}, vb_{l,2}\} \subseteq l_{1,1} \land (vb_{l,m}.g_1 \leftrightarrow tc_{inv,k}.in_1 \land vb_{l,n}.g_1 \leftrightarrow a_i.in_1)|_{(m=1 \land n=2) \lor (m=2 \land n=1)} \land a_i.type = a_{inv_c} \land (b_{s,k}.out_v \leftrightarrow b_i.in_v|_{b_i \in a_i})]] \Leftrightarrow a_{inv,k}.type = a_{inv_v}$$

$$(36)$$

## 6.2. Circuit Bias

Function: The circuit bias  $b_O$  supplies all functional blocks of type amplification stage a with voltages specified by  $b_O$ .

Structure: The circuit bias  $b_O$  has the structure of a bias with voltage output (26) (Fig. 13a). It contains all current biases and voltage biases not part of an amplification stage.

$$x_{k} = \{x_{k,1}, .., x_{k,n} | n = |x_{k}|\} \land x_{k} = [(\mathcal{X}_{vb} \cup \mathcal{X}_{cb}) \setminus \mathcal{X}_{a}] \land x_{k}.type = b_{v}$$

$$\Leftrightarrow x_{k}.type = b_{O}$$
(37)

## 220 6.3. Compensation Capacitor

*Function:* A compensation capacitor  $c_{C,k}$  increases the stability of an opamp.

Structure: A compensation capacitor  $c_{C,k}$  is connected between the outputs of two different amplification stages  $a_j, a_v$ :

$$x_{k} = \{cap_{k}\} \land [cap_{k}.p_{1} \leftrightarrow a_{j}.out_{i} \land cap_{k}.p_{2} \leftrightarrow a_{v}.out_{w}]|_{a_{j} \neq a_{v}} \Leftrightarrow x_{k}.type = c_{C}$$

$$(38)$$

## 6.4. Load Capacitor

*Function:* The load capacitor  $c_{L,k}$  represents the capacitive load the op-amp is able to drive in its application.



Figure 15: Dependency graph of the functional blocks in op-amps (see Fig. 1)

Structure: A load capacitor  $c_{L,k}$  is connected between an output of the highest (*n*-th) amplification stage  $a_n$  and ground:

$$x_k = \{cap_k\} \land cap_k.p_1 \leftrightarrow a_n.out_j \land \operatorname{net}(cap_k.p_2) = GND \Leftrightarrow x_k.type = c_L$$
(39)

#### 7. Functional Block Analysis

The functional block analysis recognizes all functional blocks in an op-amp netlist based on the definitions given in Sec. 3 - 6. Fig. 15 shows the dependency graph that arises from these definitions. Note, that bidirectional dependencies exist. Therefore complex algorithms are required for the functional block analysis.

## 7.1. Hierarchy Level 1

On hierarchy level 1, the definitions of the functional block types are independent of each other. Therefore, the definitions given in Sec. 3 can be used for recognition without any restriction to their order.

#### 7.2. Hierarchy Level 2

On level 2, every recognition of a functional block type depends on another functional block on the same level (10) - (18). Voltage bias and current bias are

Algorithm 1 Recognition of functional block types on hierarchy level 2

**Require:**  $\mathcal{X} = \mathcal{X}_{nt} \cup \mathcal{X}_{dt} \cup \mathcal{X}_{dt}$ 1:  $\mathcal{X}_{vb} := \{\} / / At$  the beginning the set of voltage biases is empty 2:  $\mathcal{X}_{cb} := \{\}$  //At the beginning the set of current biases is empty 3:  $\mathcal{X}_{ts_n}$  :=findAllTransistorStacksNMOS( $\mathcal{X}$ ) //Definition (9) 4:  $\mathcal{X}_{ts_p}$  :=findAllTransistorStacksPMOS( $\mathcal{X}$ ) //Definition (9) 5: repeat for all  $ts_k \in [\mathcal{X}_{ts_j}|_{j \in \{n,p\}} \setminus (\mathcal{X}_{vb} \cup \mathcal{X}_{cb})]$  do 6: if  $\exists_{ts_l \in \mathcal{X}_{ts_s}} [ts_k.d \leftrightarrow ts_l.g_m \land \forall_{ts_k.g_v} [ts_k.g_v \leftrightarrow ts_l.g_w]]$  then 7: 8:  $\mathbf{if} \,\,\forall_{ts_l \cdot g_m} [ts_l . g_m \leftrightarrow (ts_k . g_m \lor ts_k . d)] \land$  $\not \exists_{ts_i \in \mathcal{X}_{ts_j}} \ [ts_i.g_n \leftrightarrow ts_l.d] \ \mathbf{then}$  $\mathcal{X}_{vb} := \mathcal{X}_{vb} \cup \{ts_k\}$ 9:  $\mathcal{X}_{cb} := \mathcal{X}_{cb} \cup \{ts_l\}$ 10:else if  $ts_l \in \mathcal{X}_{cb}$  then 11: $\mathcal{X}_{vb} := \mathcal{X}_{vb} \cup \{ts_k\}$ 12:end if 13:14:end if 15:end for 16: until no new voltage or current bias was found 17:  $\mathcal{X}_{cm} := \text{findAllCurrentMirrors}(\mathcal{X}_{vb}, \mathcal{X}_{cb}) //\text{Definition} (12)$ 18:  $\mathcal{X}_{dp}, \mathcal{X}_{vdp} := \text{findAllDifferentialPairs}(\mathcal{X}_{nt}, \mathcal{X}_{cb}) //\text{Definitions} (13), (15)$ 19:  $\mathcal{X}_{inv} := \text{findAllAnalogInverters}(\mathcal{X}_{ts_n}, \mathcal{X}_{ts_p}) //\text{Definition} (18)$ 20:  $\mathcal{X} := \mathcal{X} \cup \mathcal{X}_{vb} \cup \mathcal{X}_{cb} \cup \mathcal{X}_{cm} \cup \mathcal{X}_{dp} \cup \mathcal{X}_{vdp} \cup \mathcal{X}_{inv}$ 21:  $\mathcal{X} := \text{deleteIrrelevantStructures}(\mathcal{X}) //\text{Definition}$  (19) 22: return X

at the starting point of the dependency graph being bidirectionally dependent.

<sup>240</sup> Alg. 1 presents the recognition algorithm.

To resolve all dependencies, we propose to start with the recognition of transistor stacks (9), which are auxiliary blocks independent of all functional block types of level 2. On basis of the recognized transistor stacks, the current and voltage biases are recognized. For every substrate type, a set of transistor stacks  $\mathcal{X}_{ts_j}|_{j \in \{n,p\}}$  is created (Line 3, 4). The algorithm iterates over both sets. It searches for two transistor stacks  $ts_k, ts_l$ , which are connected at their gates and also have a drain-gate connection  $ts_k.d \leftrightarrow ts_l.g_m$  (Line 7). This corresponds to the definition of a voltage bias (10), taking  $ts_k$  as voltage bias connected to a current bias  $ts_l$ . It is checked if  $ts_l$  has all the gate-drain and gate-gate

connections to  $ts_k$  needed for a current bias (Line 8), and if it is not connected with its drain to any gate of a transistor stack in  $\mathcal{X}_{ts_j}$ . This corresponds to the definition of a current bias (11). If this is the case, the  $ts_k$  and  $ts_l$  are primary voltage and current biases, i.e., they have all gate-gate and gate-drain connection to each other. Another case is that  $ts_l$  is an already identified current bias (Line

- <sup>255</sup> 11). In this case, the primary voltage and current bias were already recognized and a *secondary voltage bias*  $ts_k$  is recognized, e.g. a voltage bias which biases the uppermost gate of a wide-swing cascode current mirror. Note, that the last part of the voltage bias definition (10) is not checked as this is always ensured by using an valid op-amp topology.
- The repetitive iteration over all recognized transistor stacks is needed to ensure that all secondary voltage biases are found. After finding all voltage and current biases. The current mirrors and differential pairs are found using their definitions. The analog inverter is the last functional block of HL 2, which is recognized to omit their false recognition in differential pairs. With (19) all irrelevant functional blocks are deleted from the set of all functional blocks.

#### 7.3. Hierarchy Level 3 - 4

We combine the recognition of the functional block types of HL 3 and HL 4 as this simplifies the recognition process and resolves the bidirectional dependency of the inverting transconductance  $tc_{inv}$  and its stage bias  $b_s$ . The algorithm (Alg. 2) starts by recognizing all non-inverting transconductances. They are the only functional blocks on HL 3 that are independent of any other functional block (30).

In the next step, the loads are recognized. Here we propose not to use the exact definition of the load (24) but instead use the algorithm shown in Alg. 3.

- 275 The advantage of this algorithm is that it does not depend on recognized voltage or current biases as the definition (25) does. Often external voltage biases are used to bias the load. In this case, current biases as load are not recognized. Alg. 3 is more general and uses transistor stacks for recognition. It first searches for the nets, to which the load parts are connected (Line 4 9). This is either
- the drain net of a gate connected couple  $gcc_l.d$  or if no  $gcc_l$  exists, the drain nets of differential pairs in  $tc_{ninv,k}$ . At these nets, the algorithm searches for the transistor stacks forming the load (Line 12 - 19). Note, that a gate connected

Algorithm 2 Recognition of functional block types on the hierarchy levels 3-4

```
Require: \mathcal{X}
    1: //Searching for non-inverting stages
    2: \mathcal{X}_{tc_{ninv}} :=findAllNonInvertingTransconductance(\mathcal{X}_{dp}, \mathcal{X}_{vdp}) //Definitions (20),
               (21), (22)
    3: \mathcal{X}_l := findAllLoads(\mathcal{X}_{tc_{ninv}}, \mathcal{X}) / / Algorithm 3,
    4: \mathcal{X}_{b_{s,ninv}} := \text{findStageBiases}(\mathcal{X}_{tc_{ninv}}, \mathcal{X}_{cb}) //\text{Definition} (29)
    5: \mathcal{X}_{a_{ninv}} := findAllNonInvertingStages(\mathcal{X}_{tc_{ninv}}, \mathcal{X}_l, \mathcal{X}_{b_{s,ninv}}) //Definitions (31), (32),
               (33)
    6: \mathcal{X} := \mathcal{X} \cup \mathcal{X}_{tc_{ninv}} \cup \mathcal{X}_l \cup \mathcal{X}_{b_{s,ninv}} \cup \mathcal{X}_{a_{ninv}}
    7: //Searching for inverting stages
    8: X_{a_{inv}} = \{\}
    9: repeat
 10:
                        for all inv_k \in \mathcal{X}_{inv} do
                                 if \exists_{ts_{k,1} \in inv_k} [\exists_{a_i \in \mathcal{X}_a} a_i.out_j \leftrightarrow ts_{k,1}.g_1] \land \exists_{ts_{k,2} \in inv_k} (ts_{k,2}.type = cb) then
 11:
                                           tc_{inv,k} = ts_{k,1}
 12:
 13:
                                          b_{s,inv,k} = ts_{k,2}
                                          a_{inv,k} = \{tc_{inv,k}, b_{s,inv,k}\}
 14:
 15:
                                           \mathcal{X} := \mathcal{X} \cup \{tc_{inv,k}, b_{s,inv,k}, a_{inv,k}\}
 16:
                                  end if
                                 \mathbf{if} \ |\mathcal{X}_{a_{inv}}| = 1 \land \exists_{a_1}[a_1.type = a_s \land \exists_{l_1 \in a_1}[|l_1| = 1 \land \exists_{l_{1,1} \in l_1}(\{vb_{l,1}, vbl_2 \subseteq l_{1,1})]]]
17:
                                 then
                                           \mathbf{if} \ \exists_{ts_i}[ts_i.g_1 \ \leftrightarrow \ (vb_{l,1}.g_1 \ \lor \ vb_{l,2}.g_1) \ \land \ ts_i.d \ \leftrightarrow \ vb_j.d \ \land \ (vb_j.g_q \ \leftrightarrow \ vb_{l,2}.g_1) \ \land \ ts_i.d \ \leftrightarrow \ vb_{l,2}.g_1 \ \to \ vb_{l,2}.g_1 \ \to
18:
                                           a_{inv,1}.g_{q}|_{a_{inv,1}\in\mathcal{X}_{a_{inv}}})|_{q\leq |vb_{j}|}] then
 19:
                                                    tc_{inv,i} = ts_i
20:
                                                    b_{s,inv,v} = vb_j
 21:
                                                    a_{inv,v} = \{tc_{inv,i}, b_{s,inv,v}\}
 22:
                                                    \mathcal{X} := \mathcal{X} \cup \{tc_{inv,i}, b_{s,inv,v}, a_{inv,v}\}
23:
                                           end if
24:
                                 end if
25:
                        end for
26: until no new stage is found
27: \mathcal{X}_{b_{O}} := \operatorname{findCircuitBias}(\mathcal{X}_{cb} \cup \mathcal{X}_{vb}, \mathcal{X}_{a}) //\operatorname{Definition} (37)
28: \mathcal{X}_{c_C} := \text{findCompensationCapacitors}(\mathcal{X}_{cap}, \mathcal{X}_a) //\text{Definition} (38)
29: \mathcal{X}_{c_L} := \text{findLoadCapacitors}(\mathcal{X}_{cap}, \mathcal{X}_a) //\text{Definition} (39)
30: \mathcal{X} := \mathcal{X} \cup \mathcal{X}_{b_O} \cup \mathcal{X}_{c_C} \cup \mathcal{X}_{c_L}
31: return X
```

Algorithm 3 findAllLoads( $\mathcal{X}_{tc_{ninv}}, \mathcal{X}$ )

Require:  $\mathcal{X}_{tc_{ninv}}, \mathcal{X}$ 1:  $\mathcal{X}_l := \{\}$ 2: for all  $tc_{ninv,k} \in \mathcal{X}_{tc_{ninv}}$  do 3:  $\mathcal{N} := \{\} // \text{Set of nets the load parts are connected to is empty}$ 4: if  $\exists_{dp_l \in tc_{ninv,k}} \{dp_l\} \subset vdp_l$  then 5: $gcc_l = vdp_l \setminus \{dp_l\}$  $\mathcal{N} := \mathcal{N} \cup \{ \operatorname{net}(gcc_l.d_1), \operatorname{net}(gcc_l.d_2) \}$ 6: 7: else  $\mathcal{N} := \mathcal{N} \cup \{ \operatorname{net}(tc_{inv,k}.out_1), \operatorname{net}(tc_{inv,k}.out_2), .. \}$ 8: 9: end if  $l_{p,n} := \{\} / / \text{The load part containing NMOS transistors is empty}$ 10:  $l_{p,p}:=\{\}//\text{The load part containing PMOS transistors is empty}$ 11: for all  $n_i \in \mathcal{N}$  do 12:if  $\exists_{ts_m}[ts_m.\Phi = \Phi_n \land \operatorname{net}(ts_m.d) = n_j \land [ts_m.s \leftrightarrow (GND \lor tc_{ninv,k}.out_z)]]$ 13: $\mathbf{then}$  $l_{p,n} := l_{p,n} \cup \{ts_m\}$ 14:end if 15:if  $\exists_{ts_n}[ts_n.\Phi = \Phi_p \wedge \operatorname{net}(ts_n.d) = n_j \wedge [ts_n.s \leftrightarrow (VDD \lor tc_{ninv,k}.out_z)]]$  then 16:17: $l_{p,p} := l_{p,p} \cup \{ts_n\}$ end if 18: end for 19: $\mathcal{X}_l := \mathcal{X}_l \cup \{l_{p,p}, l_{p,n}\}$ 20:21: end for 22: return  $X_l$ 

couple if recognized, is part of a load while a differential pair is not.

After the recognition of the loads, the stage biases of non-inverting stages are recognized by definition (29). With the non-inverting transconductances, loads and stage biases, the non-inverting stages are recognized.

In the next step, inverting stages are recognized. For recognition, we use that an inverting stage is also a functional block of type analog inverter iff its stage bias is of type current bias (35). This resolves the bidirectional dependency of an

- <sup>290</sup> inverting transconductance  $tc_{inv,k}$  and its bias  $b_{s,inv,k}$ . The algorithm iterates over all recognized analog inverters. For every analog inverter, it is checked, if one of its stacks  $ts_{k,1}$  is connected with its first gate  $ts_{k,1}.g_1$  to the output of an already recognized stage  $a_i$ . This corresponds to the definition of an inverting transconductance  $tc_{inv,k}$  (23). The output of a stage is either the output of its
- load or the output of its transconductance (Fig. 11). The other transistor stack  $ts_{k,2}$  in the analog inverter must be of type current bias and thus is the stage

bias (29) of the inverting stage.

After finding the first inverting stage with current bias as stage bias, it is searched for an inverting stage with voltage bias as stage bias (36). This type of inverting stage is only part of an op-amp if the first stage fulfills the criteria of a symmetrical op-amp (Line 17). It is sufficient to search for a transistor stack  $ts_i$  connected with its gate  $ts_i.g_1$  to one of the voltage biases in the first stage load.  $ts_i$  must be connected with its drain  $ts_i.d$  to a voltage bias drain  $vb_j.d$ . The voltage bias  $vb_j$  must be connected with its gates to the current bias of the already recognized inverting stage  $a_{inv,1}$ .

As inverting stages might be connected to other inverting stages, as, e.g, a third stage, it is repeatedly iterated over the set of analog inverters until no new stage is found. Thus, also multi-stage op-amps are supported by this method. Multi-stage op-amps usually comprise multiple inverting stage. Some of them may be connected in frequency compensation in feedback loops [36, 37]. However, as they have the characteristic structure of an inverter and as the gate of one of the transistors in the transconductance is connected to the output of the previous stage, they are unambiguously identifiable.

After finding all amplification stages of an op-amp, the circuit bias, compen-<sup>315</sup> sation and load capacitors are recognized using their definitions.

## 8. Experimental results

In this section, we present experimental results of the functional block analysis. We illustrate the behavior of the algorithms presented in Sec. 7 on the example of a telescopic two-stage op-amp (Fig. 16). Furthermore, we discuss the results of the functional block analysis on three different circuits: a symmetrical op-amp (Fig. 2), a folded-cascode op-amp with CMFB (Fig. 17) and a threestage op-amp (Fig. 18). Overall more than 4000 different op-amp topologies have been successfully analyzed.

The computational cost of the algorithm is very low. The runtime for every topology is in the area of milliseconds. The time needed to add a new functional



Figure 16: Blocks recognized during functional block analysis in a telescopic two-stage op-amp

block to the algorithm depends on the uniqueness of its structures. It is very low and in the area of a few hours, if many of the already implemented functional blocks are reused. More advanced functional blocks need a day integration time. Frequency compensation methods as described in [38, 39] can be integrated in this method in less than a work day.

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Telescopic op-amp (HL 2): Fig. 16a shows all functional blocks recognized on level 2 with Alg. 1. Alg. 1 first searches for all transistor stacks in the circuit sorted according to their substrate type. All transistor stacks are marked in dark blue. Transistor stacks including transistors of the differential pair  $(P_1, P_2)$ are not shown as they are not valid (Sec. 4.6). Every transistor in the circuit 335 is a transistor stack by itself. That means for the three transistor stacks consisting of two transistors, every transistor in these stacks is also a transistor stack by itself. The algorithm checks which of the transistor stacks are voltage and current biases. Note that, for  $P_5, P_8$ , the transistor stacks of the individual transistors are classified as a current bias and voltage bias, respectively.  $P_5$  has 340 a gate connection to the voltage bias  $vb_1(P_7)$  and therefore fulfills the definition of a current bias.  $P_8$  has a gate-drain connection to itself and therefore is a voltage bias connected with its gate to the gates of the current biases  $cb_4(P_3)$  and  $cb_5(P_5)$ . The other two transistor stacks  $N_1, N_3$  and  $N_2, N_4$ , form a current mir-

<sup>345</sup> ror. The transistor stacks of the individual transistors therefore are irrelevant.

Note that  $vb_2$  does not form current mirrors with  $cb_4$  and  $cb_5$  as their sources are not connected to the same net. All voltage and current biases in this circuit are primary. All voltage biases have their needed gate-drain connection (10) by themselves, such that no secondary voltage biases are needed to establish a drain-gate connection of a voltage bias gate. Alg. 1 ends with the recognition

of the cascode differential pair  $cdp_1$  (17) and the analog inverter  $inv_1$  (18).

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Telescopic op-amp (HL 3 - HL 4): Fig. 16b shows all functional blocks recognized on levels 3 and 4 with Alg. 2. The algorithm first recognizes the differential pair as simple non inverting first stage transconductance  $tc_1$ . For the load recognition, the drain nets of  $P_3, P_4$  are used.  $P_3, P_4$  form the gate connected couple part of the cascode differential pair  $cdp_1$ . Two load parts are found: The gate connected couple forms the load part with p-doping. The load part with n-doping consists of the current mirror  $cm_5 = \{ts_{n,1}, ts_{n,2}\}$ . As stage bias, the current bias  $cb_2$  is found as it is connected with its drain to the source of  $tc_1$ . With it, all parts of the non-inverting first stage  $a_1$  are recognized. In the next step, Alg. 2 checks if the inverter recognized on level 2 is a second stage. This is true, as  $P_6$  was recognized as current bias  $cb_3$  and  $ts_{n,3}(N_5)$  is connected with its gate to one output of the first stage. Because the first stage does not

stage with voltage bias as stage bias. The voltage and current biases not part of the two amplification stages are recognized as circuit bias  $b_O$ . The recognition ends by identifying the capacitor in the circuit as compensation capacitor.

fulfill the criteria of a symmetrical op-amp, it is not searched for an inverting

Symmetrical op-amp with an additional inverting stage: Fig. 2 shows the results of the functional block analysis for a symmetrical op-amp with an additional inverting stage  $a_3$ . During the recognition of the inverting stages, first  $inv_2$  is recognized as inverting second stage  $a_{2,1}$ . Afterwards  $a_{2,2}$  is recognized,  $a_1$  fulfills the condition of a first stage of a symmetrical op-amp and with  $a_{2,1}$ , the needed second stage with current bias as stage bias is given (36). The transistor stack  $\{nt_4(P_3), nt_6(P_5)\}$  fulfills the definition of a non-inverting transcon-

ductance  $tc_{2,2}$  (23).  $vb_2$  is the stage bias with voltage output. The gate-gate connection to the stage bias of  $a_{2,1}$  is given. Note, that for a correct identifica-



Figure 17: Folded-cascode op-amp with CMFB

tion of  $a_3$  the exact definition of an inverting stage must be used (34). As  $P_7$  has a gate connection to one output of the first stage, a drain of the differential pair, it is considered as possible inverting transconductance of another second stage.

- As for this transconductance, no stage bias exist because  $N_6$  is not of type bias, it is not recognized as transconductance. Instead, after  $a_{2,1}$  is recognized,  $N_6$ is identified as inverting transconductance, because it has a connection to an output of  $tc_{2,2}$ .  $P_7$  is its stage bias.
- Folded-cascode op-amp with CMFB: Fig. 17 shows the results of the functional block analysis in a folded-cascode op-amp with CMFB. The four load transistors  $P_1, P_2, N_7, N_8$  are externally biased by the pins Vb1 and Vb2 respectively. Hence, these four transistors are not recognized as current biases (Fig. 17a) as they are not connected with their gates to a voltage bias. However with Alg. 3, they are still recognized as part of the load (Fig. 17b).  $P_6$  is also
- <sup>390</sup> neither identified as current nor voltage bias as it does not have any gate-gate connections to a another transistor with same doping. However, it fulfills the functional definition of a load as it has a drain-drain connection to  $tc_{CMFB}$ . Therefore, it is recognized with Alg. 3 correctly even if it does not fulfill the definition of a load entirely (24).
- Three-stage op-amp: Fig. 18 shows the results of the analysis for a threestage op-amp. Two analog inverters  $inv_1, inv_2$  are recognized on HL 2 (Fig. 18a). One of the transistors  $N_5$   $(inv_1)$ ,  $P_7$   $(inv_2)$  is identified to be part of a current mirror. The other transistor  $P_6$   $(inv_1)$ ,  $N_6$   $(inv_2)$  is not part of any



Figure 18: Three-stage op-amp

additional functional block on HL 2. After recognizing the first and second stage with Alg. 2, the third stage is recognized (Fig. 18b). With the gate of  $N_6$ connected to the drain of  $N_5$ , the input of third stage is connected to the output of the second stage (34).  $P_7$  is a identified current bias. Hence,  $inv_2$  fulfills all criteria of a third stage. Alg. 2 ends by identifying the compensation capacitors  $c_{c,1}, c_{c,2}$ . Both capacitors a connected between the output of two stages,  $c_{c,1}$ between the output of first and third stage,  $c_{c,2}$  between second and third stage.

Hence, both capacitors fulfill (38).

## 9. Application of the Hierarchical Functional Block Decomposition Method

Two applications of the functional block decomposition method are pre-<sup>410</sup> sented: A sizing method (Sec. 9.1, details in [2]) and a structural synthesis method (Sec. 9.2, details in [3]).

## 9.1. Application to Circuit Sizing

The common manual design process is based on analytical equations as described in [17, 18, 19, 20, 21]. For each functional block described in Secs. 3 -6, a behavior model can be derived based on these standard equations resulting in a hierarchical performance equation library (HPEL) [2]. For the functional blocks on HL 3, the equations part of the library describe, e.g., the input and output conductance  $(gin_{fb_k}, gout_{fb_k})$  of a functional block  $fb_k$ . Following equation for instance holds for the output conductance  $gout_{fb_k}$  of a functional block consisting of one or two transistor stacks  $ts_k$ :

$$gout_{i} = \begin{cases} gd_{t_{k,out}}, & \{t_{k,out}\} = ts_{k} \subseteq fb_{k} \\ \frac{gd_{t_{k,out}}gd_{t_{k,supply}}}{gm_{t_{k,out}}}, & \{t_{k,out}, t_{k,supply}\} = ts_{k} \subseteq fb_{k} \end{cases}$$
(40)

 $gd_{t_{k,j}}, gm_{t_{k,j}}$  are the output und input conductance of a transistor in  $fb_k$  with j giving the position of the transistor in the transistor stack. There are exceptions to this equation which are discussed in [2].

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An equation for the output resistance  $R_{out,n}$  of an amplification stage functional block  $a_n$  on HL 4 is developed based on (40) and the *m* functional blocks of the stage connected to the output net of the stage. These functional blocks can be stage biases, load parts and transconductances.

$$R_{out,n} = \frac{1}{\sum_{j=1}^{m} gout_{fb_j}} \tag{41}$$

This equation is part of the equation describing the open-loop gain of a stage  $A_{D,n}$  which is on the same hierarchy level in the HPEL:

$$A_{D,n} = gin_n \cdot R_{out,n}; \quad A_{D,0} = \prod_{n=1}^{l} A_{D,n}$$
 (42)

with  $gin_n$  the input conductance of the stage. The open-loop gain equation of the overall op-amp  $A_{D,0}$  is part of HL 5 of the HPEL. l is the number of all stages in the op-amp,

Analogously, performance equations for all functional blocks that have been <sup>420</sup> presented in Sec. 3 - Sec. 6 have been established [2]. After a functional block analysis of a given op-amp topology according to the methods presented in the paper, the corresponding performance equations of the functional blocks are automatically composed forming a behavioral model of the op-amp performance. This model forms a Mixed-Integer Non-linear Programming problem (MINLP)

Table 1: Results of the sizing method for the telescopic op-amp Fig. 16

(a) Performance values; M: sizing method; S: simulation

Constraints	Spec.	Μ	S
Gate-area $(10^3 \ \mu m^2)$	$\leq 15$	5.8	-
Quiescent power (mW)	$\leq 10$	5.8	6.1
Max. common-mode input	>3	3.3	4.4
Voltage (V) Min_common-mode input	_		
voltage (V)	$\leq 2$	0	0.1
Max. output voltage (V)	$\geq 4$	4.5	4.5
Min. output voltage (V)	$\leq 1$	0.3	0.2
CMRR (dB)	$\geq 90$	130	146
Unity-gain bandwidth (MHz)	$\geq 7$	10	7
Open-loop gain (dB)	$\geq 80$	120	93
Slew rate $\left(\frac{V}{\mu S}\right)$	$\geq 15$	28	22
Phase Margin (°)	$\geq 60$	60	67

Variable	Value $(\mu m/pF)$					
$W_{P_{1,2}};L_{P_{1,2}}$	172;9					
$W_{P_{3,4}}; L_{P_{3,4}}$	27;4					
$W_{P_5}; L_{P_5}$	247;3					
$W_{P_6}; L_{P_6}$	515;3					
$W_{P_{7}}; L_{P_{7}}$	7;3					
$W_{P_8}; L_{P_8}$	7;4					
$W_{P_9}; L_{P_9}$	43;3					
$W_{N_{1,2}};L_{N_{1,2}}$	90;1					
$W_{N_{3,4}};L_{N_{3,4}}$	90;1					
$W_{N_5}; L_{N_5}$	130;1					
$W_{N_{6}}; L_{N_{6}}$	269;1					
$W_{N_{7}}; L_{N_{7}}$	166;9					
	6.4					

(b) Device sizes

<sup>425</sup> for sizing the circuit, which is solved, e.g., with a constraint programming approach [40].

Table 1 shows the results of the sizing method for the telescopic op-amp (Fig. 16) using the specifications given in column 2 of Table Ia. The values calculated with the analytical equations within the sizing method are compared to simulation results using a BSIM3v3 models. The deviations due to the simpler transistor model are less then 30% and within designer expectations.

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## 9.2. Application to Structural Synthesis

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The functional block library (Sec. 3 - Sec. 6) can be applied to structural synthesis by functional block composition. Alg. 4 gives an algorithm to create the structural implementations  $S_{new}$  of a functional block  $fb_{new}$  based on the implementation  $S_1, ..., S_i$  of its subblocks and a set of characteristic connections  $R_c$ . The two-transistor implementations of a current bias (Fig. 5), e.g., are created based on two structural implementation sets  $S_1, S_2$  containing normal and diode transistors of the same doping  $\Phi$  ( $S_1 : NT_{\Phi}, DT_{\Phi}; S_2 : NT_{\Phi}$ ;). Every

combination of  $s_1 \in S_1, s_2 \in S_2$  has a drain-source connection  $(R_c : s_1.d \leftrightarrow s_2.s)$ . Thus, all structural implementations of a two-transistor current bias are created. More complex functional blocks need additional rules set as explained in [3].

Algorithm 4 Synthesis of a functional block

**Require:** Set of subblock implementations  $S_1, .., S_i$ ; Connection rules  $R_c$ 1:  $S_{new} := \{ \} //\text{The set of structural implementations of } fb_{new} \text{ is empty}$ 2: for all  $s_1 \in S_1$  do 3: 4:for all  $s_i \in S_i$  do  $s_{new} := \text{createNewImplementation}(s_1, \dots, s_i, R_c)$ 5: 6:  $S_{new} := S_{new} \cup \{s_{new}\}$ end for 78: ... 9: end for 10: return  $S_{new}$ 

Table 2: Amplification stage composition of the resulting topologies for the specification in Table Ia

First stage type	sim	ple	folded-cascode		telescopic		symmetrical	total	
# stages	1	2	1	2	1	2	-	totai	
# topologies	0	111	0	181	20	77	58	447	

With Alg. 4, the structural implementations of all functional blocks in Secs. 3
- 6 are created allowing a creation of up to 3000 topologies. The corresponding composition graph is presented in [3]. For given specifications, the topologies are sized and evaluated using an enhanced version of the sizing method described in Sec. 9.1. The respective algorithm is presented in [3]. Table 2 shows the output of the synthesis tool for the specifications in Table Ia. As the specifications are not highly demanding and no upper bounds are specified, many topologies are able to fulfill the specifications, e.g. the telescopic op-amp in Fig. 16. Defining more strict specifications reduces the number of created topologies significantly.

#### 10. Conclusion and Outlook

This paper presented a new method to represent op-amps by their functional
<sup>455</sup> block. The functional blocks are ordered hierarchically. For each functional
<sup>block</sup>, a systematic functional and structural description is given allowing an automatic recognition. Two different areas of applications are presented: Together with a performance equation library, the functional block analysis allows a topology-independent sizing of op-amps. A functional block composition
<sup>460</sup> method allows structural synthesis of op-amps. Thousands of different op-amp

topologies are created based on hierarchically generated functional blocks by small rule sets.

Future work remains in including more feedback compensation techniques in the method. Currently, a compensation capacitor is supported in the recognition algorithm. For multi-stage op-amps, additional compensation circuits as, e.g.,

[38, 39] are needed. As they have a fixed structure, the compensation circuits can be added to the method. Future research will also be on including the functional block composition method in layout synthesis.

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