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Microelectronics Reliability 41 (2001) 395–405

MICROELECTRONICS RELIABILITY

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Investigations on double-diffused MOS transistors under ESD zap conditions

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Received 19 December 1999; received in revised form 8 May 2000

Abstract

In this paper we analyzed, through experiments and 2-D simulations, the behavior under high reverse voltages of a double-diffused MOS transistor. It turned out that the drift diffusion region (resistor) between the drain contact and p-diffusion region (PI) plays an important role both in the switching on of the parasitic bipolar structure and in the failure mechanism.

1. Introduction

In bipolar-CMOS–DMOS (BCD) technology for Smart Power ICs the most common device used is the double diffused MOS (DMOS) transistor because it overcomes all the limitations of the pure bipolar IC: in fact it has no driving DC current requirement (limiting power dissipation) and it efficiently works in fast switching conditions [1]. Moreover, as MOS, the current density depends on the geometrical ratio W/L, while in the power bipolar components it depends on the emitter area so that no improvements in density can be obtained from the lithography progress. DMOS transistors are structures in which the channel length is determined by the different rate in the lateral diffusion of two kinds of dopant impurities introduced through the same opening in the poly-silicon layer. Because of that, these structures may have a very short channel length independently from the lithographic step in the used process. A low doped n region (drift region) follows the channel [2]. Many configurations of DMOS transistors are available, dependently on the voltage range they are built for. Our study is targeted at the lateral DMOS transistor for low voltage applications (few tens of volts). A cross-section of a lateral DMOS is pictured in Fig. 1: the thin oxide and the poly-gate are present all along the drift region; p-diffusion (PI) acts as a back-gate.

The subject of this study is the breakdown behavior under high reverse currents of this structure and the relationship between snapback and holding voltage (V_{T1} and V_H) and the layout and process parameters.

2. Experimental results

DMOS transistors have been tested in DC conditions (HP4145). The varied parameters are: poly-length L from 3 to 6 μm, CO–PS (contact to poly-gate spacing) from 3 to 8 μm and width W from 7 to 20 μm (one module with $W = 100$ μm was available too).

In Fig. 2 the effects of the poly-length L variations (3.5, 4 and 4.5 μm) on the DC characteristics are pictured. Source, back-gate and gate contacts are grounded. CO–PS = 3 μm and $W = 7$ μm. From Fig. 2 we can see that:

- V_{T1} (snapback) is around 45 V and I_{T1} is apparently constant (3×10^{-5} A/μm): this suggests that the mechanism leading to the DC snapback conduction mode be current controlled.
- The length of the drift diffusion region (dependent on L) modulates V_{T1}.

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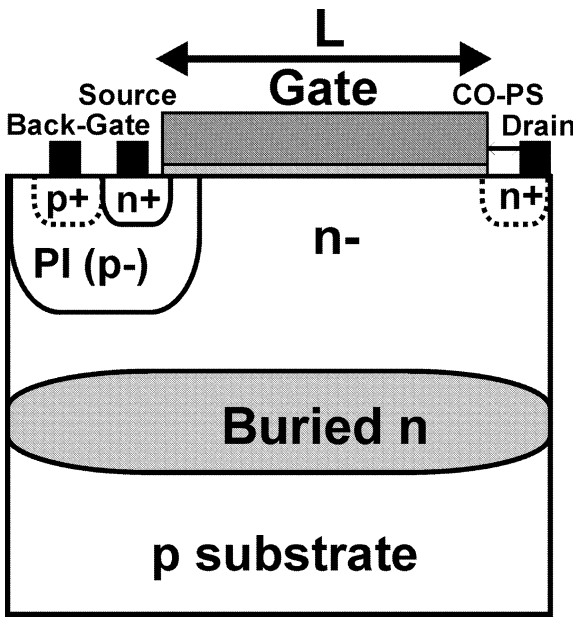


Fig. 1. Cross-section of a low voltage DMOS transistor.

- V_H is around 40 V for all the structures: the snapback swing is very limited in voltage and this might be attributed to the poor beta of the parasitic bipolar structure associated to the device. Such a large V_H causes a considerably high Joule power dissipation.
- V_{T2} is around 50 V with an I_{T2} constant for all the structures (1.3×10^{-4} A/μm); the DC performances look poor likely as a consequence of the high V_H.

In Fig. 3 the effects of the contact to poly-gate CO–PS spacing variations (3, 5, and 8 μm) are pictured. $L = 3$ μm and $W = 100$ μm. It is possible to note that:

- V_{T1} is at the same level as in the previous components, but both I_{T1} and I_{T2} do not scale properly with the increased W (factor 5 instead of expected 14). This suggests that inhomogeneities in the current flow are taking place. The behavior of the device is then moving towards a 3-D dependence, making difficult comparisons with 2-D simulations.
- The drop in voltage at the snapback is only perceptible leading to an even higher V_H which might explain the not perfect scaling of the devices with the width.
- The extra resistance due to the increased CO–PS spacing does not improve the DC performance at all.

In Fig. 4 the effects of the width W variations (7, 10 and 20 μm) are shown. CO–PS = 3 μm and $L = 4$ μm. The measurements indicate:

- V_{T1}, V_H, V_{T2} do not significantly change with W.
- I_{T1} and I_{T2} do not scale as expected with the increased W (30% instead of factor 2): this confirms the presence of inhomogeneities in the current flow.

3. Simulation approach

As previously mentioned, the studied devices are very large structures: CO–PS spacing in the order of 5 μm and gate length of 6 μm are usual values and, therefore, the length of the entire structure can easily exceed 20–25 μm. This fact together with the complexity of the structures would impose computationally prohibitive meshing when simulating. Furthermore, the background available in the literature about these devices is very poor. For this reason we adopted an approach addressed to scale down the device into a "virtual device" rigorously keeping fixed the process features (doping profiles and sheet resistance): in this way the main physical phe-

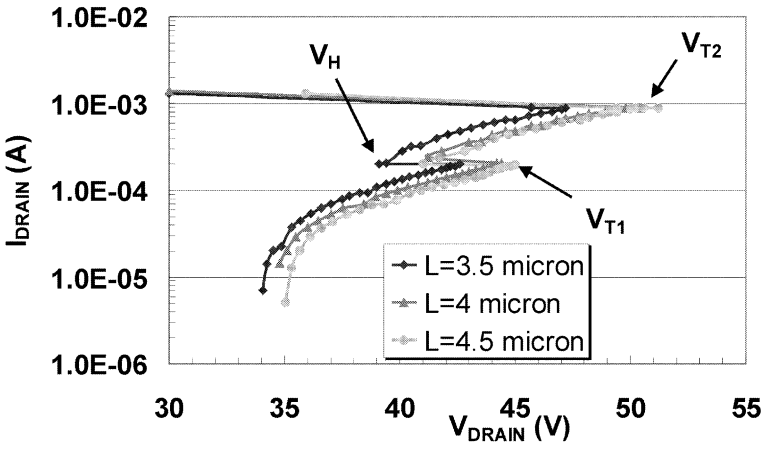


Fig. 2. Measured $I(V)$ DC characteristics of DMOS with $W = 7$ μm, CO–PS = 3 μm and L variable.

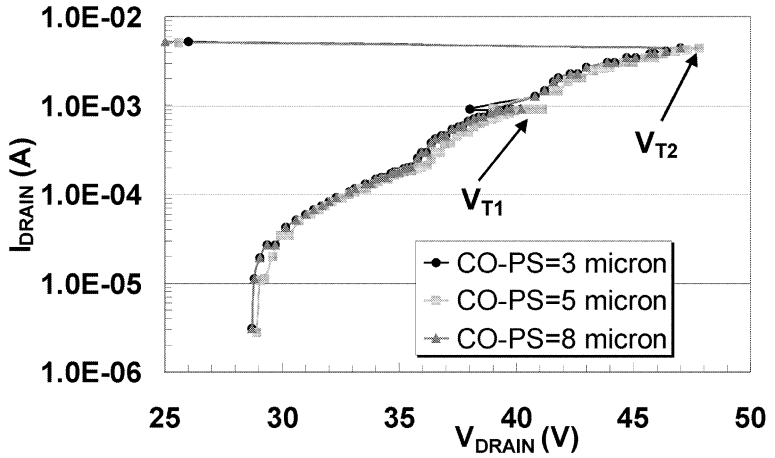


Fig. 3. Measured $I(V)$ DC characteristics of modules with $W = 100$ μm, $L = 3$ μm and CO–PS variable.

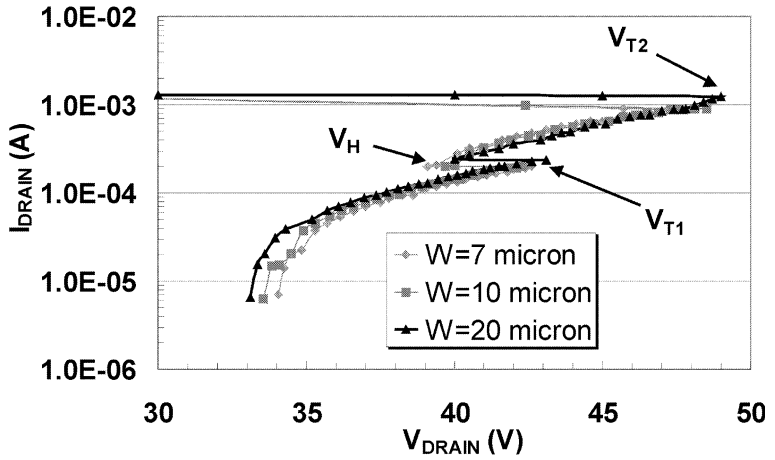


Fig. 4. Measured $I(V)$ DC characteristics of DMOS with $L = 4$ μm, CO–PS =3 μm and W variable.

nomena taking place during high reverse voltages do not change, even if the results obtained will underestimate the ones from the real structure. The structures have been designed with a Device Editor implemented in Silvaco 2-D/3-D simulation tool [3]. The main advantages of this choice are:

- The possibility of analytically defining doping profiles and process/layout features even with unlikely parameters in order to get insight on the behavior of the structure.
- Meshing optimization based on the same mesh parameters: this is important when comparing structures with layout variation [4].

Most simulations are performed "cold" because our main interest is not the second "thermal" breakdown but the mechanisms modulating the first breakdown and the holding voltage. A simulation taking into account lattice temperature will be shown also. The simulated structures (with reference to Fig. 1) have an high resistive p-substrate ($N = 3 \times 10^{13}$ cm^{-3}), a buried N between the drift region ($N = 5 \times 10^{14}$ cm^{-3}) and the substrate, a back-gate contact on the p-region which may be tied together with the source contact, minimum CO–PS distance, a channel length of about 0.25 μm, minimum bulk–source implant distance and 0.7 μm gate length. On this structure (which, from now on, we will refer to as "standard") we simulated some variations, both layout (drift region length and CO–PS distance) and process (epitaxial layer doping and p-profile).

4. Simulation results

The simulated I/V characteristics with all the electrodes grounded (except the drain contact) is shown in Fig. 5: V_{T1} is 11 V and V_H about 4 V. Notice that the

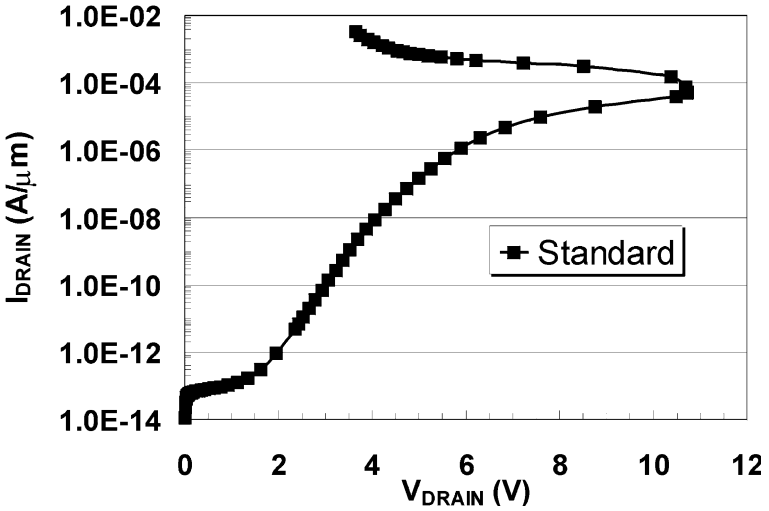


Fig. 5. Simulated DC $I(V)$ characteristics of the "standard" device.

current density at which the snapback occurs ($I_{T1} = 4 \times 10^{-5}$ A/μm) is approximately the same we obtained for a measured similar structure (Fig. 2). Notice also that the simulated V_{T1} is reduced of a factor 4–5 with respect to the measured similar structure: this factor is the same existing between the simulated and the real drift region length. In fact, as we will show ahead, the voltage mostly drops across the drift diffusion region, leading to a voltage scaling with its length.

The first variation we experimented is the drift region length (and, consequently, the poly-length, but the channel length is still unchanged) keeping constant its doping level. As pictured in Fig. 6 the drift region length modulates the snapback voltage but the current density at which the snapback occurs is unchanged.

This result, in spite of the difference in the magnitude of the voltages involved (because of the different geometry), is the same we obtained from real devices measurements (Fig. 2). The relationship between the drift region length and the snapback voltage has been investigated in previous work [5] about the breakdown characterization of N-well resistors: this might suggest that the driving mechanism for the snapback of the entire structure is the breakdown of the drift region resistor.

In N-well resistors the snapback is the consequence of the electric field localization at n^+/n^- diffused junction

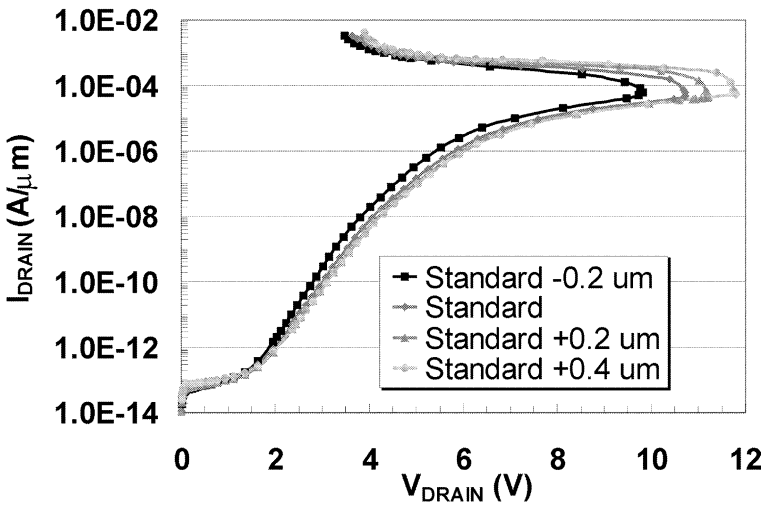
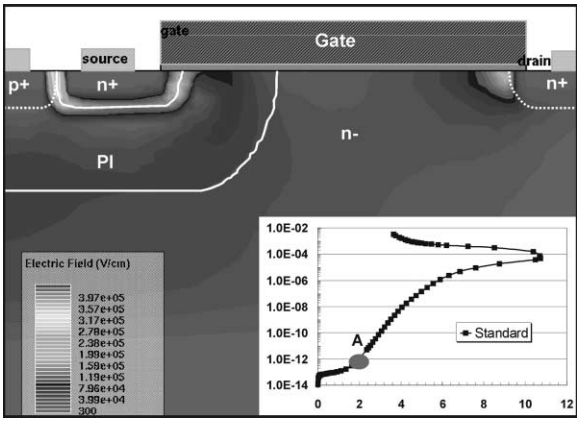


Fig. 6. Simulated effect of changing drift region length.

(anode/N-well) because of the N-well avalanche under high current conditions: the more holes are produced by impact ionization, the more the electric field becomes confined into a smaller region close to n^+/n^- junction, keeping its peak almost constant. This implies a reduction of the voltage and is externally seen as a snapback: note that this mechanism is current controlled because we need a production of minority carriers in the order of background doping of the N-well to alter the integrated electric field in the Poisson equation. The localization of the electric field is shown in Fig. 7 in which its values are pictured for different biasing points (A, B and C). At the point A (low current) there are two main components of the electric field: one due to the built-in voltage across n^+/p^+ source/back-gate contact and an other one behind the drain corner under the gate oxide edge. This component is always present and it is due to the depletion of the diffused junction n^+/n^- when a positive potential is applied to the drain while the gate is grounded. When the device reaches the holding voltage (at the point D, Fig. 8) the electric field is completely confined near the n^+/n^- junction.



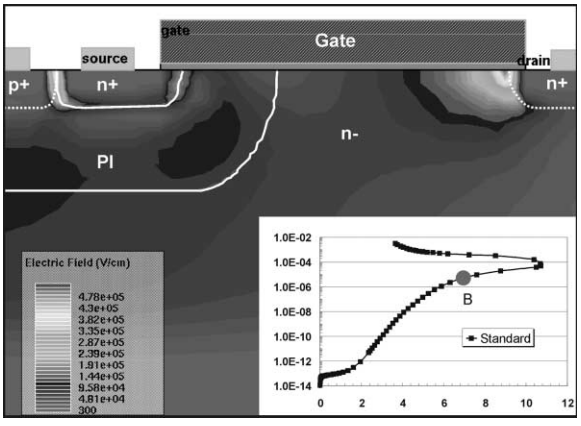


Fig. 7. Simulated electric field in the DMOS at different biasing points (A, B and C).

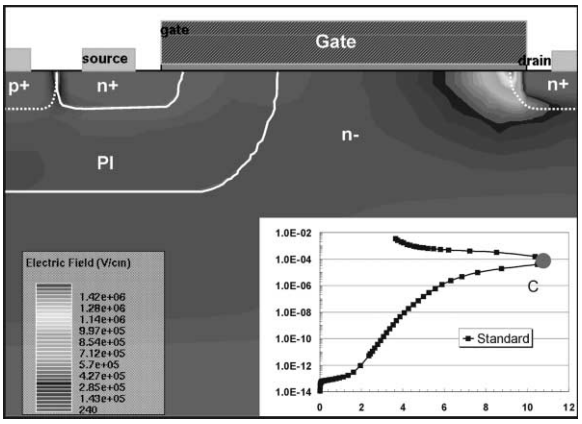


Fig. 7 (*continued*)

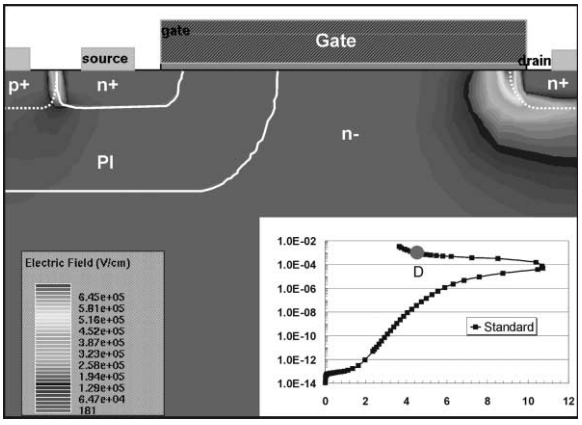


Fig. 8. Simulated electric field at point D.

It is important to remark that in this particular structure the electric field confinement may also be viewed as the Kirk effect in the lateral parasitic bipolar structure ($n^+/p^-/n$(epi)/n^+): this effect takes place in bipolar transistors with a lightly doped epitaxial collector region, under high current injection condition, in which the high field region is relocated from the n(epi)/p(base) region to the n/n^+ (collector contact) diffused junction.

This is a current controlled mechanism too (in this case from the PI/n^- junction avalanche) that takes place when the collector current requires more electrons than available through the doping [2]. Kirk effect has been found to be responsible for performance limitations in similar lateral DMOS devices [6]. To estimate the current required to initiate the Kirk effect we can make use of [2]:

$$J_{\mathrm{Kirk}} = qN_{\mathrm{Drift}}v_{\mathrm{Sat}}$$

Table 1
Calculated values for the onset of Kirk effect

N_{Drift} (cm^{-3})	J_{Kirk} (A/cm^2)	I_{Kirk} (A/μm)
1e15	1.6e3	3.2e−6
5e15	8e3	1.6e−5
1e16	1.6e4	3.2e−5

By considering a junction area of 2×10^{-9} cm^2 (depth $=2 \times 10^{-5}$ cm and width $= 10^{-4}$ cm – 2-D simulations are normalized to 1 μm width) we obtain the currents required to initiate the Kirk effect as reported in Table 1.

With reference to Fig. 9, the higher the carriers availability the earlier the onset of the Kirk effect is reached, leading to a reduced snapback voltage.

It should be also noted that the drain induced barrier lowering (DIBL) effect might play a role in the enhancement of the leakage current before the Kirk effect takes place. This effect manifests itself with the effective reduction of the channel length by increasing the drain voltage: the drain depletion region moves closer to the source depletion region, resulting in a significant field penetration from the drain to the source.

Due to this field penetration the threshold voltage is lowered, resulting in increased injection of electrons by the source over the reduced channel barrier, giving rise to increased drain current [7]. In Fig. 10 the effect in the I/V characteristics of changing the channel length (through the analytical definition of the back-gate junction lateral spreading) is shown: the enhanced leakage for short channel length as a result of threshold voltage reduction due to the DIBL effect is clearly seen.

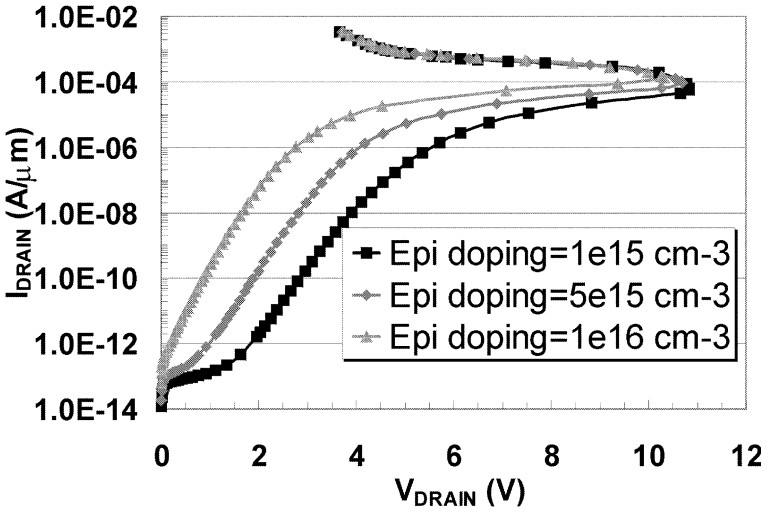


Fig. 9. Simulated effect of changing drift region doping.

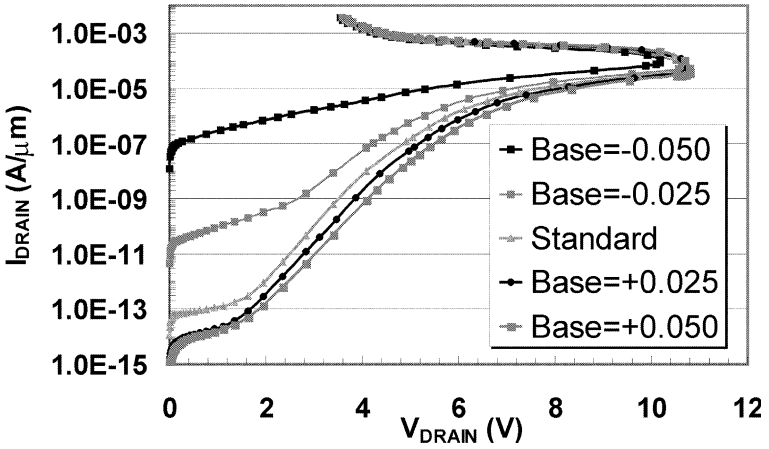


Fig. 10. Simulated effect of changing channel (base) length through definition of lateral junction spreading.

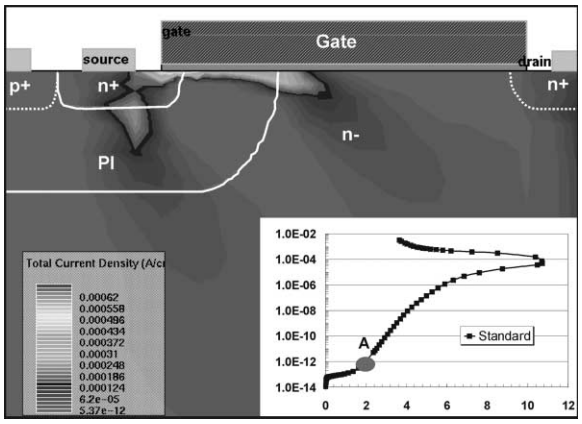


Fig. 11. Total density current at point A.

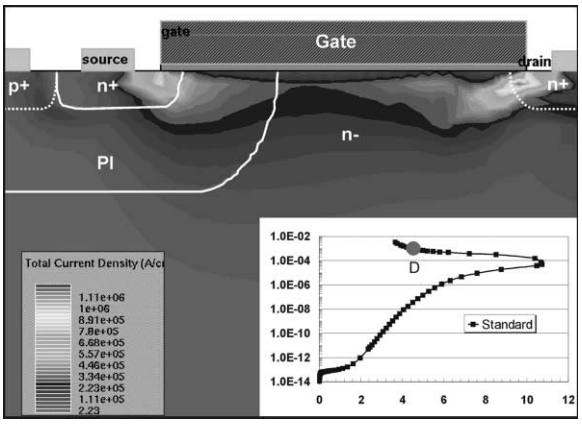


Fig. 13. Total density current at the point D.

Moreover, a decreased channel (base) length results in a reduced snapback voltage because of the increasing of the beta associated to the bipolar structure.

To investigate the behavior of the parasitic bipolar structure associated to the device under study, we analyzed the current at different biasing points. At the point A (Fig. 11) a small current is flowing along the channel. At the snapback point (Fig. 12) the holes current in the back-gate contact direction is large enough to locally bias the base/emitter (source/back gate) junction.

Finally the bipolar parasitic structure is switched on (Fig. 13, in which it is possible to note the relevant base current at the holding voltage confirming the lateral parasitic bipolar action). Summarizing the results so far presented, with reference to the simulated DC I/V characteristics shown in Fig. 5, for low voltage level there is the leakage of n^-/p^- junction that might be enhanced by DIBL effect. For higher current injection levels, because of the PI/n^- junction avalanche, Kirk effect takes place resulting in a relocation of the electric field (and, ultimately, of the drift region/PI junction) close to the n^-/n^+ region. When in this region the electric field is large enough to cause impact ionization there is a production of electron–hole pairs: electrons are collected at the drain contact and holes are traveling towards the p^+ contact increasing the voltage drop across the back-gate region, resulting in the biasing of the base of the lateral parasitic structure which is fully turned on once the holding voltage is reached.

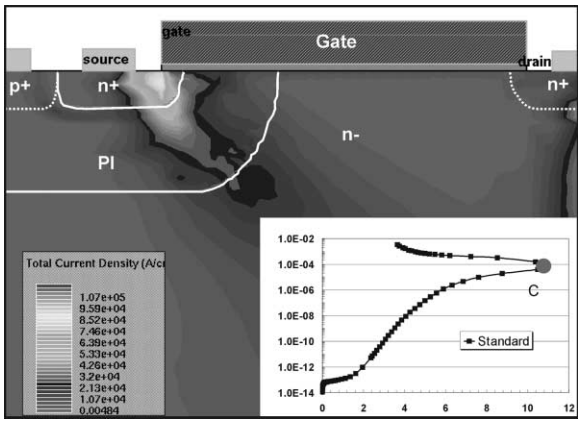


Fig. 12. Total density current at the snapback (C).

In Fig. 14 the electron concentration along a vertical cross-section in the channel (surface = 0, junction depth = 0.2) is shown: it indicates the conductivity modulation of the base region because of the electrons injected, via the channel, into the drain. Furthermore we simulated the application of a voltage on the gate electrode (technique often used with capacitative coupling to lower V_{T1}). The results are reported in Fig. 15: as we expected, the snapback voltage decreased with the increasing of the applied voltage [8]. In fact the mobile charge induced by the MOS action reduces the need of current to switch on the parasitic structure and, then, reducing the snapback. In addition, the application of a gate voltage reduces the electric field in the y-direction caused by the n^+/n^- junction depletion due to the positive potential at the drain contact: therefore the Kirk limit is higher and the current at which the snapback occurs is higher.

In the layout of the standard DMOS transistor we moved the bulk contact away from the source contact to verify the effect of increasing the value of external base region resistance.

The results are pictured in Fig. 16 showing a small decreasing in the snapback voltage because less base current is necessary to forward bias the source/back gate junction.

Moreover we investigated on the effects produced by the changes in the CO–PS (contact to poly-spacing) distance. In protection structures for CMOS

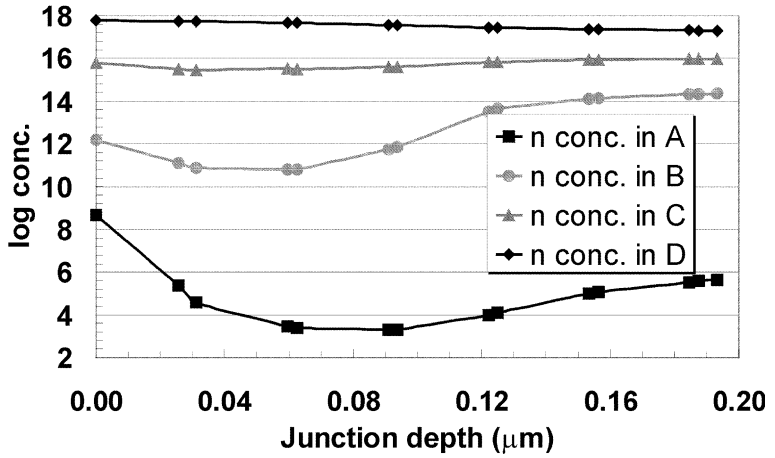


Fig. 14. Electrons density for different biasing points (defined in Figs. 7 and 8) along a vertical cross-section in the channel (surface = 0; junction depth = 0.2).

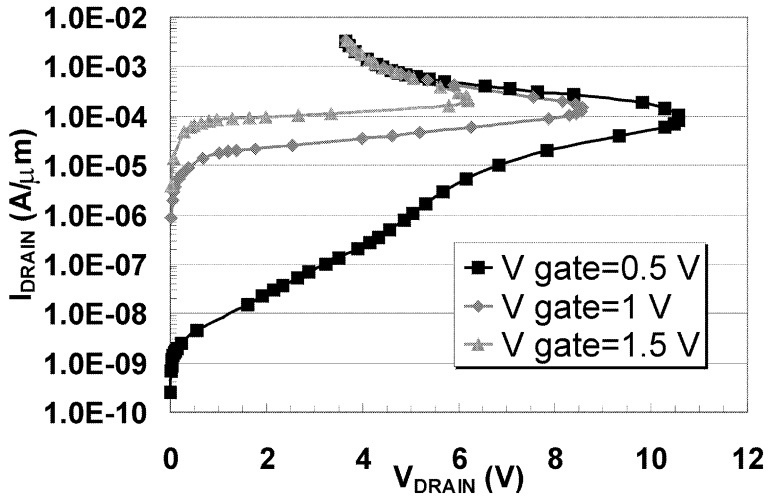


Fig. 15. Simulated effect of applying a gate voltage.

technologies (usually ggnMOSt) this parameter is known to play a critical role in the performances of the structure [9].

Conceptually it consists of an extra resistor at the drain which enables the spreading of the stress current, "slowing down" the filamentation phenomenon: this means a better current sustaining capability before reaching the second "thermal" breakdown which leads to an irreversible damage of the structure. Unfortunately this phenomenon has got a typical 3-D symmetry and, therefore, our 2-D simulations were not able to prove any current constriction phenomenon: the results are shown in Fig. 17 and are on the same track for what we already concluded about the increasing of the drift resistive region (snapback voltage modulated from the increased resistivity). In particular, the snapback voltage modulation is very small because the largest voltage drop is located in the drift diffusion region.

So far we have performed "cold" simulations for the above mentioned reasons: as last step we took into account thermal boundary conditions and solved the lattice temperature too. The I/V characteristics (Fig. 18) does not change until Joule dissipated power is strong enough to cause self-heating effects and create deviations from the purely electrical characteristics.

It is interesting to note the distribution of the lattice temperature in the marked biasing point: the temperature peak (Fig. 19) is located in the n^+/n diffused junction region where the dissipated Joule power (Fig. 20) has a maximum.

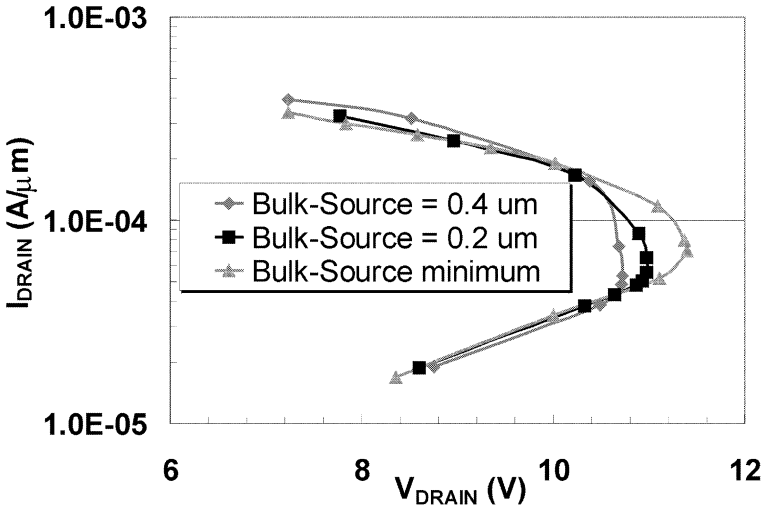


Fig. 16. Simulated effect of changing bulk–source distance.

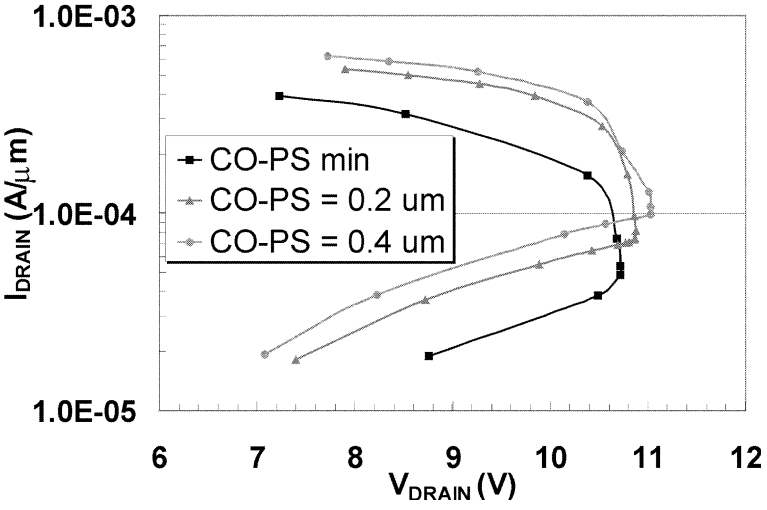


Fig. 17. Simulated effect of changing CO–PS distance.

The last two results confirm the importance of this region not only for the breakdown behavior but also for the perspective in the ESD maximum sustaining current capability. Therefore damage after a destructive ESD stress is expected to be located in this zone. To verify this prediction we took different pictures of the damaged area of the devices just after they were broken: all pictures look like Fig. 21. A large spot between the drain contact and the gate edge is apparent.

In particular, in Fig. 22, a deprocessed DMOS after a destructive stress is pictured: some spots from the gate edge to the drain contacts are well visible. In both cases the only part involved in the failure is the drain side.

5. Conclusions

For the behavior of low voltage DMOS transistors under high reverse voltage conditions we found:

- New insights in lateral DMOS behavior.
- The combination of the breakdown at the n^-/n^+ junction (due to a Kirk-like effect initiated by the PI/n^- junction avalanche) and the DIBL effect enable the turn on of the parasitic bipolar structure associated to the device. This is a current controlled mechanism.
- This effect causes a relocation of the electric field near the diffused junction n^+/n^-.

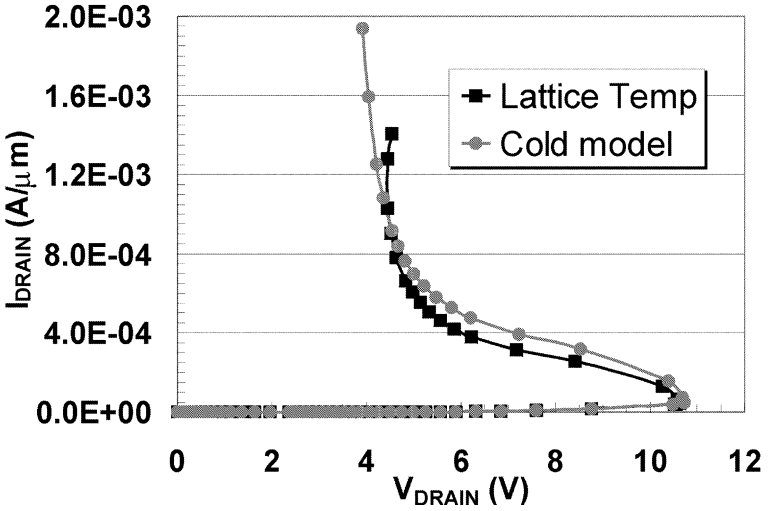


Fig. 18. "Cold" vs. "hot" simulations of DC $I(V)$ characteristics.

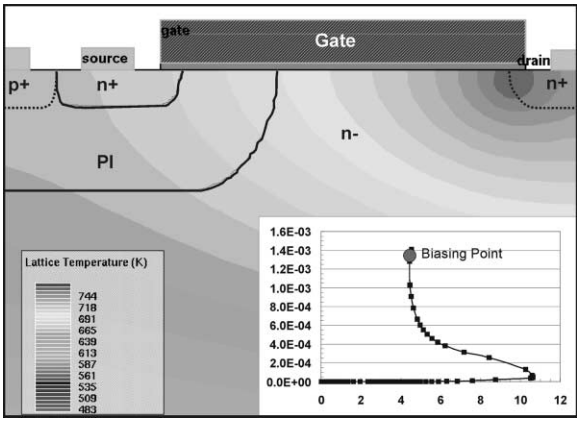


Fig. 19. Temperature distribution in the marked biasing point.

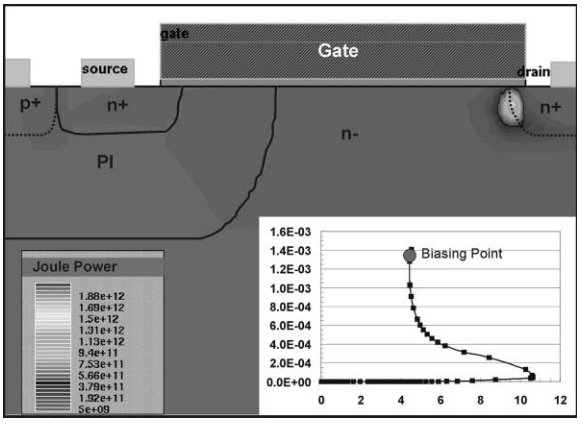


Fig. 20. Joule power distribution in the same biasing point as in Fig. 19.

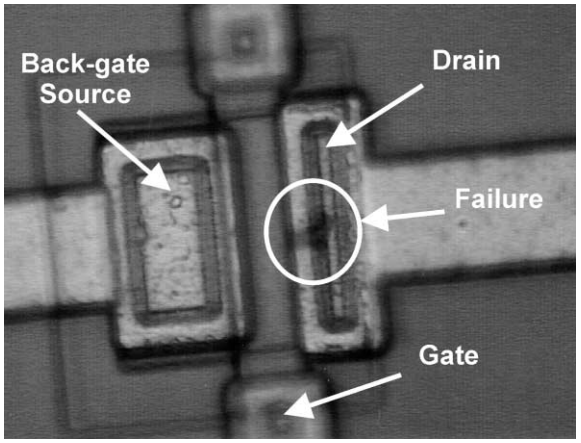


Fig. 21. Damaged area.

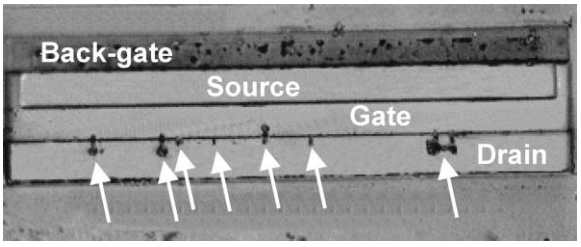


Fig. 22. Picture of a deprocessed DMOS.

- The maximum power dissipated is across n^+/n^- diffused junction and, therefore, here is located the most likely failure site.

- Applicability of the concept of lateral parasitic transistor being turned on after the snapback voltage is reached.
- The snapback voltage can be modulated both by the length of the drain extension (gate length) and by the application of a gate voltage.

Acknowledgements

Huug van der Vlist and Michiel Stoutjesdijk from Philips Semiconductors Nijmegen are gratefully acknowledged for their fruitful contributions. Marcel Hoeven from Philips Semiconductors Nijmegen is acknowledged for his support during the measurements.

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