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# The time-voltage trade-off for ESD damage threshold in amorphous silicon hydrogenated thin-film transistors

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**Abstract**

It is investigated whether damage or breakdown of the amorphous silicon thin film transistors (α-Si:H TFT's) under pulsed stress depends on the stress time. The drain of grounded gate TFT's has been stressed applying repeated square voltage pulses of different duration (100ns to 10s). The evolution and the mechanisms of the pre-breakdown degradation will be presented and discussed. Finally, the temperature distribution across an α-Si:H TFT under applied stress will be simulated by means of coupled electro-thermal simulations.


## 1. Introduction

In our earlier experiments with top-gate amorphous silicon thin-film transistors (α-Si:H TFT's) [1], ESD (electrostatic discharge) robustness was investigated by means of Transmission Line Model (TLM) [2]. It was discovered that under electrostatic discharge stress a degradation of threshold voltage (soft failure) sets in long prior to the electric breakdown (hard failure). It was shown that this pre-degradation is due to creation of states in the amorphous silicon and that is not directly related with the gate dielectric catastrophic breakdown.

In this paper the time-voltage trade off under ESD stress is investigated in order to give an in-depth analysis of the ESD effects in TFT's. The conclusions drawn from the experimental are illustrated with help of electro-thermal simulations.

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## 2. Description of experiments

### 2.1. Device description

Amorphous silicon thin-film transistors (α-Si:H TFT) were first proposed for device applications by Le Comber *et al.* in 1979. They operation is very similar to the operation of crystalline MOS transistors. α-Si:H TFT's are nowadays widely used for different applications, such as active matrix addressed LCD's (lap-top computers, monitors, flat-panel TV sets), fingerprint and X-ray image sensors etc.

TFT's used in the experiments are top-gate (staggered) symmetrical α-Si:H TFT's with a nitride gate insulator (Fig. 1). To ensure uniformity, before stressing, the TFT's are annealed at 280°C for an hour. A typical operational drain voltage is $V_D \cong 10V$ and a typical operational gate voltage is $V_G \cong 15V$. The typical threshold voltage is $Vt \cong 6V$. Due to the high resistance of amorphous silicon, these transistors have very low gain. The drain current level is very low (~ micro amps). That is acceptable

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for their application is displays, as they are always used as switches in an active matrix. The devices used in this experiment were specially designed for testing, with variations of design parameters: channel length (L) and channel width (W).

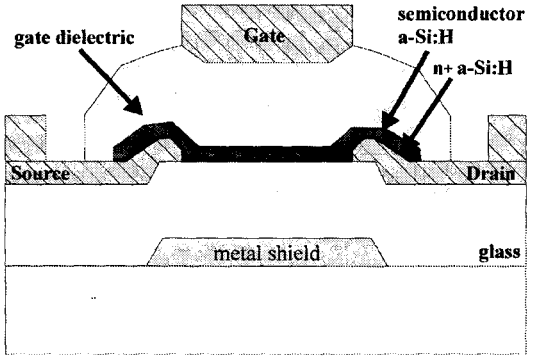


Fig. 1. Cross-section of an a-Si:H TFT

### 2.2. Transmission line model (TLM) set-up

For the experiments with a very short pulse (in order of nano sec), Transmission Line Model (TLM) is used. The TLM set-up was originally designed for the studying of the transient behaviour of electrostatic discharge protection devices for the IC industry [2].

Our TLM set-up is built using a high voltage generator that produce the stress bias, a transmission line that determines the time delay and a digital oscilloscope DSO HP 54710A and a Parameter analyzer HP4145B, which are used to monitor the device under stress during and after stressing. For data acquisition, graphical measurement control software ("veetest" of Hewlett-Packard) is used. The TLM set-up is shown in Fig. 2.

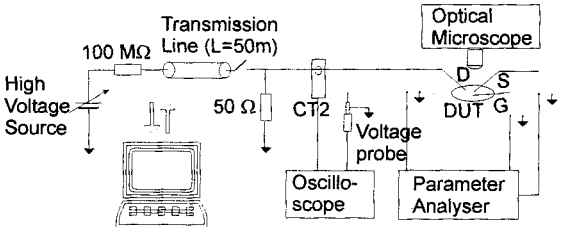


Fig. 2. Schematic of TLM set-up

### 2.3. Experiments

The drain of the TFT's was stressed with high voltage square pulses. The voltage was increased in steps up to breakdown. Short voltage pulses with lengths variations from 100ns to 1μs were applied using TLM with different transmission line lengths. For pulses with lengths varying from 0.4s to 10s a standard semiconductor parameter analyzer HP4145B with a voltage expander was used to stress the transistors (for convenience called Long pulse stress). For Long pulse stress the maximum voltage was limited by equipment to 200V. During stress the drain current and voltage are measured and after each stress pulse the transfer characteristic ($V_d$=0.1V) was measured.

Stress was, in both cases: TLM and Long pulse, applied on the drain of TFT's, while gate and source were grounded. From measured $I_D(V_D)$ characteristics during TLM zap, we observed that voltage measured on the drain monotonously increases under TLM stress. It shows that during testing a TFT transistor is not active in the snapback mode, unlike standard Si MOS devices.

## 3. Analysis of experimental results

### 3.1. Breakdown voltage over time

Breakdown voltages ($V_{bd}$) have been measured for all TFT's with different W/L's under 100ns, 300ns, 500ns and 1μs TLM stress. In Fig. 3 the breakdown voltages measured for TFT's with the same W/L (=18/9) on the same glass after different pulse lengths is plotted versus the pulse lengths. Fig. 3 does show differences in $V_{bd}$ for different pulse lengths. The average curve is not introduced for the clarity of results.

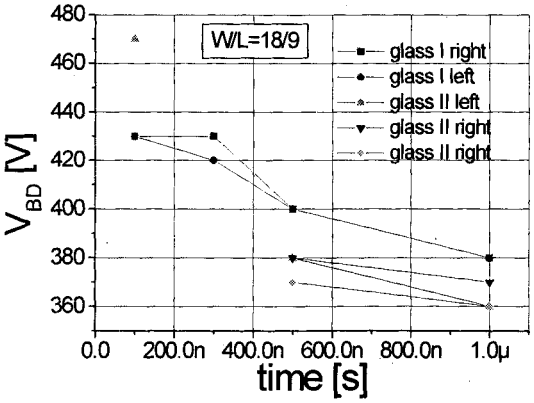


Fig. 3. Breakdown voltage after pulsed stress with different pulse duration

For TFT's with W/L=100/6 and W/L=100/4, which have much lower breakdown voltage because of their shorter channel [1] then the standard TFT's,

breakdown voltage was monitored under both TLM and Long pulse stress. For these two TFT's, $V_{bd}$ of 150V and 110V, respectively, were measured after 1s Long pulse stress. After the TLM stress, breakdown voltages of ~280V and ~200V, respectively, were measured. Thus the same dependence in breakdown voltage vs time is found between pulse lengths ranges of 100ns-1μs and 0.4s-10s. The slope of the breakdown voltage decay on the time scale 100ns-10s is found to be linear and constant until the point when thermal equilibrium is established and is expected that breakdown voltage curve enters the steady state part.

The conclusion of all experimental data could be drawn that breakdown voltage depends on the pulse duration. It is due to the energy consumed at TFT, as explained by the Wunsch & Bell model [3]:

$$E = \int_0^t I(t)V(t)dt \qquad (1)$$

Though the current in TFT under square voltage pulse proves to be not constant in time (it increase with time), we could assume from (1) that $V_{br}$ lowers if the pulse length of applied stepped voltage stress increases. The power-density-dependant failure of amorphous silicon TFT was previously investigated in [4] in range 1-10msec.

### 3.2. Pre-breakdown degradation analysis

Transfer characteristics $I_D(V_G)$ of TFT's with W/L=18/9 are measured between each two ESD stress pulses in order to follow development of degradation of TFT parameters such as threshold voltage, subthreshold slope and transconductance. On one glass sample TFT's were stressed with TLM and on another sample TFT's were stressed with Long pulse stress. At the first glance, the measurements data shows that pre-breakdown degradation starts sooner under Long pulse stress.

Fig. 4a and 4b show the threshold voltage ($V_t$) shift monitored during TLM and Long pulse stress, respectively. $V_t$ is given by the intersection of the slope of the linear transfer characteristic with the x-axis.

Fig. 5a and 5b show the transconductance ($g_m$) degradation after TLM and Long pulse stress, respectively. The transconductance is defined as:

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{W}{L}\mu C V_{DS} \qquad (2)$$

Fig. 6 shows the subthreshold slope (S) degradation after TLM and Long pulse stress. S is given by:

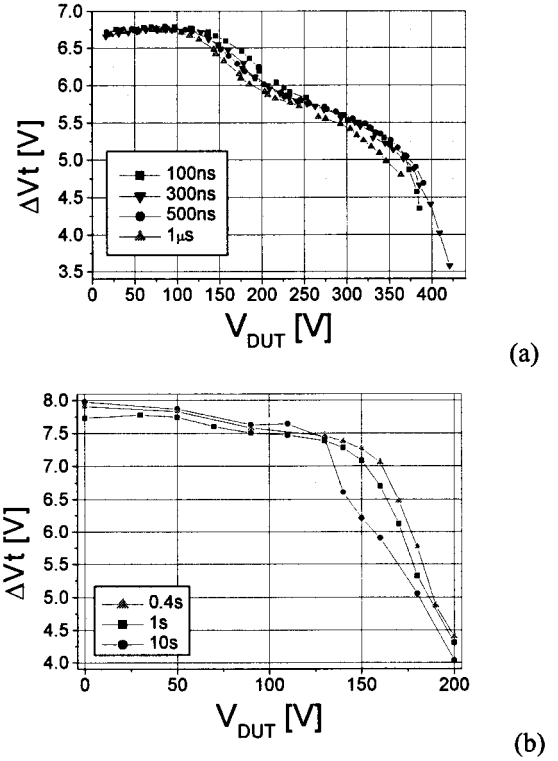


Fig. 4. Threshold voltage shift during (a) TLM stress and (b) Long pulse stress

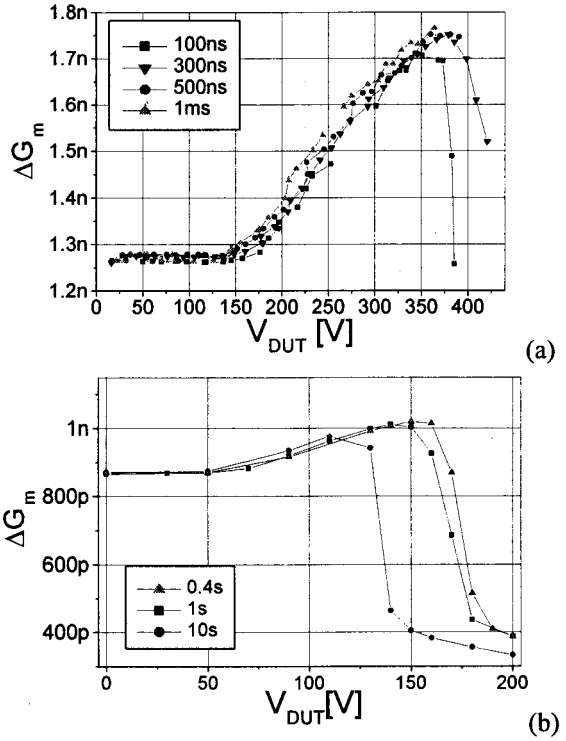


Fig. 5. Transconductance shift during (a) TLM stress and (b) Long pulse stress

$$S = \frac{\partial V_G}{\partial(\log I_D)} \quad (3)$$

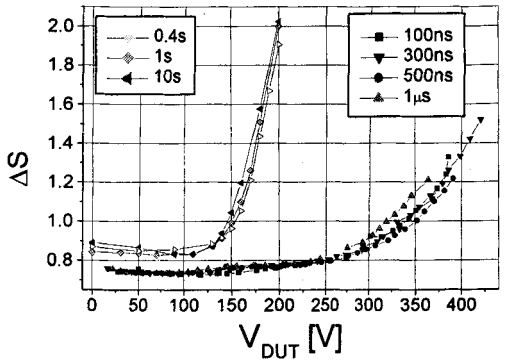


Fig. 6. Subthreshold slope shift during TLM stress and Long pulse stress

Table 1a gives an overview of the data shown in Fig. 4, 5 and 6 e.g. the degradation behaviour of $V_t$, $g_m$ and S in different voltage regions for 300ns TLM stress and table 1b lists the same for 1s Long pulse stress.

Table 1: Lists of degradation behaviour of Vt, gm and S during different voltage stress regions for (a) TLM stress and (b) Long pulse stress

(a)

| | 10-50 | 50-130 | 130-220 | 220-380 | 380-$V_{bd}$ |
|---|---|---|---|---|---|
| $V_t$ | + | 0 | - | - | same |
| $g_m$ | +/0 | 0 | + | same | -- |
| S | - | 0 | + | + | same |

(b)

| | 0-50 | 50-110 | 110-150 | 150-200 |
|---|---|---|---|---|
| $V_t$ | +/0 | - | - | same |
| $g_m$ | 0 | + | same | -- |
| S | 0/- | 0/- | + | same |

The slight increase in $V_t$ after the first TLM steps is already known as the so-called turnaround phenomenon [5] described by Kaneko et al. In our case, the $V_t$ does not change directly from a positive to a negative $V_t$ shift, but from a positive $V_t$ shift first to a constant $V_t$. At low stress pulses the $V_t$ shift is positive because of state creation close to the conduction band in the a-Si layer. As the voltage stress increases the $V_t$ starts to decrease (>130V). $g_m$ measured after the second TLM pulse is a little higher then the $g_m$ measured after the first TLM pulse. After these first pulses $g_m$ is constant up to a stress voltage of 130V. The $g_m$ starts to increase until the stress voltage reaches 380V, after 380V (just before the breakdown) $g_m$ decreases sharply. The shift of S shows the same dependence as the $V_t$ shift but with opposite sign. Initially S decreases until a stress voltage of 50V, and then S stays constant for a while, until stress voltage of 130Vwhen S starts to increase.

For Long pulse stress the same regions can be identified as with TLM stress, only difference is that they appear earlier, making the threshold of degradation lower. The turnaround phenomenon as seen with TLM stress cannot be identified now, from the reason that the voltage stepping was not as fine as during TLM measurements.

As $V_t$ and S show a similar dependence (with different sign) on the stress voltage it means that the degradation is mostly caused by state creation/removal. There is no evidence that charge trapping is taking place. An explanation for the constant $V_t$, $g_m$ and S region could be given in the following way. Firstly, the positive $V_t$ shift under initial voltage steps is due to filling of the already existing states in amorphous silicon. Afterwards, as gate bias is zero, the current level across the channel is therefore initially low, so that the equilibrium situation in the channel is not excited. Up to 130V the influence of the electric field caused by the drain voltage is not enough to lower the potential barrier between the source and the drain and to degrade $V_t$, $g_m$ and S. Later on, when due to a very high voltage on the drain a large current starts to flow through the channel (basically due to punch-through effect), an accordingly high thermal heating develops. Therefore the current in the channel increases even more being able to create new states in amorphous silicon. As the electric field (close to the interface) in the channel direction is non-uniform [6], it induces a non-uniform distribution of created /removed states. This means that the stress is different in different positions in the channel relative to the drain and source. With each voltage step it widens across the channel [1]. Once again, the turnaround phenomenon has to do with stabilizing/equilibrium processes. The secondary change under higher voltages is due to state creation in α-Si near the interface.

### *3.3. Damage threshold over time*

The pre-breakdown degradation dependency on time is explained through the damage threshold. Damage threshold, a stress voltage under pre-breakdown degradation sets in, was extracted as a voltage for which threshold voltage $V_t$ starts to decrease (Fig. 4). The extrapolated function of the threshold of degradation over stress pulse length is

shown in Fig. 7. Measurements of the damage threshold shown in Fig. 7 involve both TLM and Long pulse measurements.

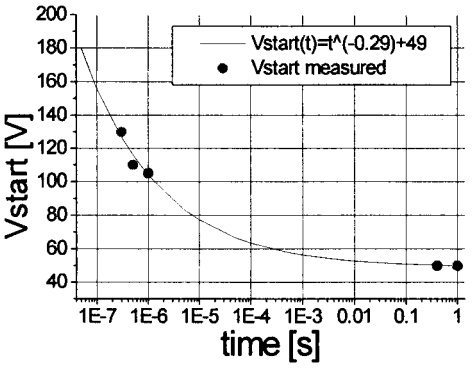


Fig. 7. The time dependence of the degradation presented with points (measurements) and line (descriptive power law curve)

The measured data are approximately described (as the number of data is low for a reliable fitting) by an analytical function, which is based on the formula that describes time dependence of the threshold voltage $V_t$ shift at voltages where states creation dominates, described by a power law, $\Delta V_t \approx a \cdot t^{\beta}$, with $\beta$ about 0.3 to 0.5 [7]. It concurs very well with the measurements, which supports our earlier statement that the secondary degradation of the threshold voltage is due to state creation.

## 4. Transient simulations of heating

It is proved from the experimental data that the pre-breakdown degradation is thermally activated processes. It is also shown how the threshold of the pre-breakdown damage changes with stress time. The question is whether the change of the damage threshold with the change of the stress time is related to the thermal heating. Therefore, the 3D electro-thermal simulations were performed in transient regime. A simulator has been used which translates a thermal model into an electrical equivalent, which in turn can be simulated using an electrical circuit simulator [8]. The stress conditions similar to the one in the experiment ($V_D$=350V, $V_G$=10V, $V_S$=0V, W/L=100μm/20μm) were simulated for variations of the pulse length. The results of the transient simulations are presented here by only one point chosen at the end of the stress pulse, when thermal heating in its peak. The space coordinates of the location for which the results are shown are in the middle of the TFT width, at the drain side, which is chosen as it is the hottest point in the TFT [9].

Fig 8 shows the temperature rise for the stress pulses of different duration. It is shown in Fig. 8 that a certain time, which is in order of an ESD pulse, is needed for establishing a temperature constant in time. After 100 μs the temperature rise in the hottest point (the centrepoint of the channel width at the drain side) is almost of the end of temperature.

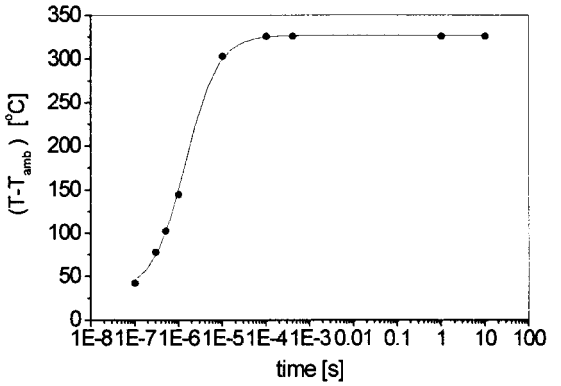


Fig. 8. Simulated temperature of a TFT under ESD stress of different duration.

On another hand, it was previously shown that the pre-breakdown degradation is due to state creation/removal in amorphous silicon, which is a thermally activated process [7]. By performing electro-thermal simulations is confirmed that the function of threshold of degradation over time (Fig. 7) is approximately following the function of temperature establishing in a TFT under high voltage stress (Fig. 8). After the TFT enters thermal equilibrium and constant temperature is established, the function of the threshold of degradation saturates as well.

## 5. Conclusions

An experimental study of the time dependences of the breakdown voltage and the pre-breakdown degradation under a stepped ESD stress is carried out. It is described how both the breakdown voltage and the pre-breakdown degradation process are dependent on the duration of the ESD zap. The dependence of the threshold of degradation with pulse duration was described by a power law and explained by means of electro-thermal coupled simulations. It is also confirmed that pre-breakdown degradation is due to creation/removal of states in the amorphous silicon.

## References

[1] Tošić N., Kuper F.G., Mouthaan T. Transmission line model testing of top-gate amorphous silicon thin film transistors. Proc. of IRPS 2000. (2000) pp 289-294.
[2] Maloney T. J., Khurana N. TLP techniques for circuits modeling of ESD phenomena. Proc. of EOS/ESD Symp. (1985) 49-54.
[3] Dwyer V. M., Franklin A. J., Campbell D. S. Thermal failure in semiconductor devices. Solid State Electronics, Vol. 33, No. 5 (1990) pp. 553-560.
[4] Tada M., Uchikoga S., Ikeda M. Power-density-dependent failure of amorphous-Si TFT. AMLCD Proc. (1996) pp. 269-272.
[5] Tai Y. H., Tsai J. W., Cheng H. C., Su F. C. Anomalous bias-stress-induced unstable phenomena of hydrogenated amorphous silicon thin film transistors. Applied Physics Letters, Vol. 67, No. 1 (1995) pp.76-78.
[6] Kaneko Y., Sasano A., Tsukada T. Characterization of instability in a-Si TFTs. Journ. Appl. Phys., Vol. 69, No. 10 (1991) pp. 7301-7305.
[7] Powell M. J., van Berkel C., Hughes J. R. Time and temperature dependence of instability mechanisms in amorphous silicon thin film transistors. Appl. Phys. Letters, Vol. 54, No. 14 (1989) pp. 1323-1325.
[8] Krabbenborg, B. H. Modelling and simulation of electrothermal interaction in bipolar transistors, PhD Dissertation, University of Twente, The Netherlands, 1994.
[9] Tošić N., Kuper F.G., Mouthaan T. High voltage effects in top-gate amorphous silicon thin film transistors. Mat. Res. Soc. Symp .Proc., Vol. 621 (2000) pp. Q8.5.1 - Q8.5.4.