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Squeeze: Efficient Compact Fractals for Tensor Core GPUs

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Abstract

This work presents Squeeze, an efficient compact fractal processing scheme for tensor core GPUs. By combining discrete-space transformations between compact and expanded forms, one can do data-parallel computation on a fractal with neighborhood access without needing to expand the fractal in memory. The space transformations are formulated as two GPU tensor-core accelerated thread maps, $\lambda(\omega)$ and $\nu(\omega)$, which act as compact-to-expanded and expanded-to-compact space functions, respectively. The cost of the maps is $\mathcal{O}(\log_2 \log_s(n))$ time, with n being the side of a $n \times n$ embedding for the fractal in its expanded form, and s the linear scaling factor. The proposed approach works for any fractal that belongs to the Non-overlapping-Bounding-Boxes (NBB) class of discrete fractals, and can be extended to three dimensions as well. Experimental results using a discrete Sierpinski Triangle as a case study shows up to $\sim 12\times$ of speedup and a memory reduction factor of up to $\sim 315\times$ with respect to a GPU-based expanded-space bounding box approach. These results show that the proposed compact approach will allow the scientific community to efficiently tackle problems that up to now could not fit into GPU memory.

Keywords: Compact Fractals; GPU; Tensor Cores; Thread Mapping; Compact Space;

1. Introduction

Many natural phenomena exhibit fractal like features in their structure, such as vegetation growth [1, 2], terrain formation [3, 4], molecular dynamic patterns [5], blood vessels generation [6], among many other examples. Fractals structures exhibit self-similarity, a property where the whole structure's information is present at different levels of scale. Mathematical definitions of fractal geometry have been formulated in order to model and simulate natural phenomena that cannot be easily explained in terms of traditional Euclidean geometry.

One known approach often employed in parallel simulations is to use a discrete *embedded* representation of the fractal, where it is contained inside a *bounding-box* embedding in expanded form. Although this representation indeed simplifies the mapping of parallel threads onto data elements and the exploration of its neighbors, it sacrifices compute resources as it discards threads that fall outside the region of interest at run-time, as well as memory by having to store the whole embedding instead of just the fractal. Figure 1 depicts an example fractal embedded in a bounding-box.

This parallel resource and memory problem is not specific to just one fractal, but to all discrete fractals handled this way. In particular, here we focus on the Non-overlapping Bounding-Boxes (NBB) class of fractals [7], which satisfies two properties: i) the smallest level of the fractal occupies one unit of discrete space and from that point on, it can only scale up, and ii) each fractal has a unique transition function that takes the fractal in its current scale level, and replicates it in space to generate the fractal at the next scale level. In the NBB class, we assume that replicas can be translated, but cannot rotate neither overlap with each other.

1.1. The two problems with embedded fractals

In the embedded representation, as the fractal gets larger, the number of fractal data-elements will become asymptotically smaller than the number of non-fractal elements (the empty spaces or

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Figure 1: The Sierpiński Carpet embedded in a discrete euclidean domain of 27×27 elements.

holes of the embedding), bringing up two problems:

- **[parallel efficiency]** P1: The number of computational resources (threads from the grid) mapped to the problem will grow in terms of the bounding-box (embedding space), and not in terms of the number of elements of the fractal which is what is actually needed. With small fractals the problem is not so dramatic, but as the fractal grows, this difference between fractal and empty elements gets larger.
- [memory usage] P2: The memory usage will increase in terms of the bounding-box, and not in terms of the fractal, putting a very early limit on the largest problem size that fits in the GPU.

The research question is whether there exists an efficient GPU scheme for solving P1 and P2. To achieve this, the fractal must be processed in its compact form and not in the expanded embedded one. Figure 2 shows an example NBB fractal, with its compact representation below, at each level.



Figure 2: The construction of the empty-bottles NBB fractal.

The challenge is to access the data-parallel neighborhoods efficiently, as these will no longer be Moore or Von-Neumann for every cell. Figure 3 illustrates this difference (the placement of neighbors in compact space is properly explained in Section 3).



Figure 3: A comparison of the neighborhood between expanded and compact space for a cell in the Sierpinski Triangle.

This work presents Squeeze, a tensor core GPU approach capable of doing parallel computations, including stencil-like or nearest-neighbors simulations, on compact NBB fractals. It enables applications such as PDE solvers, cellular-automata, spin-model simulations, among others, to do efficient fractal simulation in compact space, as they rely on accessing neighboring cells to simulate the corresponding phenomena. Squeeze is based on the combination of two block-space maps that act between compact and embedded space, both adapted as tensor core MMA operations to further increase GPU performance. Experimental results show that Squeeze is up to $12 \times$ faster and $315 \times$ more memory efficient than a GPU-based bounding box approach, and can even match the performance of another recent GPU-based work that only improved performance but still sacrificed memory.

The remaining sections of the manuscript cover related work (Section 2), the proposed Squeeze approach (Section 3), experimental results (Section 4) and conclusions (Section 5).

2. Related Work

This section will cover the first related work [7, 8] in more detail, as it establishes the foundations for the present work. The rest of the works are synthesized and grouped by type of contribution.

Navarro *et al.* [7, 8] proposed an efficient GPU Tensor-core accelerated thread map for NBB fractals, denoted $\lambda(\omega)$, where ω is a 2D coordinate. The authors report up to $9 \times$ of speedup over a bounding-box approach, and up to an extra 40% of speedup by using GPU tensor cores. The $\lambda(\omega)$ map allows using a reduced number of threads to reach the fractal data elements in an expanded embedded representation. In terms of CUDA programming, the approach proposed by Navarro *et al.* compacts the CUDA Grid of thread-blocks to the minimum necessary to efficiently process the fractal, leading to a significant speedup. Figure 4 illustrates the benefits of using $\lambda(\omega)$ compared to bounding-box (BB).



Figure 4: Mapping of threads with BB and $\lambda(\omega)$ [7].

Although $\lambda(\omega)$ can solve problem P1 and improve performance significantly, it cannot manage all¹ types of simulations in compact space, such as stencil or general nearest-neighbors ones. Therefore, $\lambda(\omega)$ cannot solve problem P2 properly, leaving an open research problem on finding an efficient GPU solution for P1 and P2.

The rest of the related work is grouped into three main topics: i) GPU processing in complex domains, ii) Compact GPU processing on sparse data iii) acceleration of non-AI tasks via GPU tensor cores.

2.1. GPU processing in complex domains.

Jung *et al.* [9] developed an algorithm to map triangular (2-simplex) shaped data to a rectangular box to accelerate LU and Cholesky decomposition. The total memory used is reduced in half.

Ries *et al.* [10] developed a new method to compute the inverse of triangular matrices by developing a recursive parallel space mapping from a compact rectangular domain using GPU. The map's complexity is $O(\log_2(n))$.

Navarro *et al.* [11, 12, 13] proposed a GPU block-space mapping for 2 and 3-simplex domains based on a linear numbering of discrete elements. Authors report an empirical speedup of up to $1.5 \times$ and $2.3 \times$ over a bounding-box approach, for 2 and 3-simplices, respectively.

2.2. Compact GPU processing on sparse data.

Zachariadis *et al.* [14] proposed tSparse, an algorithm to accelerate sparse General Matrix Multiplication (GEMM) using Tensor Cores. Their approach use specific data structures and

¹The only case where $\lambda(\omega)$ can work in compact space is when threads operate just their own cell.

Look-up tables to efficiently save data. This approach significantly reduces computational resources requirements. It is on average $1.53 \times$ faster than other sparse GEMM techniques and the use of tensor cores provides an additional 68% of extra performance.

Weber *et al.* [15] presented a novel approach that significantly accelerates sparse matrix and vector multiplication in GPU. Authors report up to $13 \times$ speedup.

Ferrando *et al.* [16, 17] accelerated the processing of 3D cellular automaton simulations using an Octree to subdivide the 3D space. Their approach has a mixed GPU-CPU implementation with raw processing done in GPU and Octree update in CPU.

2.3. Acceleration of non-AI tasks via Tensor Cores.

Carrasco *et al.* [18] studied the theoretical benefit of tensor core based arithmetic reductions. Authors conclude that a tensor core based reduction is, indeed, faster. Continuing with their work [19], an implementation of said techniques resulted with a empirical speedup of $3.2 \times$ over traditional CUDA cores in large problem sizes.

Dakkak *et al.* [20] used tensor core to accelerate scan and arithmetic reductions in GPU achieving up to $100 \times$ speedup for small sized problems in reduction and up to $3 \times$ for scan.

The main difference of our proposal with respect to the described related work, is the focus on handling discrete fractal domains in compact space, and also the extra acceleration by adapting all map computations to GPU tensor cores. The next Section explains Squeeze; the proposed approach that allows efficient GPU tensor core processing on compact NBB fractals.

3. Overview of Squeeze

The proposed approach is a GPU scheme capable of processing any NBB fractal in compact space. As a result, it increases GPU performance and reduces memory usage when compared to an expanded bounding-box approach. Squeeze combines two GPU thread maps: $\lambda(\omega)$, an existing state-of-the art map [7] that transforms from compact space to expanded space, and $\nu(\omega)$, a new proposed map that transforms from expanded space to compact space. Using the two maps in conjunction, it is possible to do any kind of discrete simulation using only the compact space.

The notation $\mathcal{F}_n^{k,s}$ will be used to denote a fractal in the NBB class and to introduce the values n, k, s. Here, $n \in \mathbb{N}$ is the linear size of the fractal along one axis, $k \in \mathbb{N}$ the number of self-similar replicas generated by its transition function and $s \in \mathbb{N}$ the growth ratio of n in the next scale level, along an axis. For example, the Sierpiński Carpet (Figure 1) is $\mathcal{F}_n^{8,3}$ and the empty bottles fractal (Figure 2) is $\mathcal{F}_n^{7,3}$. Parameters k and s are specific to a fractal and n scales up by factors of s as the fractal level increases. The space used by a fractal, denoted as $\mathcal{V}(\mathcal{F}_n^{k,s})$ may be expressed as:

$$\mathcal{V}(\mathcal{F}_n^{k,s}) = k^r \tag{1}$$

where $r = \log_s(n)$ is defined as the scale level. Many different NBB fractals can be described using the same parameters. A table of NBB examples can be found in the work that formulated $\lambda(\omega)$ [7].

The presentation of Squeeze continues with a explanation of how any NBB fractal can be compacted into a rectangular region, then with a general view of how neighborhood exploration is achieved in compact space, which includes a brief revisit to $\lambda(\omega)$, and a detailed formulation of the new map $\nu(\omega)$ and its adaptation to GPU tensor cores.

3.1. Compacting NBB Fractals

Any NBB fractal expressed in the expanded embedded bounding-box representation, denoted D^2 , has a corresponding compact representation, denoted D^2_c . This compact representation is a rectangular region of size $k^{\lfloor \frac{r}{2} \rfloor} \times k^{\lceil \frac{r}{2} \rceil}$ elements, which satisfies $\mathcal{V}(\mathcal{F}_n^{k,s}) = k^r$.

Given a NBB fractal $\mathcal{F}_n^{k,s}$ in expanded embedded space, with $r = \log_s(n)$ the number of levels it has, the packing of its discrete data-elements into compact space follows a logic similar to an *unrolling* process of r steps. Let $\mu = 0$ refer to $\mathcal{F}_n^{k,s}$ at level 0; at this level the compact space has only one data element and coincides with the embedded space as well. At $\mu = 1$ (odd), the compact space is scaled up in x by k times (replication factor). At $\mu = 2$ (even), the compact space is scaled up in y by k. This process continues the same way for odd and even values until $\mu = r$. Figure 5 shows as an example the compaction logic for the Viczek fractal.



Figure 5: Compact space logic for the Viczek fractal $\mathcal{F}_{27}^{5,3}, r=3$.

3.2. Exploring Compact Fractal Space

Parallel exploration in a fractal's compact space is a special procedure, because a cell's neighborhood in D^2 in drastically different when seen in D_c^2 . Squeeze combines the already known $\lambda(\omega)$ map, with a the new map $\nu(\omega)$ (formulated ahead in Section 3.4) in such a way that the former acts as a tensor core-accelerated function from compact-space to embedded-space, while the latter acts as a tensor-core-accelerated function from embedded-space to compact-space. By using the two maps, it is possible for all fractal locations to explore their neighborhoods without expanding the fractal into embedded space in memory, thus preventing memory sacrifices.

To explore fractal neighborhood in compact space, Squeeze first uses $\lambda(\omega)$ to transform the thread's data-element location into expanded embedded space. Once the thread's location is transformed, it can easily offset its coordinate to define a neighborhood in this virtual expanded space which is transformed back to compact space with $\nu(\omega)$. With this, each neighbor is now identified in compact space and GPU threads can access the element in memory and continue the application's computation transparently. This approach performs at most one execution of $\lambda(\omega)$ map and ℓ executions of $\nu(\omega)$, where ℓ is the number of neighbors to explore. Figure 6 illustrates how the Squeeze approach uses both maps in conjunction.



Figure 6: Illustration of the process to access neighboring cells in a Sierpinski Triangle. The red cell represents the simulated element.

3.3. Revisiting $\lambda(\omega)$

Although $\lambda(\omega)$ is extensively described in [7], we provide a short summary that will be useful to formulate the new map $\nu(\omega)$. Map $\lambda(\omega)$ is formally defined as a thread-block mapping that transforms a coordinate from compact parallel space to a unique coordinate in the embedded space. This mapping can be done in $\mathcal{O}(\log_2(\log_s(n)))$ time.

The basic intuition behind $\lambda(\omega)$ is a coordinate offset accumulation in the compact space by detecting in which replica does the coordinate ω resides and offset accordingly in relation to its value. This is repeated in a top-down manner passing through the different scale levels, *i.e.*, from $\mu = r$ to u = 1 (level u = 0 does not generate any offset). This folding scheme is illustrated in Figure 7.



Figure 7: The action of $\lambda(\omega)$ illustrated for a single element in a Sierpinski Triangle at level r = 3. The red element is mapped from compact space to expanded embedded. The dashed orange blocks represent the scope of the current μ where the replica is identified, and the red shaded region is the current known sub-region where the cell is guaranteed to belong. The blue arrows are the offsets to accumulate at that iteration.

The map $\lambda(\omega) : \mathbb{N}^2 \to \mathbb{N}^2$ is defined as follows

$$\lambda(\omega) = \sum_{\mu=1}^{r} \Delta_{\mu} \tag{2}$$

where ω is a parallel resource coordinate (such as a thread or a block of threads). The process is a summation of offsets Δ_{μ} at each level, which are defined as

$$\Delta_{\mu} = \tau(\beta_{\mu}) \cdot s^{\mu - 1} \tag{3}$$

where τ is an normalized offset in the number of replicas along each axis (the scaling value s). In practice, τ acts through $H_{\lambda}[\beta_{\mu}] : \mathbb{N} \mapsto \mathbb{N}^2$ which can be a look-up table of size k that returns 2D coordinates, or a direct arithmetic hash if the replica patterns allow it. With this, τ is defined as

$$\tau(\beta_{\mu}) = H_{\lambda}[\beta_{\mu}] = (\tau_x, \tau_y), \quad \tau_x, \tau_y \in [0..s - 1]$$

$$\tag{4}$$

For example, in the Sierpinski triangle we have that s = 2 and the number of replicas is k = 3. Therefore, the possible outcomes for τ would be $\tau(0) = (0,0)$, $\tau(1) = (0,1)$ and $\tau(2) = (1,1)$ to refer the top, middle and right replicas, respectively. The proper scaling of the offset is done by the $s^{\mu-1}$ factor. Input β_{μ} is an auxiliary index defined as

$$\beta_{\mu}(\omega) = \left(\frac{\omega_x(\mu \mod 2) + \omega_y((\mu+1) \mod 2)}{k^{\lceil \frac{\mu}{2} \rceil - 1}}\right) \mod k \tag{5}$$

and has a range of [0, k - 1]. It identifies, within scale level $\mu \in [1..r]$, which of the k replicas of the fractal does the coordinate ω belong to,

To summarize $\lambda(\omega)$, this map serves as a mechanism to go from compact space to expanded embedded space. In the next sub-section, we formulate $\nu(\omega)$, the map that allows going from expanded embedded space back to compact space.

3.4. Formulation of $\nu(\omega)$

In order for Squeeze to work, we require a transformation from expanded space to compact space, *i.e.*, $\mathbf{D}^2 \mapsto \mathbf{D}_c^2$. We propose $\nu(\omega) : \mathbb{N}^2 \mapsto \mathbb{N}^2$, a map that acts as the inverse of $\lambda(\omega)$. As with $\lambda(\omega)$, $\nu(\omega)$ assumes that the origin (0,0) is located at the upper-left corner of both \mathbf{D}^2 and \mathbf{D}_c^2 spaces, and the x, y axes increase to the right and downwards, respectively.

To formulate $\nu(\omega)$, the offset accumulation approach is used again, but now checking on the expanded space what replica does element ω belongs to at each level using a top down scheme, and applying the offset into the compact space starting from (0,0) (upper-left). Going through all the scale levels, $\mu = r$ to $\mu = 1$ ($\mu = 0$ can be skipped as it gives zero offsets), allows collecting all the offset contributions. For even values of μ , the offset is accumulated in the x axis and for odd values, in the y axis. The magnitude of the offset depends on the actual value of μ . Figure 8 illustrates the process in a Sierpinski Triangle of r = 3.

The formulation of $\nu(\omega)$ follows a similar procedure that of $\lambda(\omega)$ [7]. Let $H_{\nu}(\theta_{\mu}) : \mathbb{N}^2 \to \mathbb{N}$ be a look-up table of size k, that given a coordinate $\theta_{\mu} = (\theta_{\mu,x}, \theta_{\mu,y})$ returns a value in the range



Figure 8: Example of the process done by $\nu(\omega)$ with a Sierpinski Triangle of r = 3. The red element is mapped from embedded space to compact space. The dashed region is the actual scope of iteration μ where the replica is identified. The blue arrows are the offsets to accumulate at each iteration.

[0, k-1] that represents which replica does the coordinate ω belong to at level μ in the embedded fractal. The coordinate θ_{μ} is defined as:

$$\theta_{\mu,x|y} = \left\lfloor \frac{\omega_{x|y} \mod s^{\mu}}{s^{\mu}} \right\rfloor \tag{6}$$

Let Δ^{ν}_{μ} (with superscript ν to denote that it refers to $\nu(\omega)$) denote the offset of the replica at a particular scale level. Δ^{ν}_{μ} is defined as:

$$\Delta^{\nu}_{\mu} = k^{\left\lfloor \frac{\mu-1}{2} \right\rfloor} \tag{7}$$

for ω_x and ω_y coordinates. Let $f(\mu)$ denote a filter function that alternates the accumulation of offsets between axes x and y as μ increases,

$$f(\mu) = (f_x(\mu), f_y(\mu))$$
 (8)

$$f_x(\mu) = (\mu - 1) \operatorname{\mathbf{mod}} 2 \tag{9}$$

$$f_y(\mu) = (\mu) \mod 2 \tag{10}$$

Combining the offsets with the lookup-table results and the filters, $\nu(\omega)$ becomes:

$$\nu(\omega) = (\nu_x(\omega), \nu_y(\omega)) \tag{11}$$

$$\nu_x(\omega) = \sum_{\mu=1}^{r} \Delta^{\nu}_{\mu} \cdot H_{\nu}[\theta_{\mu}] \cdot f_x(\mu)$$
(12)

$$\nu_y(\omega) = \sum_{\mu=1}^r \Delta_{\mu}^{\nu} \cdot H_{\nu}[\theta_{\mu}] \cdot f_y(\mu).$$
(13)

The map $\nu(\omega)$ can be computed by each GPU thread in parallel. However, in practice a better practice is to map blocks of threads in order to allow thread collaboration in the computation of $\nu(\omega)$ and data-locality at a small scale.

3.5. Moving from Thread-level to Block-level

To make the process more efficient on GPU, one can apply Squeeze at a block-level, that is, instead of mapping the thread coordinates, to map the block-coordinates. With this change, all $\rho \times \rho$ threads of a block now represent one coarse coordinate. In other words, block-level Squeeze can be seen as handling a lower level version of the fractal, where now r, n change to $r_b = r - \log_2(\rho)$, and $n_b = \frac{n}{\rho}$. This has the benefit of requiring less operations, allowing thread cooperation and producing memory locality within each block. Thread cooperation in a block allows doing a parallel reduction on Eqs. (12) and (13), resulting in a running time of $O(\log_2 \log_s(n))$ for $\nu(\omega)$. It is also worth noticing that in block-level Squeeze, space will be compacted at block-level, as expected, and inside each block one would find a small, constant size, expanded embedded fractal. Similar to quick-sort or other divide and conquer algorithms, applying micro-brute-force solutions at the last levels of a fractal structure can prove to be more efficient in terms of parallelism and locality. Figure 9 illustrates a block-level compact space.



Figure 9: Block-level Squeeze. In this example, each block has 4×4 elements, making the Sierpinski Triangle, of level of r = 4, become a coarser one of $r_b = 2$.

These micro-fractals indeed introduce an extra memory usage and may have some unused threads, but this overhead is constant as long as the size of the micro-fractals is in terms of the block-size which is constant.

Although block-level Squeeze has an efficient upper bound of $\mathcal{O}(\log_2(\log_s(n)))$ for both $\nu(\omega)$ and $\lambda(\omega)$, this performance can be further accelerated with tensor core units (TCU).

3.6. Accelerating Squeeze with Tensor Core Units

Today modern GPUs have up to hundreds of Tensor Core Units (TCUs). Each TCU provides a hardware-level matrix-multiply-accumulate (MMA) operation defined as

$$D = A \times B + C \tag{14}$$

that when called, is executed by a warp of threads and runs in parallel with the rest of the tensor core units of the GPU chip. Matrices A, B, C, D can have in the order of 256 elements, or more if precision is relaxed to FP16 or less.

The acceleration of Squeeze with tensor cores is achieved by encoding the sum of products found both in $\lambda(\omega)$ and $\nu(\omega)$. The Tensor Core adaptation of $\lambda(\omega)$ was already done in its previous work [7], therefore this subsection describes the process for the remaining map $\nu(\omega)$. The adaptation consists of encoding the sum of products found in Eq. (12) and Eq. (13) as MMA operations. The encoding is

$$A = \begin{pmatrix} \Delta_{1}^{\nu} f_{x}(1) & \Delta_{2}^{\nu} f_{x}(2) & \dots & \Delta_{r}^{\nu} f_{x}(r) \\ \Delta_{1}^{\nu} f_{y}(1) & \Delta_{2}^{\nu} f_{y}(2) & \dots & \Delta_{r}^{\nu} f_{y}(r) \\ 0 & 0 & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & 0 \end{pmatrix}$$

$$B = \begin{pmatrix} H_{\nu}[\theta_{1}] & 0 & \dots & 0 \\ H_{\nu}[\theta_{2}] & 0 & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ H_{\nu}[\theta_{r}] & 0 & \dots & 0 \end{pmatrix}$$
(15)

(17)

with C being a zero-matrix. These MMA operations are assigned one per warp, and given that the MMA can be perceived as a O(1) operation (hardware level), potential performance speedup is expected. The programming of tensor cores was done using CUDA's WMMA API available. Current restrictions on CUDA tensor cores specify that each tensor core matrix (known as fragment in CUDA) can have at most 256 elements when using FP16 multiplication $(A \times B)$ and FP32 accumulation (+C). This work chose 16×16 matrices for Squeeze, as the F16/FP32 configuration provided correct results.

3.7. Theoretical Memory Reduction Factor

Figure 10 shows the theoretical Memory Reduction Factor (MRF) of Squeeze over a expanded bounding-box (BB) scheme, for three NBB fractals.

From the plot it is possible to note that the MRF grows exponentially as the size of the fractal increases. At $n = 2^{16}$, Squeeze obtains an MRF close to $400 \times 105 \times$ and $3.4 \times$ for the Viczek,



Figure 10: Theoretical memory-reduction-factor of Squeeze.

Sierpinski Triangle and Sierpinski Carpet fractals, respectively. This enables the possibility to process in a single GPU fractals that did not fit before.

4. Experimental Setup and Results

Experimental tests were employed using Conway's game of life running on a Sierpinski Triangle as a case study, considering a Moore's neighborhood in expanded space. Only elements that belong to the fractal are simulated as well as considered as neighbors for the others, *i.e.*, the *holes* were skipped. Life/Death conditions were adapted for this same reason. Three different GPU-based fractal processing approaches were implemented²:

- 1. **BB**: Expanded grid and fractal representation in memory. It is the *classic approach*.
- 2. $\lambda(\omega)$: Compact grid and expanded fractal [7]. It is a state-of-the-art approach.
- 3. Squeeze: Compact grid and compact fractal. It is the proposed approach.

Figure 11 shows a comparison of the grid and memory requirements for each approach, using as an example the *chandelier* fractal.



Figure 11: Comparison of grid and memory spaces of the three approaches. The chosen fractal is named chandelier.

The performance metrics are the execution time, denoted T, and Speedup denoted S. Execution time was measured as the average time of 100 runs of 1000 simulation iterations for each hardware setup (listed in Table 1). This guaranteed an standard error lower than 1%. The Speedup is defined as

$$S = \frac{T_{ref}}{T_{comp}} \tag{18}$$

where T_{ref} is reference time, *e.g.* the bounding-box running time, and T_{comp} is the time of the tested approach. Parameters r and ρ were tested in the range r = [0, 20] and $\rho = [2^0..2^5]$, respectively. A shared and non-shared memory version of each method was tested. The results

²The repository will be available in the published version.

presented only show the fastest version of each one. For BB and $\lambda(\omega)$ the fastest one was without³ and Squeeze with shared memory due to the extra memory accesses on local space. Finally, both $\lambda(\omega)$ and $\nu(\omega)$ use tensor core acceleration.

The computer setups used are listed in Table 1.

	HW	Model
A	GPU	TITAN V, 5120 cores, 12GB
	TCU	640 Tensor Cores First Gen
	CPU	Intel i7-6950X 10cores
В	GPU	TITAN RTX, 4608 cores, 24GB
	TCU	576 Tensor Cores Second Gen
	CPU	Intel i7-6950X 10-core
С	GPU	A100, 6912 cores, 40GB
	TCU	432 Tensor Cores Third Gen
	CPU	$2 \times$ AMD Epyc 7742, 64cores

Table 1: Hardware setups used.

Setup C is a DGX A100 node of the Patagón Supercomputer [21] from Austral University of Chile.

4.1. Case study: Sierpinski Triangle

Experimental tests were done on the Sierpinski Triangle as an NBB fractal case study, simulating John Conway's game of life adapted to fractals. The reason why this fractal was chosen is mostly because it is one of the most recognized ones and has resulted to be a key structure for several applications, such as antenna construction [22, 23], cellular automata simulations [24, 25], fractal molecular ensembles [26], DNA self-replication [5], among others. In NBB notation, the Sierpiński triangle denoted as $\mathcal{F}_n^{3,2}$, with k = 3 and s = 2.

Replacing the Sierpinski fractal specific parameters in $\nu(\omega)$ yields⁴:

$$\Delta^{\nu}_{\mu} = 3^{\frac{\mu-1}{2}} \tag{19}$$

$$\nu_x(\omega) = \sum_{\mu=1}^r 3^{\frac{\mu-1}{2}} H_\nu[\theta_\mu] f_x(\mu)$$
(20)

$$\nu_y(\omega) = \sum_{\mu=1}^r 3^{\frac{\mu-1}{2}} H_\nu[\theta_\mu] f_y(\mu)$$
(21)

where $H_{\nu}(\theta_{\mu}) : \mathbb{N}^2 \to \mathbb{N}$ enumerates each replica as: 0 at the top, 1 the middle and 2 the right one. In the particular case of Sierpinski triangle, it is possible to use the hash expression

$$H_{\nu}[\theta_{\mu}] = \theta_{\mu,x} + \theta_{\mu,y} \tag{22}$$

which is equivalent to the look-up table $H_{\nu}[(0,0)] = 0$, $H_{\nu}[(0,1)] = 1$, $H_{\nu}[(1,1)] = 2$.

In the tested application, the cellular automaton simulation, each thread accesses a fractal adaptation of Moore's neighborhood, that means at most eight $\nu(\omega)$ maps for the neighbors that needs to be brought back to the compact space. This neighborhood upper bound of eight neighbors brings the possibility to group up to eight $\nu(\omega)$ maps into one tensor core MMA operation, because the matrices are of size 16×16 . Also, for technical simplicity the Tensor core approach was implemented for block sizes $\rho = 16$ and $\rho = 32$, other block-sizes use a regular CUDA computation of $\lambda(\omega)$ and $\nu(\omega)$.

 $^{^{3}}$ As a side note, we observed that for stencil computations, classic *shared-memory* practices that were known to produce the fastest implementations in older GPUs (such as Nvidia K40), may no longer produce such effect in newer GPU architectures. We suspect it may relate to the improvements on the L2 cache.

⁴For the Sierpinski Triangle version of $\lambda(\omega)$, see Navarro *et al.* [7]

4.2. Performance Plots

Figure 12 presents Squeeze's execution time T at different block sizes ρ next to the fastest versions of BB and $\lambda(\omega)$ in terms of chosen block size.



Figure 12: Execution times of the 3 approaches; BB, $\lambda(\omega)$ and Squeeze.

Starting with the NVIDIA A100, Once $n > 2^{12}$, Squeeze's $\rho = 16$ and 32 configurations become significantly faster than BB (blue curve). On the other hand, for smaller problems in the range $n \le 2^{12}$, all configurations of Squeeze ran slower than the best version of BB. Since Squeeze uses one $\lambda(\omega)$ map in the process, in theory $\lambda(\omega)$ would act as a lower bound for the performance of Squeeze, which in general is the case. Results with the TITAN RTX show a similar behavior than of the A100, once $n \ge 2^{13}$ and with $\lambda(\omega)$ as the lower bound. In the TITAN V, Squeeze at $\rho = 16$ is faster than BB once $n \ge 2^{11}$. Surprisingly, for this GPU Squeeze produces an anomaly and manages to run slightly faster than the best version of lambda for $n \ge 2^{15}$ by a small margin. Possible causes of this anomaly are discussed in Section 5. From these plots, it becomes clear that the best absolute performance of Squeeze is at $\rho = 16$.

Figure 13 presents the Speedup of Squeeze over BB at different block sizes ρ . Speedup curves



Figure 13: Speedup of Squeeze over BB. Each curve is the speedup for a particular block size.

of the NVIDIA A100 show that for $n \geq 2^8$ speedup starts to increase reaching a maximum of up to ~ 12× with block sizes of $\rho = 1, 2, 4, 8$. For $\rho = 16, 32$ Squeeze reaches up to ~ 3.7× of speedup. Thanks to the 40GB of GPU memory of the A100, it was possible to push the maximum problem size up to 2^{16} , except for the curve of S_{1x1} that could not reach the maximum size because of CUDA's grid size limits. The TITAN RTX under-performed in comparison with the other GPUs for $n \leq 2^{12}$. Past that value, speedup increases above 1 for all values of ρ , reaching a top speedup of ~ 3.2×. The TITAN V shows a similar pattern to the A100, with a top speedup of ~ 11×.

Figure 14 shows what is the performance contribution of the tensor cores. Results show a significant speedup across values of n, with the exception of $S_{32\times32}$ in TITAN V, where performance is negatively affected by using tensor cores, reaching S 0.75×. The reason is unknown, but could be attributed to limitations in Volta architecture and the behavior of warps with first-gen tensor core units. The top speedup varies by GPU/Generation: on the A100 its ~ 1.11×, on the TITAN RTX is around ~ 1.2× and on the TITAN V up to ~ 1.3×. In any of the three cases, it is a significant extra-acceleration.



Figure 14: The impact of using tensor cores vs not using them, for all three TCU generations (Volta, Turing and Ampere).

4.3. Memory Reduction Factor

Table 2 presents the total memory measured, as well as the memory reduction factor (MRF) by each approach to process a level r = 16 Sierpinski Triangle across different block sizes. We recall that block sizes have a size-reduction effect on the fractal due to the block-level Squeeze approach.

Table 2: Total memory needed and memory reduction factor (MRF) for each approach on the Sierpinski triangle at r = 16.

ρ	$BB \mid \lambda(\omega)$	$ u(\omega)$	MRF
1×1	16 GB	0.16GB	$99.8 \times$
2×2	16 GB	$0.21 \mathrm{GB}$	$74.8 \times$
4×4	16 GB	$0.29 \mathrm{GB}$	$56.1 \times$
8×8	16 GB	0.38 GB	$42.1 \times$
16×16	16 GB	$0.50 \mathrm{GB}$	$31.6 \times$
32×32	16GB	0.68 GB	$23.7 \times$

The table shows how small block sizes of $\rho = 1, 2$ are close to a MRF of $100\times$, while larger block sizes gradually diminish the MRF factor because of the micro-fractals inside each block. Nonetheless, it is worth noticing that at $\rho = 16$ (Squeeze's best configuration), the MRF is $31.6\times$ which is a substantial improvement over BB and $\lambda(\omega)$.

Additional experiments showed that the 40GB of the A100 GPU allowed Squeeze to process fractals of up to level r = 20, while BB and $\lambda(\omega)$ could only reach level r = 16 before running out of memory. The r = 20 achieved with Squeeze required from ~ 13 to ~ 55 GB of memory depending on the block size ρ . Processing a fractal of this size with a BB or $\lambda(\omega)$ approach would require 4096GB of memory, this translates to a MRF of ~ 315× for Squeeze.

5. Discussion and Conclusions

This work presented Squeeze: an approach for handling compact fractals efficiently on GPUs. By using an efficient compact representation, two benefits emerge: i) computation is employed only in the fractal elements and not in the entire embedding space, bringing speedup with respect to a bounding-box approach, and ii) it produces a significant reduction in memory usage, moving from expanded space to the Hausdorff dimension of the fractal. Tests with the A100 GPU provided a memory reduction factor (MRF) of up to $\sim 99.8 \times$, with a potential of $\sim 315 \times$ for level r = 20. The MRF increases as the fractals becomes larger, meaning that future generation of GPUs could reach problem sizes that would be infeasible with traditional approaches that use the fractal's expanded embedded form.

In terms of performance, tests with the Sierpinski triangle showed up to $12 \times$ of speedup compared to a Bounding Box approach. Results also showed that the speedup, similar to the MRF, keeps increasing with the fractal size. When comparing Squeeze with the state of the art $\lambda(\omega)$ approach, we noted $\lambda(\omega)$ is actually a performance lower bound. Although it is clear this lowerbound should exist as a general rule, we noted that one performance result with the Titan V GPU showed that Squeeze managed to run slightly faster than $\lambda(\omega)$. The cause of this anomaly might be related to internal properties of first-gen tensor cores or with the behavior of shared memory / memory accesses in Volta. Further research on this matter could give more insights.

Adapting the computation of Squeeze to GPU tensor cores provided up to 30% of extra performance compared to just using regular CUDA cores. Future improvements to tensor cores, both in quantity and performance, would provide an even higher improvement. As future work, it would be useful to come up with a way to build arbitrary fractal structures by combining different NBB fractals at each scale level, as well as to extend Squeeze to support compact processing on 3D and higher-dimensional fractals. As a final conclusion, the proposed approach can be adopted by the community to accelerate simulations on NBB fractals and understand phenomena at larger scales.

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