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Extraction of the active acceptor concentration in (pseudo-) vertical GaN MOSFETs using the body-bias effect

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ABSTRACT

We report and discuss the performance of an enhancement mode n-channel pseudo-vertical GaN metal oxide semiconductor field effect transistor (MOSFET). The trench gate structure of the MOSFET is uniformly covered with an Al_2O_3 dielectric and TiN electrode material, both deposited by atomic layer deposition (ALD). Normally-off device operation is demonstrated in the transfer characteristics. Special attention is given to the estimation of the active acceptor concentration in the Mg doped body layer of the device, which is crucial for the prediction of the threshold voltage in terms of device design. A method to estimate the electrically active dopant concentration by applying a body bias is presented. The method can be used for both pseudo-vertical and truly vertical devices.

Since it does not depend on fixed charges near the channel region, this method is advantageous compared to the estimation of the active doping concentration from the absolute value of the threshold voltage.

1. Introduction

Recently, significant progress has been achieved in the GaN device technology for power applications. Most of these achievements can be attributed to advancements of the AlGaN/GaN high electron mobility transistor (HEMT) and first products for voltage ratings up to 600 V are commercially available. However, the lateral device structure of the HEMT implies less efficient area scaling at higher voltage ratings compared to a vertical GaN device. In vertical device topologies, the scaling towards higher breakdown voltage is achieved by increasing the drift layer thickness independently from the lateral device dimensions. Based on this consideration, vertical devices on bulk GaN substrates should be more suitable for higher power/voltage ratings compared to lateral device designs [1].

Different vertical device concepts like the current aperture vertical electron transistor (CAVET) [2], the vertical MIS FET [3 5] or the vertical heterostructure FET [6] have been reported in the past years. Several contributions have also been made for the vertical trench MOSFET, with [7] or without re grown channel layer [8,9]. A quasi vertical MOSFET on GaN on Si was shown in Ref. [10]. The inherent normally off behavior of the enhancement mode device prevents false turn on and enables

fail safe operation.

Since the availability of GaN bulk material is still limited, it is more convenient to fabricate pseudo vertical devices on a sapphire substrate in order to develop a good understanding of the fundamental device and material properties. Later, the process flow can be adjusted to transfer the "pseudo" to a "true" vertical design.

The electrically active (not passivated) acceptor concentration (N_A) of the Mg doped p GaN layer is an important parameter for device operation and threshold voltage. The ratio of ionized acceptors N_A / N_A can locally reach 100% in a space charge region, which enables the indirect esti mation of N_A . Although, methods have been proposed to estimate the activation of Mg on c plane structures in Refs. [11,12], in the vertical trench technology large parasitic contributions resulting from overlap capacitances to the source and drift layer inhibit the estimation of N_A at the trench sidewall. Additionally, the remaining hydrogen content can be inhomogeneous after lateral hydrogen out diffusion treatments [11]. By taking advantage of a separate body contact to the p GaN N_A can be obtained from measuring the body bias effect on the threshold voltage directly at the vertical channel of a trench MOSFET. The compromise associated with a separate body contact is the increase of the active de vice area, resulting in higher leakage current and decreased area

* Corresponding author. *E-mail address:* rico.hentschel@namlab.com (R. Hentschel). efficiency compared to combined source and body contact designs.

2. Device fabrication

Starting with an AlN based nucleation layer, the $p/n^{-}/n^{+}$ GaN tem plate was grown on a sapphire substrate by metal organic chemical vapor deposition (MOCVD). The layer sequence consists of a 2.6 μ m thick n⁺ GaN layer (Si doped with a concentration of 3×10^{18} cm⁻³), a 1.1 µm thick n⁻ GaN drift layer (Si doped with a concentration of 2×10^{16} cm⁻³) and a 0.8 µm thick p GaN layer (Mg doped with a nominal concentration of $3\times 10^{18}\,\text{cm}^{-3}$), as shown in Fig. 1. Prior to growing the n^+ GaN source layer (Si doped) with plasma assisted molecular beam epitaxy at 650 °C and growth conditions as described in Refs. [13,14], a hydrogen out diffusion anneal was performed at 750 °C for 10 min in nitrogen followed by outgassing at 600 °C for 4 h in the ultra high vacuum growth environment. The upper n^+ and p GaN layer stacks have a dislocation density of 1×10^9 cm⁻² 3×10^9 cm⁻² determined by atomic force mi croscopy (AFM). The drift layer thickness of 1.1 µm was chosen to sustain a moderate breakdown voltage while maintaining the ability to etch down to the lower n⁺ GaN layer for the pseudo vertical backside drain contact deposition.

The device isolation and metal contacts to the different GaN layers were processed by alternating dry etching with BCl₃ and Cl₂ plasma metal evaporation with subsequent structuring by lift off and annealing. Ti/Al and Ni/Au based stacks have been used as contact metals for n and p GaN layers, respectively. Starting with the source and drain n GaN contacts, annealing in nitrogen atmosphere was carried out in order to obtain ohmic behavior. The source and drain n GaN metal stack is opti mized to withstand HCl and HF surface treatments and possible oxida tion, during the body p contact anneal at 500 °C for 5 min with oxygen addition after the Ni/Au deposition. However, an aggressive surface conditioning e.g. with tetramethylammonium hydroxide (TMAH) or aqua regia of the dry etched p GaN surface to further improve the body contact quality is not possible at this step of the process flow.

The trench gate module was fabricated in one sequence. The trench formation starts with a Cl based inductively coupled plasma (ICP) dry etching step, using a plasma enhanced chemical vapor deposited (PE CVD) Si_xN_y hard mask. Subsequently a wet chemical treatment with 25% TMAH in water for 60 min at 80 °C was performed in order to smoothen the trench sidewall and remove damage caused by the plasma etching. The previously fabricated contacts are covered and protected by the hard mask during this step. Similar processes were reported in Refs. [15,16] and optimized for our requirements. After removing the remaining hard mask in an HF wet etch, the obtained gate trench was covered with a 30 nm thick Al₂O₃ film using ALD and a similar process as reported in Ref. [17]. A TiN gate electrode was subsequently deposited by ALD and was structured by dry and wet chemical etching to complete the gate module. In regions outside of the gate stack the Al₂O₃ serves as a first passivation layer of the device. Fig. 1 shows a schematic cross section of

the device with separate body contact and a scanning electron micro graph (SEM) of one sidewall of a gate trench. The uniform deposition of Al_2O_3 and TiN is essential for a good channel control and low leakage.

3. Results and discussion

The transfer and output characteristics in Fig. 2 and Fig. 3 demon strate device functionality. Scaling of the current characteristics with various gate and drain bias as well as normally off operation are shown. The transfer curves exhibit a threshold voltage of about 3 V obtained at a current criterion of 1×10^{-4} A/mm. Extraction of the field effect mobility (μ_{FE}) from g_m according to Ref. [18] results in a maximum μ_{FE} of $38 \text{ cm}^2/\text{V}$ as shown in Fig. 2. This value underestimates the mobility, since series resistance contributions are not taken into account, but are quite significant as described below. From the output curve at V_{GS} 8 V, an on resistance $(R_{DS,on})$ of about 24 Ω mm is derived. For the pseudo vertical device with rather large lateral dimensions, the channel resistance is the most interesting part, since it would contribute in a similar way to the overall R_{DS,on} of a true vertical device. Some of the other series contributions to the total $R_{DS,on}$ are obtained by means of transfer length method (TLM) structures in combination with the used design parameters. Contact resistances for source and drain are in the range of 1 2 Ωmm and source and drain layer resistances are about $3\,\Omega$ mm and $8\,\Omega$ mm, respectively. Resistances of the metal lines are negligible and with estimations of the drift layer and spreading resistance of about 2 3 Ωmm, the channel resistance should be in the range of $10\,\Omega$ mm. The true channel mobility can thus be estimated to be approximately in the range of 70 $80 \text{ cm}^2/\text{V}$.

More information on the channel region can be obtained from transfer curves in double sweep mode as presented in Fig. 4. The curves show a subthreshold swing of 200 mV per decade of the drain current. The observed hysteresis between backward and forward sweep of 350 mV would correspond to an interface trap density of N_{eff} 5.6 × 10¹¹ cm⁻² at the dielectric/channel interface using the for mula and parameters as described below. Lowering of the channel resistance due to an increased mobility and reduced trapping can be expected with optimization of the channel/dielectric interface.

The devices exhibit a moderate on/off current ratio of 5 orders of magnitude, due to a relatively high off current. This current level is not limited by the gate leakage, but caused by the large active device area and parasitic leakage components [19].

In the following section, we discuss the correlation between the threshold voltage and the Mg acceptor concentration. The acceptor concentration (N_A) can be much smaller than the total incorporated Mg concentration due to hydrogen passivation [20]. The relation between



Fig. 1. Schematic cross section (not to scale) of one half of the symmetric pseudo-vertical MOSFET (right) and cross sectional scanning electron micrograph of a single gate trench edge (left). Contributing series resistances to the on-resistance $R_{DS,on}$ are shown with the contact resistances R_c , drift and drain layer resistance R_d and R_D , source resistance R_S and channel resistance R_{ch} .



Fig. 2. Transfer characteristics $I_D(V_{GS})$ for different drain-source voltages V_{DS} , each measurement was started at 0 V, field-effect mobility calculated from the transconductance.



Fig. 3. Output characteristics ID(VDS) of the device measured for different gate bias VGS and for VDS from 0 V to 4 V.



Fig. 4. Transfer characteristics $I_D(V_{GS})$ measured from 0 V to 7 V and back at a drain-source voltage of 0.1 V. A threshold voltage of around 2.8 V (at $I_D = 1 \times 10^{-4}$ A/mm), a subthreshold slope of 200 mV/decade (black fit line) and a voltage shift of 350 mV between both sweeps can be extracted.

the threshold voltage and N_A including a body bias term is given by (1) and can be rearranged and solved for N_A [21].

$$V_{th} = \Phi_{ms} = \frac{Q_{eff}}{C_{ox}} + 2\varphi_F + \frac{\sqrt{2q\varepsilon_o\varepsilon_r N_A} (2\varphi_F - V_{BS})}{C_{ox}}$$
(1)

Here, *q* is the elementary charge and ε_0 and ε_r are the vacuum and the relative permittivity of GaN. $C_{ox} = 2.5 \times 10^{-7}$ F/cm² is the oxide capac itance of the 30 nm Al₂O₃ dielectric, which was extracted from *C*(*V*) measurements of planar MIS n GaN structures processed in parallel on the same wafer and die. For the work function of TiN a value of 4.8 eV [22,23], is used in the calculation of the work function difference Φ_{ms} between metal and semiconductor. The term Q_{eff}/C_{ox} reflects the voltage contribution of charges effectively located at the dielectric/GaN interface Although, both the Fermi energy with respect to the intrinsic level φ_F and the work function difference Φ_{ms} depend weakly on N_A , but the calculation of these three values can be iteratively performed with an acceptor level of $0.2 \text{ eV} \gg 3 \text{ kT}$ [24,25] above the valence band maximum, with a temperature of T 300 K and *k* representing the Boltzmann constant. It has to be mentioned that due to the deep acceptor

level of about 0.2 eV only a small fraction of the (hydrogen free) Mg acceptors are ionized at room temperature in equilibrium or at flat band condition, typically in the range of 3 8%. This portion is equal to the hole concentration in bulk material, but the fraction of ionized acceptors can reach up to 100% of the hydrogen free Mg atoms in a depleted space charge region. Hence, doping concentrations obtained by methods involving a space charge region yield the total hydrogen free (active) acceptor concentration determining the threshold voltage of the device. A first estimate of N_A can be derived from a typical V_{db} as shown in Fig. 4 ($V_{th} \approx 3$ V, at I_D 1 × 10⁻⁴ A/mm, down sweep) under the assumption of N_{eff} 0 cm⁻². As result a value of N_A 4.6 × 10¹⁷ cm⁻³ is obtained. This estimation can strongly be influenced by interface charges under the gate.

Utilizing the body bias effect on the threshold voltage provides a way to access the acceptor concentration N_A directly on the MOSFET under test without assumptions on fixed gate dielectric or interface charges. The transfer characteristics with V_{GS} from 0 V to 6 V with varying body bias are shown in Fig. 5 on a similar device. In order to stabilize the transfer curve the measurement at V_{BS} 0 V was repeated multiple times. From the shift of the threshold voltage ΔV_{th} an active acceptor concentration of N_A can be calculated by:

$$N_A \qquad \frac{\Delta V_{th}}{\Delta \sqrt{(2\varphi_F - V_{BS})}} \bigg)^2 \frac{C_{ox}^2}{2q\varepsilon_o\varepsilon_r} \tag{2}$$

The data shown in Fig. 5 yield an average value of about $2.5 \times 10^{17} \text{ cm}^{-3}$. The obtained values of N_A for each separate curve of Fig. 5 are shown in Fig. 6. The extracted level of N_A remains nearly constant for different V_{BS} with a value of about $N_A = 2.5 \pm 0.5 \times 10^{17} \text{ cm}^{-3}$. This value is lower than the previously calculated value. Re calculation according to (1) with $N_{eff} = 0 \text{ cm}^{-2}$ and $V_{BS} = 0 \text{ V}$ yields a V_{th} of 2.4 V.

Attributing the difference of measured and calculated V_{th} to a fixed, trapped charge effectively located at the dielectric/GaN interface, a value of around Q_{eff} 1×10^{12} cm⁻² can be obtained, which is higher compared to the value obtained directly from the hysteresis in Figs. 4 ($5.6 \ 10^{11} \ \text{cm}^{-2}$). It is likely that the total trap concentration is in the range of N $1.5 \times 10^{12} \ \text{cm}^{-2}$, but it consists of both fast and slow responding traps.

Under the assumptions of the complete ionization of the hydrogen free Mg acceptors in an electric field inside the space charge region beneath the gate and a nominal p GaN doping concentration of 3×10^{18} cm⁻³, the obtained value leads to a hydrogen passivated Mg fraction of around 92%, matching theoretical calculations in Ref. [26] for the applied hydrogen out diffusion anneal with low thermal budget.

4. Conclusion

The body bias effect on the threshold voltage of (pseudo) vertical GaN MOSFETs enables an estimation of the effective channel doping without assumptions on charges in the gate dielectric or its interface to the p GaN. By means of the body bias effect, the ionized acceptor con centration was determined to be about $2.5 \times 10^{17} \text{ cm}^{-3}$ in the space charge region of the device. This corresponds to 8% of the total incor porated Mg with a concentration of 3×10^{18} cm⁻³ and corresponds to the concentration of hydrogen free Mg sites under the assumption of com plete ionization in the space charge region. This percentage value, on the one hand, might be increased using a hydrogen out diffusion treatment with higher thermal budget. On the other hand, once the acceptor con centration is known, more insight in charge related phenomena in the dielectric or at the dielectric/p GaN interface can be obtained. This valuable information is not easily accessible from capacitance methods, since the channel capacitance at the vertical sidewall of the trench gate structure is significantly affected by parasitic contributions in realistic structures directly on the vertical sidewall of the trench gate.



Fig. 5. Transfer characteristics $I_D(V_{GS})$ at different body bias voltages V_{BS} with 1 V step width, each measurement was started at $V_{GS} = 0$ V and performed at a V_{DS} of 0.1 V.



Fig. 6. Threshold voltage (right axis) and calculated active acceptor concentration (left axis) versus body-source voltage V_{BS} for both sweep directions of the transfer curve.

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