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Low-frequency noise in hot-carrier degraded nMOSFETs

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Abstract

This paper discusses the low-frequency (LF) noise in submicron nMOSFETs under controlled transistor aging by hot-carrier stress. Both traditional, steady-state LF noise as well as the LF noise under periodic large-signal excitation were found to increase upon device degradation, for both hydrogen passivated and deuterium passivated $Si–SiO_2$ interfaces. As hot-carrier degradation is slower in deuterium-annealed MOSFETs, so is the increase of the noise in these devices. The noise-suppressing effect of periodic OFF switching is gradually lost during hot-carrier degradation, as the LF noise under periodic large-signal excitation increases more rapidly than the LF noise in steady-state.

1. Introduction

Low-frequency (LF) noise is of growing concern for analog CMOS circuit design. It is therefore important to characterize the amount of LF noise not only for fresh devices but also during the lifetime of the transistor. In MOSFETs LF noise originates from traps in the gate dielectric and at the $Si–SiO_2$ interface. Time accelerated degradation by hot-carrier (HC) stressing changes the density and the distribution of the trapped oxide charge and the trapped interface charge. The damage caused by the hot-carrier injection is clearly visible in a reduction of the maximum transconductance (g_m), the drive current (I_{ON}) and a shift of the threshold voltage (V_T) of the device. An increase in the trap concentration, due to hot-carrier stress, also results in an increase of the LF noise as reported in literature [1].

In this paper we quantify the noise increase resulting from hot-carrier degradation. Furthermore, we investigate two methods that could reduce LF noise: that is bias switching and deuterium passivation.

2. Experimental

nMOSFETs fabricated in a 0.18 μm process with a drawn gate length $L = 0.5$ μm and gate width $W = 2.0$ μm with a gate oxide thickness of 7 nm (the embedded flash dielectric) were used. The devices were processed until the first metal level. Final step in the device processing was a 30 minute post metal anneal (PMA) at 450 °C in a D_2/N_2 or H_2/N_2 ambient. The DC device characteristics and LF noise were respectively measured with an Agilent 4156C parameter analyser and an Agilent E550 phase noise setup.

The applied hot-carrier (HC) stress of $V_{ds} = 4.5$ V and $V_{gs} = 2.1$ V was periodically interrupted for device characterization and LF noise analysis. These were performed in reverse mode (i.e. with the source and drain terminals interchanged), since the hot-carrier damage is mainly located on the drain side. In this way the degraded region forms a part of the controlled channel and the device degradation can be more clearly observed [2,3]. The applied bias voltages correspond to peak substrate current conditions. The chosen drain voltage was sufficiently low to prevent premature gate oxide breakdown.

The LF noise was measured using a differential setup described earlier [4], using a matched transistor pair. The HC stress was applied to both MOSFETs simultaneously.

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The difference of the two transistor's drain currents was measured to accurately determine the noise.

Two sets of noise measurements are performed. First at a constant biasing and secondly when the transistors are switched periodically between ON and OFF (below threshold). The steady-state LF noise measurements were performed at a fixed drain current of 10 μA, making a reliable comparison between the noise measured before and after stress. This was made possible by increasing V_{gs} to compensate for the increase in V_T due to hot-carrier stress. For this switched measurement the excitation frequency used was 10 kHz with a duty cycle of 50%. In both biasing conditions, the noise power was calculated at a frequency of 100 Hz.

3. Results

As expected the incorporation of deuterium at the interface does not influence the virgin transistor parameters [5]. LF noise always has a large device-to device-variation for devices of these dimensions. The noise of the D_2- and H_2- annealed samples is comparable within the statistical variation within one wafer. Fig. 1 shows the degradation of the maximum transconductance, g_m, for samples with a PMA in H_2 and D_2 environment. The bars indicate the statistical variation within the wafer. Due to the time-consuming nature of the LF-noise measurements the number of tested devices was limited to 10 for each anneal condition. Using the lifetime criteria of a 50 mV threshold voltage shift (ΔV_T) or 10% reduction in g_m we find an increased lifetime by a factor 4 for the D_2 annealed transistors compared to the H_2 annealed ones. Fig. 2 compares the noise spectral density measured on fresh devices and after 1000 s HC stress, for both H_2 and D_2 passivated devices. The hydrogenated samples show a significant noise increase after 1000 s HC stress whereas the deuterated samples show negligible increase in LF noise. Fig. 3 shows the distribution of LF noise at 10 Hz for fresh and stressed devices on both H_2 and D_2 passivated transistors. After 1000 s stressing the D samples show no significant noise increase. It can even be seen that the LF noise increase for H_2 samples after 1000 s stress is larger that the LF noise increase after 4000 s for the D_2 devices. Periodically switching the devices between the ON and OFF state dramatically reduces the LF noise. At 50% duty cycle a 6.02 dB reduction results from the fact that in the off-time no noise is generated [4]. Fig. 4 shows that the observed reduction in fresh devices is typically much larger than 6.02 dB, as

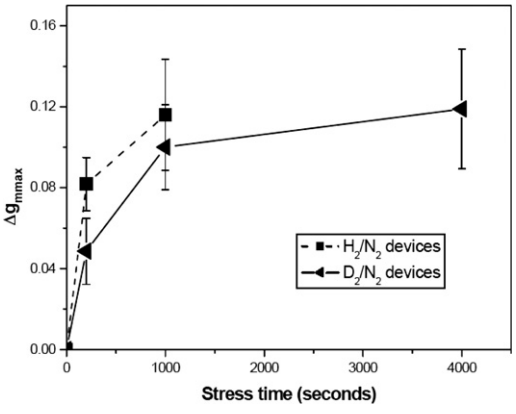

Fig. 1. Relative transconductance change. The bars indicate the statistical variation within the wafer.

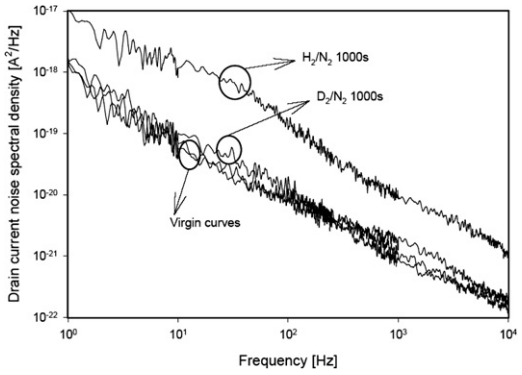

Fig. 2. Low-frequency noise power spectral density for virgin and stressed devices.

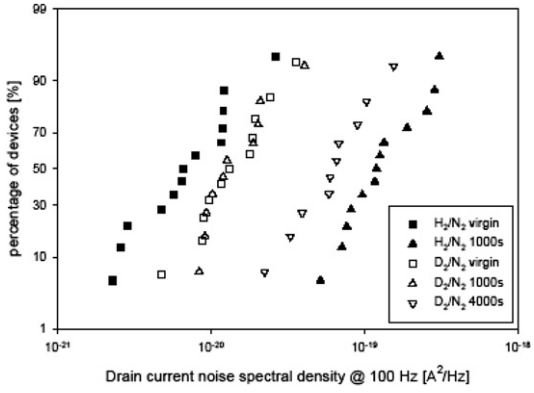

Fig. 3. Distribution of the noise spectral density for H_2 and D_2 passivated fresh and stressed devices.

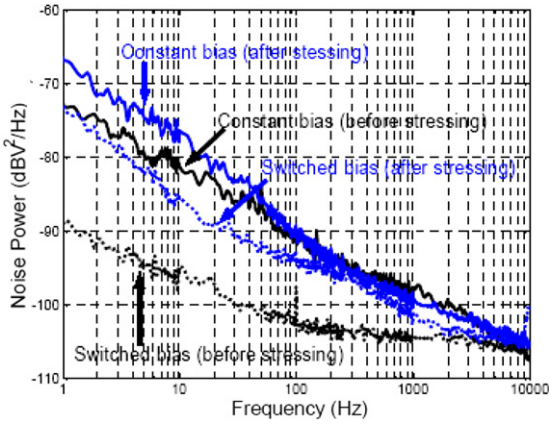

Fig. 4. LF noise spectra of fresh and degraded hydrogen passivated transistors (1000 s HC stress).

reported earlier [4,6,7]. Note that above the switching frequency of 10 kHz no noise reduction is expected [4]. Noise measurements with high switching frequencies have shown this anomalous noise reduction effect to persist up to 3 GHz [8].

After the devices have been degraded by 1000 s of HC stress both the LF noise under constant biasing as well as that of the switched transistors increase. As can be clearly seen from Figs. 4 and 5 the benefit of periodically switching the transistors OFF decreases with stress time. Fig. 5 shows the increase in noise for both the constant biased as well as the periodically switched transistors. Similar as what is observed for the DC device degradation (see Fig. 1) the increase in noise is approximately 4-fold slower for the transistors with a D_2 passivated interface. The relation between the V_T-shift and the corresponding LF noise increase is depicted in Fig. 6. The data points are grouped along two lines, one for LF noise under constant biasing and one for the LF noise when the transistors are periodically switched OFF. We observe that the isotope effect, invisible on fresh devices, manifests itself as a retardation in both HC degradation and noise increase.

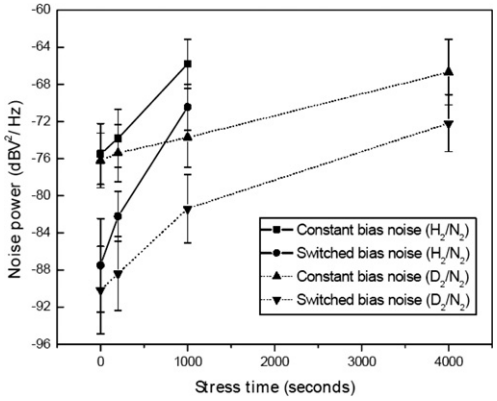

Fig. 5. Noise increase for constantly biased and periodically switched transistors.

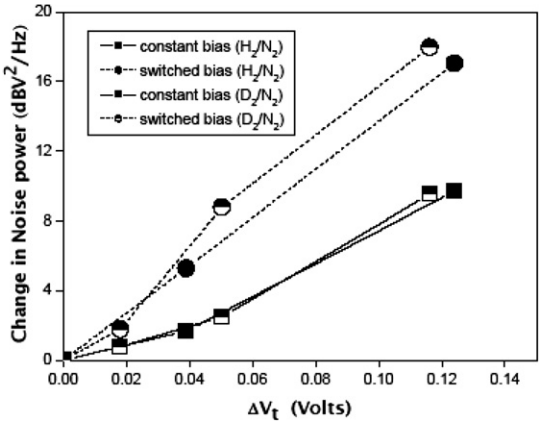

Fig. 6. Correlation between the increase in LF noise and the threshold voltage shift under constant biasing and periodic switching of H_2 and D_2 passivated transistors.

4. Discussion

Prolonged hot-carrier stressing increases the trap density at the Si–SiO_2 interface resulting in a decrease in g_m and I_{on} and an increase of V_T. Deuterium passivation of the interface retards the hot-carrier degradation due to the slower desorption of deuterium [9–11] reducing the interface state generation rate. The noise in deuterium passivated samples hence increases slower compared to the hydrogenated samples. For fresh devices it has been reported previously that periodic OFF switching of the transistors results in a change in the time constants of the dominant slow traps [12]. This in turn results in a reduced LF noise that is now mainly due to fast traps (fast with respect to the switching frequency).

Hot-carrier stress under peak substrate bias conditions increases the number of fast interface traps and herewith increases the LF noise. The impact of hot-carrier degradation on the LF noise under periodic switching is much larger than on LF noise under constant biasing due to this dominance of the fast traps. In other words, the newly created interface traps are insensitive to the periodic OFF switching, which only affects the pre-existing slow traps. As a result the noise suppression benefit by bias switching rapidly decreases when transistors suffer from hot-carrier degradation.

On the contrary deuterium passivation retards hot-carrier degradation and consequently also retard the LF noise increase.

Applying a combination of deuterium passivation to retard LF noise increase with bias switching to reduce the LF noise gives the lowest possible LF noise. However, for analog CMOS circuits biased in hot carrier sensitive conditions, deuterium annealing results in a more constant LF noise compared to bias switching which might be beneficial for circuit designers.

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