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Investigation on the degradation indicators of short-circuit tests in 1.2 kV SiC MOSFET power modules

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Abstract

This paper provides a comprehensive investigation on both static characteristics and short-circuit performance of 1.2 kV SiC MOSFET power modules with 2nd generation planar technology. The experimental approach is based on the static characteristics measurements and the short-circuit tests with gradual increase of pulse time duration. If any variation of the static characteristics appears, the time duration of next short-circuit tests would keep the same with the last pulse duration (approach 1) or increase continuously (approach 2). The results of the short-circuit waveforms show a gate degradation which is further confirmed with the measurement of the gate leakage current. Additionally, other degradation indicators, including positive shift of threshold voltage, drain leakage current and on-state resistance increase are evidenced and discussed in this paper. These can be used for early prediction of the degradation and failure in the short-circuit conditions.

1. Introduction

Silicon Carbide (SiC) power electronic devices are now considered as the key components for future applications due to their superior physical properties compared with the silicon devices (i.e. increased electric field strength, thermal conductivity and electron velocity) [1]. However, the reliability of SiC devices needs to be further evaluated since silicon-based devices have proven to be more reliable, especially under Short-Circuit (SC) conditions [2].

Many efforts have been carried out to analyse the performance of SiC MOSFETs during SC tests [3]. The change in drain current slope and the appearance of drain current tails at turn-off have been discussed in [4] and [5]. Moreover, the static characteristics before and after the SC tests have also been investigated; among these, the positive and negative shift of threshold voltage (V_{th}) has been discussed in [6] and [7], respectively. The longer pulse time duration (t_{SC}), larger number of repetitive short circuits (from 1 pulse to 100 pulses SC) and larger gate-source voltage (from +18 V/-5 V to +20 V/-5 V) during SC tests could aggravate the variation of threshold voltage at several hundred mV level [8]. Additionally, the on-state resistance ($R_{ds,on}$) [9], gate leakage current (I_{GSS}) [10] and drain leakage current (I_{DSS}) [7] also vary after repetitive SC tests. Nevertheless, most of the previous works were focused on discrete devices; the degradation indicators and physical mechanisms of SiC MOSFET power modules in the SC conditions still need to be fully understood.

In this paper, the SC performance of commercial 1.2 kV/ 500 A SiC MOSFET power modules are presented. A gate degradation has been observed during the SC tests and the successive static characterizations. The impact of SC tests on the static characteristics, including threshold voltage (V_{th}), gate leakage current (I_{GSS}), drain leakage current (I_{DSS}) and on-state resistance ($R_{DS,on}$) have been measured and analysed. Finally, the effects of room-temperature recovery after SC tests have also been investigated for the first time.

2. Test setup and approaches

A 2.4 kV/ 10 kA Non-Destructive Tester (NDT) has been used for SC tests. The principle schematic

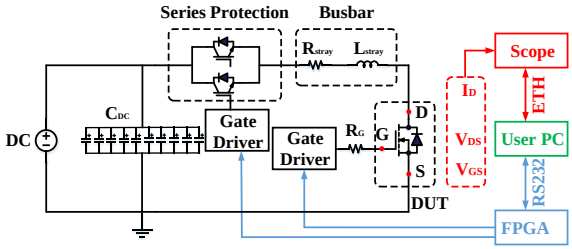

Fig. 1. Principle schematic of the Non-Destructive Tester (NDT).

Fig. 2. Picture of NDT setup in the laboratory.

and its appearance are shown in Fig. 1 and Fig. 2, respectively. The needed SC energy is provided by a high voltage power supply (DC) and the capacitor bank (C_{DC}). A series protection, consisting of 4 IGBT power modules which are paralleled to increase the current capability, is used as a circuit breaker to prevent explosions and allow failure analyses on the degraded samples. A 10 nH busbar has been designed to ensure low stray inductance. The Device Under Test (DUT) is a 2nd generation planar SiC MOSFET power module, having a half-bridge configuration and rated at 1.2 kV/ 500 A. The DUT is driven by a +20 V/-5 V gate voltage and the used gate resistance is equal to 10 Ω.

The experimental approach includes two parts: (i) static characterizations and (ii) SC tests, as shown in Fig. 3 and Fig. 4. Initially, the static characteristics are measured before the first SC test, including threshold voltage (V_{th}), gate leakage current (I_{GSS}), drain leakage current (I_{DSS}) and on-state resistance ($R_{DS,on}$). Then, the SC test is performed, and the drain-source voltage (V_{DS}), gate-source voltage (V_{GS}) and drain current (I_D) waveforms are recorded. At the end of every test, a static characterization of the device is performed, then, the pulse time duration is increased gradually with fixed drain-source voltage (500 V) and room temperature. The SC test is stopped when a clear variation of the static characteristics is observed or the acquired SC waveforms show a clear gate damage (i.e. V_{GS} drops).

Based on this experimental procedure, the results of the static characteristics after each SC test will be compared with the previous one. As can be seen in Fig. 3, when the pulse time duration (t_{SC}) increases from the blue line to the green line, there is no obvious

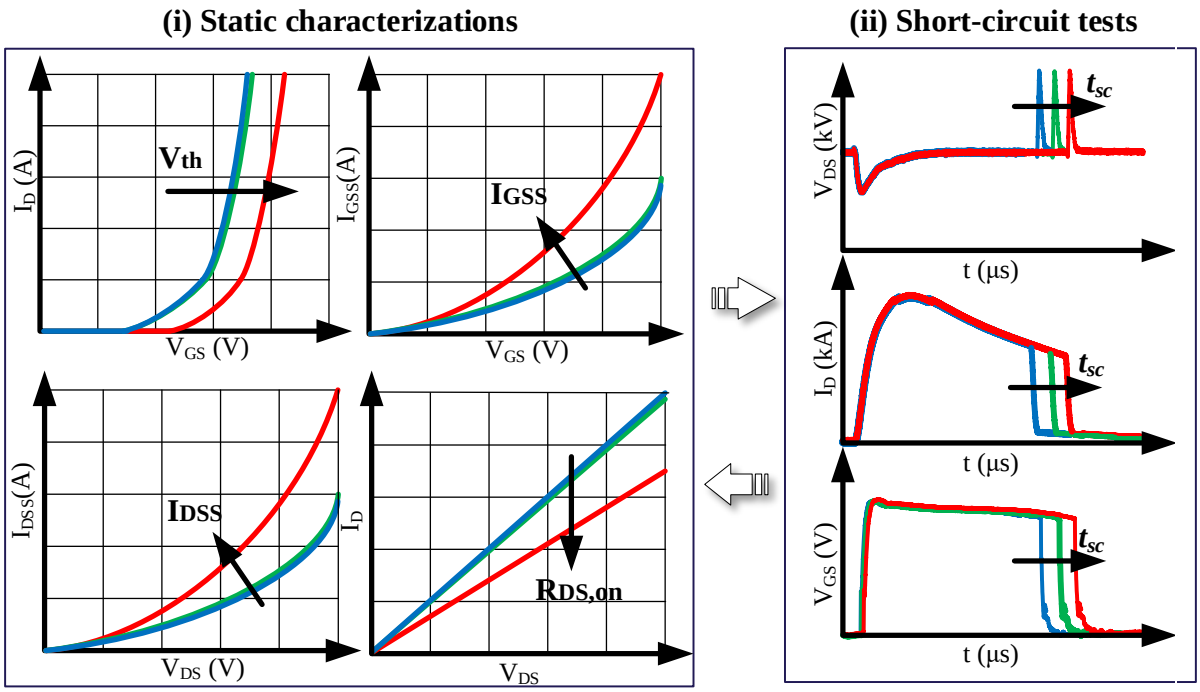

Fig. 3. Schematic of experimental approaches combined with both SC tests and static characteristics.

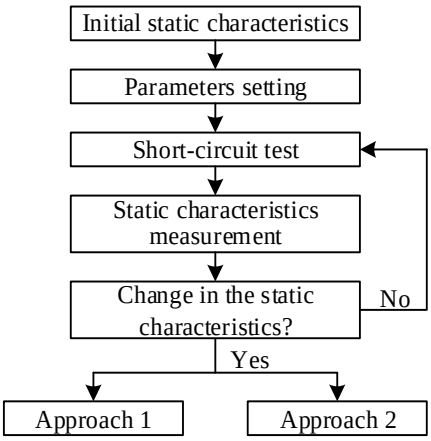

Fig. 4. Flow chart of experimental approaches combined with both SC tests and static characteristics.

change in the static characteristics. Thereafter, if the pulse time duration of SC test is further increased (from the green line to the red line), the variation of the static characteristics might be more obvious. At this point, two approaches are followed as shown in Fig. 4.

One approach named in the following as approach 1 is to keep the last SC pulse duration (t_{SC}) and repeat the SC test with the same t_{SC} again and again. If the variation on the static characteristics gradually changes in the same direction, this t_{SC} can be recognized as the critical time at the fixed bias voltage and temperature condition.

The second method named as approach 2 is to increase the t_{SC} continuously no matter if there is any variation of the static characteristics. This approach allows to investigate the intrinsic SC duration limit at a given DC voltage.

3. Experimental results and discussion

3.1. Approach 1

At first, the pulse time duration (t_{SC}) of SC test is increased gradually from 1 µs to 10 µs in steps of 1 µs showing no obvious change of the SC waveforms or static characteristics. A little change on the static characteristics appears for the first time at t_{SC} = 11 µs. However, a more obvious change has been recorded when the SC time duration is set to 11.2 µs. This t_{SC} is considered as the critical SC time, thus, the pulse time is no longer increased and several SC tests have been performed again and again at the same conditions.

The drain-source voltage (V_{DS}), gate-source voltage (V_{GS}) and drain current (I_D) during SC tests when the pulse time duration (t_{SC}) is equal to 11 µs and repetitive 11.2 µs are presented in Fig. 5. The

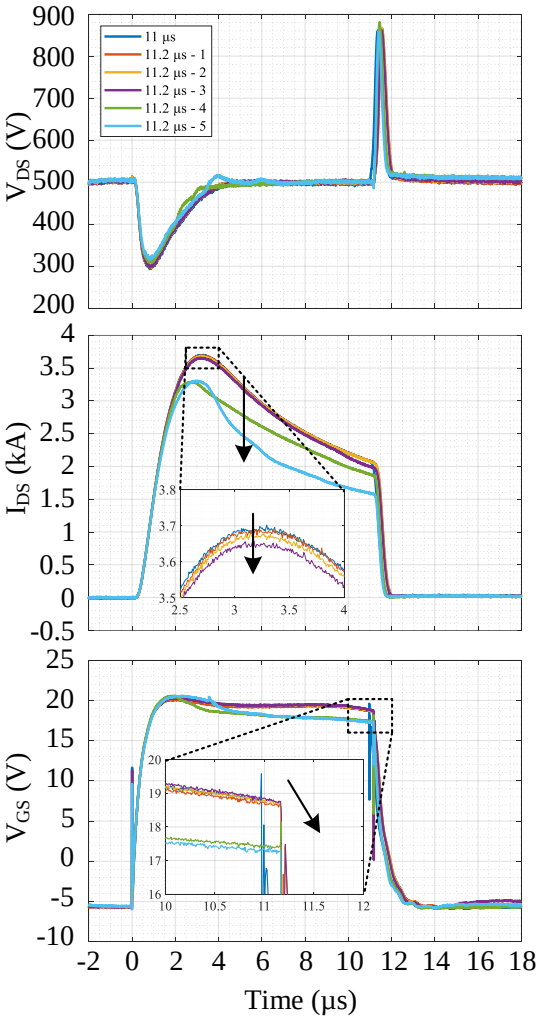

Fig. 5. Drain-source voltage (V_{DS}), drain current (I_D) and gate-source voltage (V_{GS}) waveforms at repetitive SC tests with 11.2 µs pulse time duration (V_{DS}=500V).

critical energy (E_C) is 13.83 J at 11.2 µs.

It can be observed that the on-state gate voltage amplitude clearly decreases from the fourth repetition to the fifth repetition. Meanwhile, a reduction of drain current is observed especially in the fourth and fifth repetitions, which is in agreement with the decreasing gate-source voltage.

The formulated hypothesis is that the gate voltage drop corresponds to a gradual increase in the gate leakage current originating from conductive paths which are formed through the oxide during the SC tests and eventually cause a permanent gate damage. This is also consistent with the reduction of the SC current as presented in Fig. 5. Moreover, the observed variation of V_{GS} and I_D are in agreement with the results observed for discrete devices in [10] and [11], which are related to the degradation of gate structure.

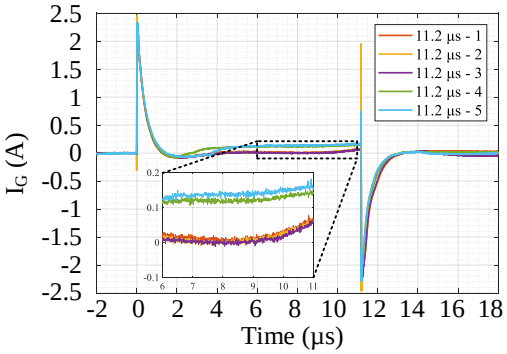

Fig. 6. Calculated gate current (I_G) waveforms from the first to fifth repetitive SC test at 11.2 µs (V_{DS}=500V).

Besides, another voltage probe is placed before the external gate resistance (R_G = 10 Ω) and the gate-source voltage including the R_G is measured during the SC tests in order to obtain the voltage drop on the R_G. Then, the gate current (I_G) during SC tests can be calculated with the value of the gate resistance and the measured voltage drop across the gate resistance. Fig. 6 shows the gate current waveform with increasing SC repetitions. It is worth to note that the gate leakage current increases from 68 mA for the first repetition up to 160 mA for the fifth repetition at bias voltage of 500V and SC time duration of 11.2 µs.

After each SC test, the static characteristics are measured, including the threshold voltage (V_{th}), the gate leakage current (I_{GSS}), the drain leakage current (I_{DSS}) and the on-state resistance ($R_{DS,on}$) which are presented from Fig. 7 to Fig. 10.

In Fig. 7, the threshold voltage shifts positively after each SC test at 11.2 µs. Because of the increased oxide conductivity, the effective gate voltage on the device is slightly reduced when the threshold voltage is measured, which ends up in an equivalent threshold voltage shift.

The results of Fig. 8 confirm that the gate leakage current increases gradually. An obvious increase of I_{GSS} is observed after the second SC test at 11.2 µs, which keeps increasing after each SC test, resulting in 0.1 A with the fifth repetitive SC test at 11.2 µs.

Similarly, the drain leakage current and the on-state resistance increases after the third SC test at 11.2 µs, as shown in Fig. 9 and Fig. 10, respectively. These results indicate that the gate degradation in turns affects the drain leakage path and leads to the reduction of V_{GS} when the I_D-V_{DS} characteristics (on-state resistance) is measured.

3.2. Approach 2

The second approach consists in increasing the SC time, even if the static characteristics vary. The

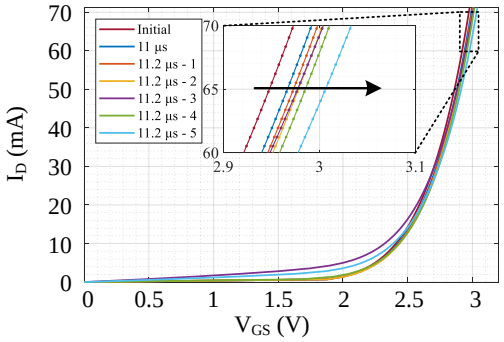

Fig. 7. Threshold voltage shifts after repetitive SC tests at 11.2 µs (V_{DS}=20V).

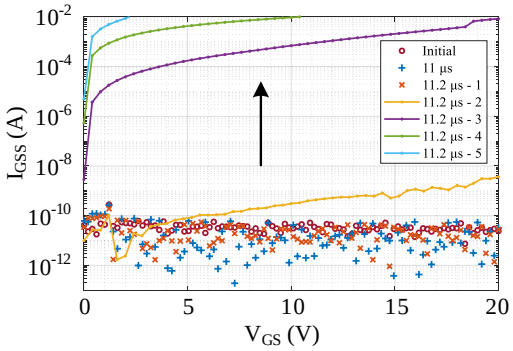

Fig. 8. Gate leakage current increases after repetitive SC tests at 11.2 µs.

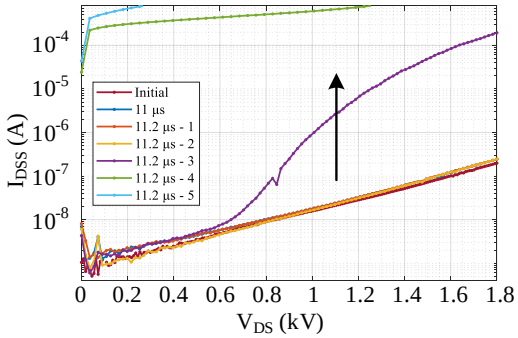

Fig. 9. Drain leakage current increases after repetitive SC tests at 11.2 µs.

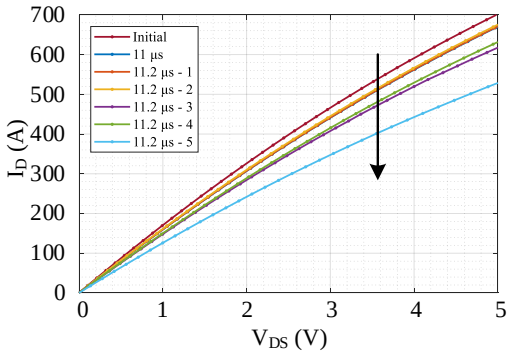

Fig. 10. On-state resistance increases after repetitive SC tests at 11.2 µs (V_{GS}=20V).

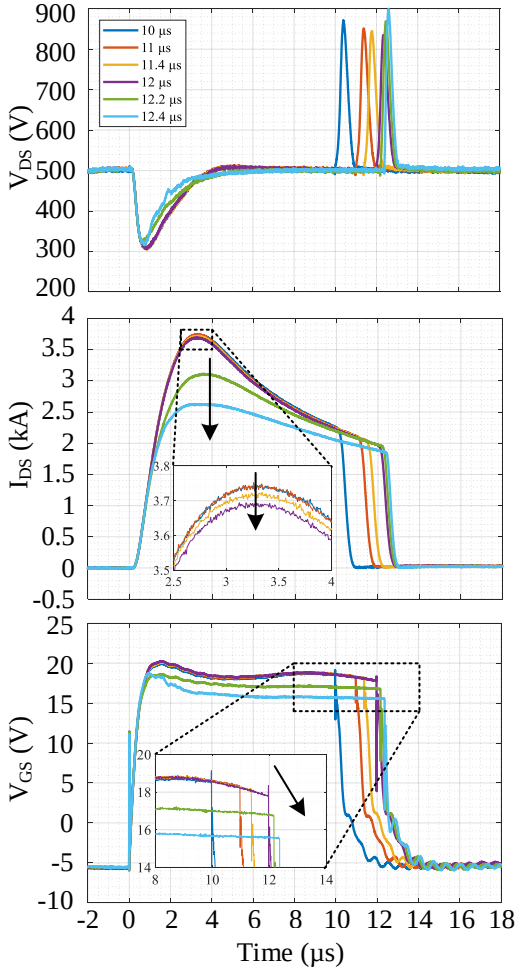

Fig. 11. Short-circuit waveforms including drain-source voltage (V_{DS}), drain current (I_D) and gate-source voltage (V_{GS}) from the experiment at 10 µs to 12.4 µs.

drain-source voltage (V_{GS}), gate-source voltage (V_{GS}) and drain current (I_D) waveforms during the SC tests from 10 µs to 12.4 µs are shown in Fig. 11. The t_{SC} was stopped at 12.4 µs because of a large V_{GS} drop.

The static characteristics measured after each SC test show a positive shift of the threshold voltage and the increase of drain leakage current as they are presented in Fig. 12 and Fig. 13, respectively.

The results of the SC waveforms and the static characteristics show the same trends when compared to the first approach, which also confirms the formulated hypothesis of gate degradation.

Besides, the reduction of the drain current during SC tests is verified by the gate-source voltage decrease according to the Eq. 1 when the V_{DS} is much larger than (V_{GS} - V_{th}).

$$I_D=\frac{1}{2}\cdot\kappa\cdot(V_{GS}-V_{th})^2 \quad (1)$$

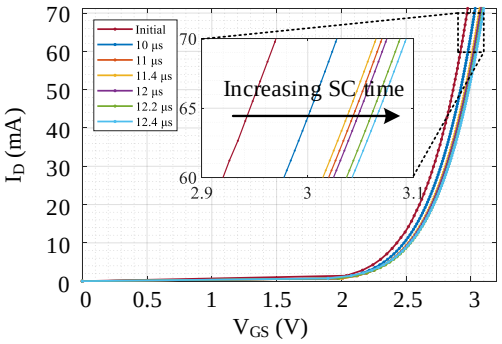

Fig. 12. Threshold voltage shifts vs. SC time duration (V_{DS}=500V).

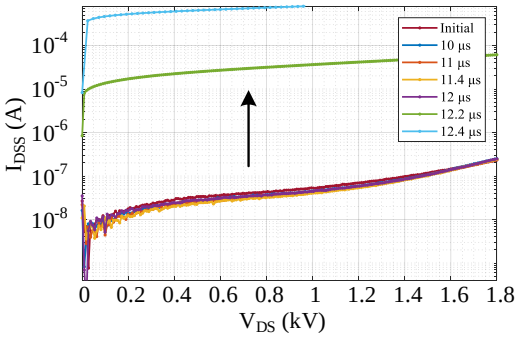

Fig. 13. Drain leakage current vs. SC time duration (V_{DS}=500 V).

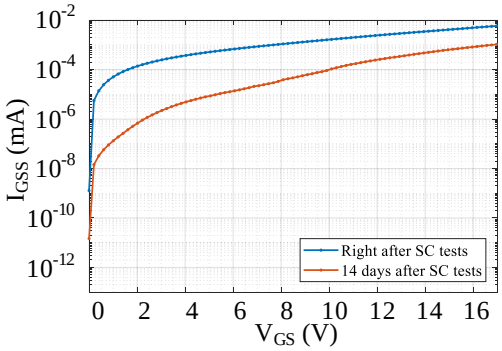

Fig. 14. Gate leakage current decreases 14 days after the last SC test.

The value of κ calculated by the SC waveform of approach 2 at 12 µs is 27.48 when the drain current (I_D) achieves the peak. In this case, the I_D is 3.695 kA and the V_{GS} at this moment is 19.480 V (V_{th} is equal to 3.08 V after this SC test).

Then, for the SC test at 12.2 µs, the V_{GS} is 18.154 V (V_{th} is equal to 3.093 V) and the I_D calculated by the same κ is 3.116 kA, which is consistent with the experimental result (3.117 kA). Similarly, the calculated I_D (2.586 kA) from the SC test at 12.4 µs agrees with the experimental results (2.630 kA), when the V_{GS} is 16.820 V and the V_{th} is 3.099 V.

4. Room-temperature recovery

The static characteristics of DUT have been measured again 14 days after the last SC test. The variation of gate leakage current, compared with the results obtained right after the SC tests, are shown in Fig. 14.

The results shown in Fig. 14 indicate that the gate oxide damage has a recovery trend. According to the literature, bias-temperature stress-activated defects partially can take place and recover at room temperature in time scales of weeks [12] and the room-temperature recovery would be extensively studied as the next step.

5. Conclusions

This paper shows the impact of the short-circuit events on the static characteristics of SiC MOSFET power module with 2nd generation and planar technology. The degradation indicators, including the positive shift of threshold voltage, the increase of gate leakage current, drain leakage current and on-state resistance, are analysed following two approaches. The first approach is to apply the same short circuit pulse once a variation of the static characteristics is detected. The second approach is to gradually increase the short circuit pulse even if the static characteristics vary. The results of both approaches show the same trends and confirm that the gate structure can become degraded with a few short circuit tests. The hypothesis of a conducting path formed through the oxide is confirmed by experimental measurements. The gate leakage current is measured again after 14 days, proving that a bias-temperature stress-activated defects come into play.

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