Bias temperature instability and condition monitoring in SiC power MOSFETs

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Abstract

Threshold voltage shift due to bias temperature instability (BTI) is a major concern in SiC power MOSFETs. The SiC/SiO_2 gate dielectric interface is typically characterised by a higher density of interface traps compared to the conventional Si/SiO_2 interface. The threshold voltage shift that arises from BTI has significant implications on the reliability of SiC power MOSFETs, hence, techniques for detecting the change in electrical parameters due to gate oxide degradation are desirable. Using accelerated high temperature gate bias stress tests on SiC MOSFETs, it has been shown that the output and transfer characteristics are affected by BTI. This paper presents the impact BTI induced threshold voltage shift on the forward voltage of the SiC MOSFET body diode during third quadrant operation. Using the forward voltage of the body diode during reverse conduction of low currents, threshold voltage shift can be detected, hence, the impact of BTI can be evaluated. The implications of the body diode forward voltage shift on junction temperature measurements are also studied in the context of TSEPs. The findings in this paper are important for engineers seeking to implement condition and health monitoring techniques on SiC power devices.

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1. Introduction

The advantages of SiC MOSFETs over their silicon counterparts are well known and documented, however, lingering reliability questions regarding the performance of the gate dielectric under Bias Temperature Instability (BTI) and Time Dependent Dielectric Breakdown (TDDB) remain [1, 2]. The presence of carbon atoms during the thermal oxidation of SiC causes a SiC/SiO_2 interface with higher magnitudes interface trap density and oxide charges compared with the traditional Si/SiO_2 interface [3]. Furthermore, the smaller band offsets at the SiC/SiO_2 interface means there is a reduced barrier for carriers to scale and contribute to gate leakage current and gate dielectric degradation.

As a result of the SiC/SiO_2 interface, threshold voltage instability and early gate oxide breakdown are known reliability concerns in SiC MOSFETs. BTI contributes to threshold voltage instability and is due to trapped charges in the oxide and its interface [3, 4].

This paper investigates the degradation of the gate oxide of SiC power MOSFETs under high temperature gate bias (HTGB) and analyses its impact on the electrical characteristics of the power device. Understanding how the degradation of the gate oxide affects the electrical parameters of the SiC power MOSFETS would be fundamental for defining gate oxide reliability indicators and implementing gate oxide monitoring strategies.

2. HTGB Stress in SiC MOSFETs

In the study presented in this paper, high temperature gate bias (HTGB) has been used for accelerating the degradation of SiC power MOSFETs, following the approach presented in [5], where HTGB tests were used for obtaining a prediction of the lifetime using the integrity of the gate oxide and the threshold voltage shift of SiC MOSFETs. The approach in this investigation uses accelerated gate bias stress tests to obtain a degraded oxide after which the electrically degraded MOSFET is characterised. The objective here is to measure non-recoverable gate degradation which means that a long relaxation time (4 to 24 hrs) is used to ensure that the captured carriers in the interface and fixed oxide traps are released. During the stress test, the drain and source terminals of the MOSFET were shorted and during the relaxation phase, the gate and source terminals were shorted while the device was cooled down to the ambient temperature, as shown in Figure. 1

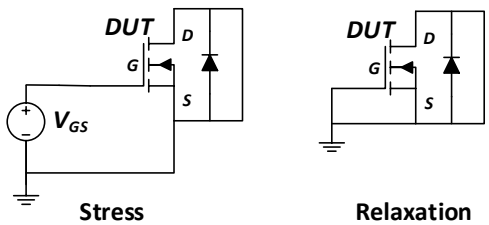

Fig. 1. Electrical schematic of the HTGB test during the stress and relaxation phases

Table 1 Gate voltages used for the HTGB stress tests. Output and transfer evaluation

Positive HTGB (1 hour stress, T=150 °C)	Negative HTGB (1 hour stress, T=150 °C)
+20 V to +40 V	-10 V to -40 V

The device evaluated in this study is a trench SiC MOSFET, which seems to be the gate structure adopted by different manufacturers in their latest generation devices. The devices were initially studied under positive and negative HTGB using the gate voltage ranges given in Table I. The temperature T of the device (150 °C in these tests) was set using a small DC heater attached to the device. Using the test setup previously described, discrete SiC trench MOSFETs were subjected to both positive and negative HTGB cumulative stress tests. The devices were characterised at ambient temperature (output, transfer and 3rd quadrant characteristics) using a curve tracer Tektronix model 371B, after each stress step and a minimum relaxation time of 4 hours with V_{GS}=0.

In [2, 4, 6] it is stated that the threshold voltage shift recovers with time, however, the rate of recovery is higher when a gate voltage of opposite polarity is applied or the gate is shorted to the source (V_{GS}=0). In this study, V_{GS}=0 is used to ensure that only non-recoverable shifts are characterised.

2.1. Transfer and output characteristics

The transfer characteristics are shown in Fig. 2(a) for cumulative positive HTGB stress and Fig. 2(b) for cumulative negative HTGB stress. In Fig. 2, it can be observed that the magnitude of non-recoverable V_{TH} shift generally increases with the magnitude of V_{GS} bias. As reported in literature [3, 4], V_{TH} increases with positive bias and decreases with negative bias. Evaluating the measurements, the shift in the transfer characteristics caused by the negative stress is more apparent than the shift caused by the positive stress. From the stresses presented in Fig. 2 it can be observed that for the lower V_{GS} stresses the shift of V_{TH} recovers after the relaxation phase, before characterization. This is particularly apparent in the case of the NBTI stresses, as shown in Fig. 2(b).

The output characteristics, for the maximum cumulative gate stress are shown in Fig. 3(a) for the positive HTGB and Fig. 3(b) for the negative HTGB. In both figures, the output is presented for both high and low gate-source voltages.

First, analysing the impact of both positive and negative BTI, from the results presented in Fig. 3, it is clearly observed how the on-state resistance increases due to PBTI and reduces due to NBTI. As stated in [3], the increase of the on-state resistance due to PBTI causes an increase of the on-state losses and reduction of the overdrive voltage in the on-state and whereas the reduction of the on-state resistance will cause a reduction of the on-state losses.

The negative shift of V_{TH}, as shown in Fig. 2, can have serious implications in the reliability, as the parasitic turn-on caused by high dV/dt could be easily triggered due to the lower V_{TH}, increasing the power dissipated on the MOSFET [7]. In the case of power modules where chips are paralleled for increasing the current capability, which is a common practice for SiC MOSFETs, if the threshold voltage shift caused by BTI is uneven both positive and negative shifts could have an impact on the performance and reliability of the power module.

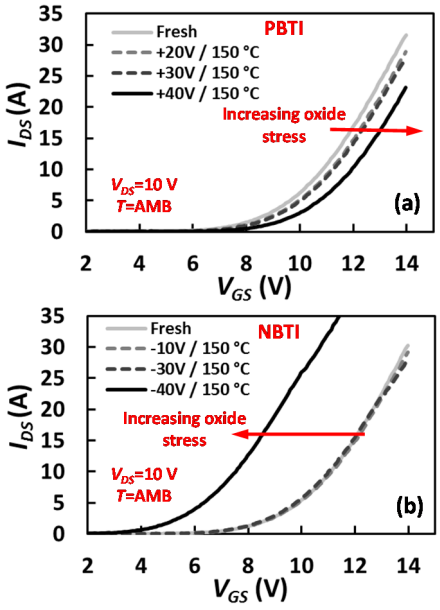

Fig. 2 Transfer characteristics of a SiC Trench MOSFET (Set 1): (a) After positive HTGB stress (b) After negative HTGB stress

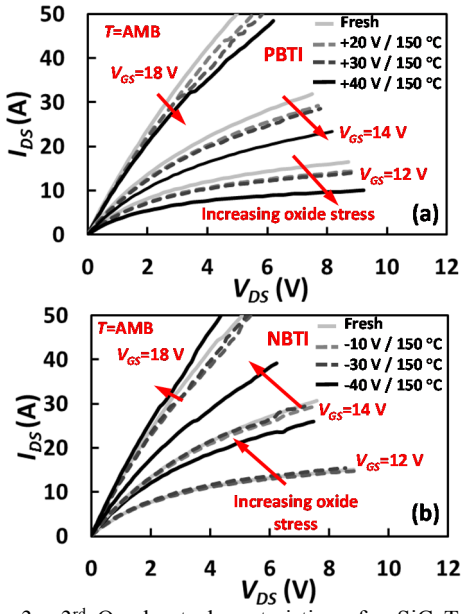

Fig. 3. 3rd Quadrant characteristics of a SiC Trench MOSFET. (Set 1): (a) After positive HTGB stresses (b) After negative HTGB stresses

Looking at the measurements in Fig. 3, it can be observed that the impact of the degradation of the gate oxide (threshold voltage shift) is more apparent at low V_{GS} than at high V_{GS}. This is due to that fact that the ON-state resistance is more sensitive to V_{TH} at low V_{GS} where the channel resistance dominates the drift resistance. This fact could be used for improving gate oxide condition monitoring strategies based on the on-state resistance, as will be shown in section 3.

2.2. Body diode characteristics

Due to the higher built-in voltage of a SiC PN junction, the body effect is more apparent in SiC MOSFETs, causing a lower on-state voltage V_{ON} of the body diode in reverse conduction, when the gate is biased at V_{GS}=0 [8]. In this situation, an inversion channel is formed because of the positive potential appearing at the p-body to n$^-$-SiC interface. A more detailed explanation is given in [8, 9]. The HTGB stress tests affect V_{TH}, hence it is important to evaluate how BTI affects the 3rd quadrant characteristics of SiC MOSFETs.

Fig. 4 shows the 3rd quadrant characteristics for a new set of SiC trench MOSFETs measured at V_{GS}=0 and both cumulative positive and negative stresses of 30 minutes duration, as defined in Table 2. The minimum recovery time for this set of measurements was 15 hours. The positive HTGB stress causes an increase of the forward voltage of the body diode while a negative HTGB causes a reduction of the forward voltage. The impact of BTI is more apparent for the negative stresses. Gate voltages higher than recommended values have been used to accelerate oxide aging.

Table 2 Gate voltages used for HTGB stress tests. Body diode evaluation

Positive HTGB (30 minutes, T=150 °C)	Negative HTGB (30 minutes, T=150 °C)
+35 V / +35 V/ +40 V	-35 V /-35 V/ -40 V

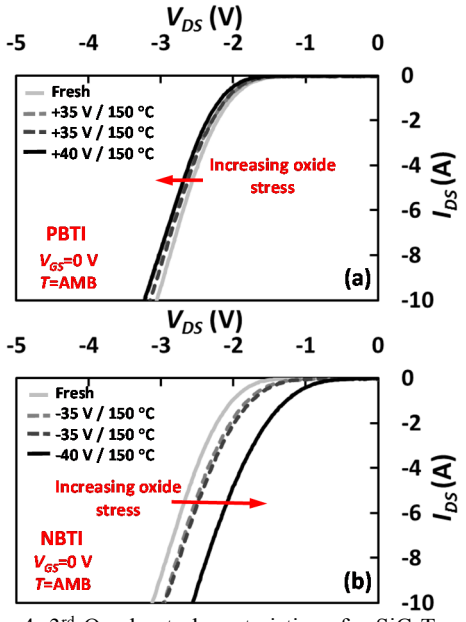

Fig. 4. 3rd Quadrant characteristics of a SiC Trench MOSFET (Set 2): (a) After positive HTGB stresses (b) After negative HTGB stresses

3. Implications for Condition Monitoring

Very recent work on this topic has been presented in [10] for Si power MOSFETs. In this section, the on-state resistance and the 3rd quadrant characteristics are evaluated as indicators of gate oxide degradation for SiC MOSFETs.

3.1. On-state resistance as indicator of V_{TH} shift

Compared with Si power MOSFETs, in SiC MOSFETs, the channel resistance R_{CH}, has an important contribution to the total on-state resistance of device [3]. Its value given by Eq. 1, where L_{CH} is the length of the channel, W the channel width, μ_n the electron effective mobility, C_{OX} the gate oxide capacitance density and V_G the gate driving voltage.

$$R_{CH} = \frac{L_{CH}}{W\mu_n C_{OX}(V_G - V_{TH})} \quad (1)$$

If the gate driving voltage V_G is reduced, the value of the channel resistance increases and the impact of the shift of the threshold voltage V_{TH} caused by BTI on the on-state resistance will be more apparent. This is similar to the improvement of the temperature sensitivity of determined electrical parameters presented in [11]. This is shown for the NBTI stresses

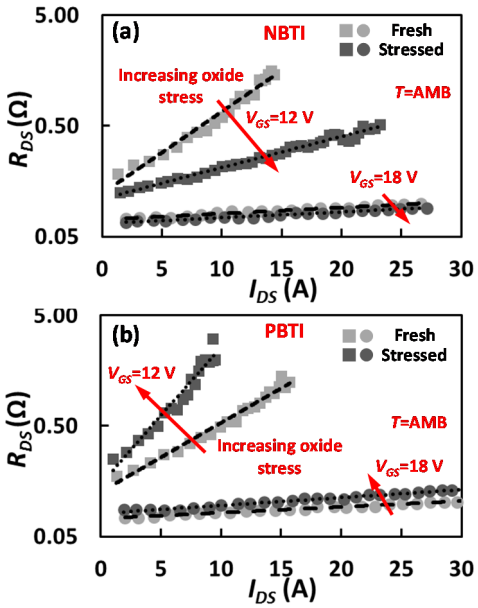

Fig. 5. Impact of V_{TH} shift due to BTI on the on-state resistance. SiC trench MOSFET (a) NBTI (b) PBTI

in Fig. 5(a), where the on-state resistance has been obtained using the output characteristics for the fresh and highly degraded MOSFET shown in Fig. 3(b). The measurements are shown for both V_{GS}=12 V and V_{GS}=18 V. Similar results are obtained for the PBTI stresses, but the resistance increases due to BTI instead of reducing, as shown in Fig. 5(b).

Analysing the results shown in Fig. 5, it can be seen that driving the MOSFET with a lower gate voltage (thereby increasing the contribution of the channel resistance to the total on-state resistance) makes the impact of V_{TH} shift more apparent, especially if the MOSFET is driven into saturation. Increasing the on-state resistance will cause higher conduction losses, hence the use of intelligent gate drivers, capable of generating customized pulses for gate oxide monitoring would be beneficial. Finally, it is important to mention the on-state resistance of a SiC MOSFET is a Temperature Sensitive Electrical Parameter (TSEP) [11, 12] and its value is affected by temperature, hence the use of $R_{DS\text{-}ON}$ as indicator of gate oxide reliability will require identifying the temperature by other means or decoupling the impact of temperature and gate oxide degradation.

3.2. Body diode voltage as indicator of V_{TH} shift

In the case of the SiC MOSFETs, the body diode voltage V_{SD} appears to be a good indicator of gate oxide degradation under BTI, as the results in Fig .4 show. Using this parameter as an indicator of gate oxide degradation requires further assessment because V_{SD} is affected by the operating junction temperature, as it is a well-known and established TSEP. The impact of the junction temperature on V_{SD} at low currents as the oxide stress increases is shown in Fig. 6. In this figure, it is clearly observed that the degradation of the gate oxide affects the calibration curves of the TSEP, measured here for a current of 50 mA using a digital multi-meter model HMC8012 from Hameg. The positive HTGBs stress shifts the calibration curve upwards, as shown in Fig. 6(a), while the negative HTGB stress shifts the curve downwards, as presented in Fig. 6(b), hence the accuracy of the junction temperature measured using V_{SD} as a TSEP can be affected.

Fig. 6 shows the measured V_{SD} for both gate-source voltages of 0 V and -4 V. In the case of using -4 V, the body effect is minimized, as the increase of V_{SD} indicates. The impact of the BTI on the temperature sensitivity of the TSEP is reduced since the measured V_{SD} is less sensitive to oxide stress state. This is particularly effective in the case of the PBTI stress, as the results in Fig. 6(a) show. Hence, it is highly recommended that V_{SD} is measured with a negative V_{GS} if V_{SD} is to be used as a TSEP, as was also stated in [13]. In the case of PBTI, at V_{GS}= 0V, the shift of the calibration curve is +0.20 V while at V_{GS}= -4 V the increase is +0.03 V. For the NBTI measurements, the shifts are –0.84 V and -0.54 V for V_{GS} = 0 V and V_{GS} =-4 V respectively.

Finally, it is important to mention that if the temperature is known, the forward voltage at low currents can be used as a cursor of threshold voltage shift/gate oxide degradation.

The transfer characteristics corresponding to the 3rd quadrant characteristics shown in Fig. 4 are presented in Fig. 7. From the transfer characteristics measured at ambient temperature, it is possible to extract the threshold voltage [14], hence a relationship between

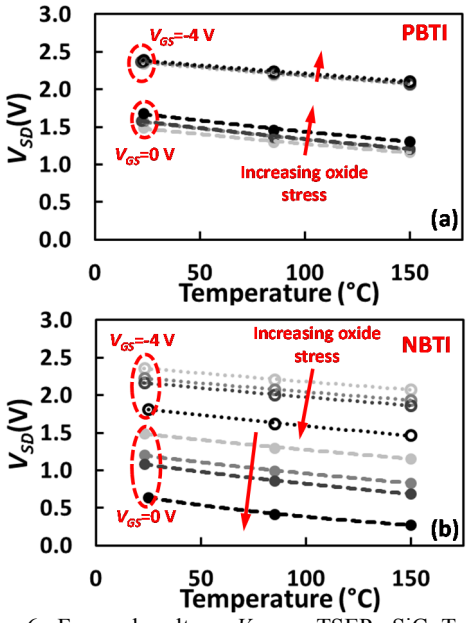

Fig. 6. Forward voltage V_{SD} as TSEP. SiC Trench MOSFET (a) Negative HTGB stress, (b) Positive HTGB stress

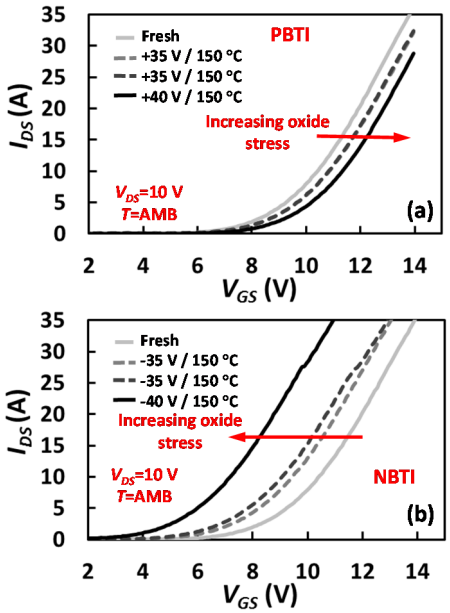

Fig. 7. Transfer characteristics of a SiC Trench MOSFET (Set 2), (a) After positive HTGB stresses (b) After negative HTGB stresses

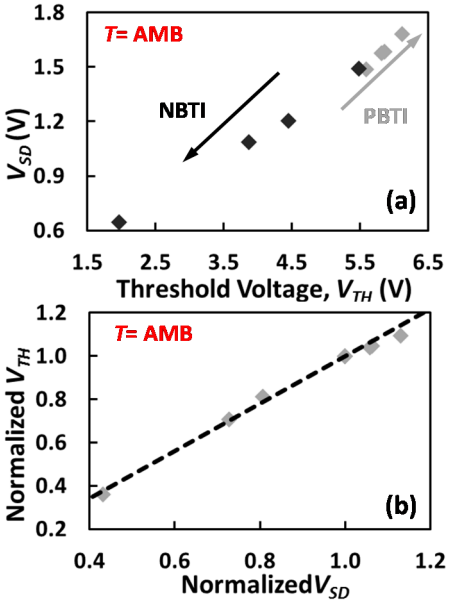

Fig. 8 (a) Extracted threshold voltage as a function of the measured V_{SD} for I=50 mA and V_{GS}=0. Ambient temperature (b) Normalized relationship between V_{SD} (I=50 mA, V_{GS}=0) and V_{TH} at ambient temperature

the threshold voltage shift due to BTI and the body diode voltage of the stressed SiC MOSFET can be defined. This relationship is based on the body effect, hence a gate voltage V_{GS}=*0* is used for maximizing the impact of the threshold voltage shift on the body diode voltage.

Fig. 8(a) shows the measured V_{SD} at 50 mA for both positive and negative stresses as a function of the extracted V_{TH}. Both values were measured at ambient temperature and V_{TH} was extracted using the current-to-square-root-of-transconductance-ratio method, as defined in [13]. A clear linear relationship between the shifts of V_{SD} and V_{TH} can be identified.

To reduce the effect of device variability on BTI shifts, both V_{TH} and V_{SD} were normalized as shown in Fig. 8(b). The relationship between the normalized V_{SD} and the normalized V_{TH} is given by Eq. 2, which can be used for estimating the normalized V_{TH} shift using the body diode voltage (measured at 50 mA).

$$V_{TH,nor} = 1.1 \cdot V_{SD,nor} - 0.1 \qquad (2)$$

4. BTI and V_{TH} shift characterization using the body diode

Comparing both the transfer characteristics after degradation presented in Fig. 2 and Fig. 7, the recovery of the threshold voltage shift can be clearly identified in the case of the BTI tests shown in Fig. 2. This indicates that biasing the device at V_{GS}=0 and with enough relaxation time, the threshold voltage shift can recover. Moreover, this also highlights an issue that arises from this recovery and can have

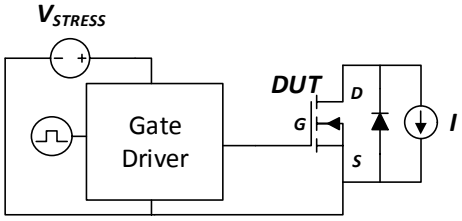

Fig. 9.Electrical schematic of the circuit for V_{TH} shift evaluation

serious implications for qualification of devices, as the measured V_{TH} shift may not be representative of the real shift caused by the stress [6] i.e. there may be some V_{TH} recovery in the time duration between the end of the test and the V_{TH} characterisation.

One of the novel features regarding the use of V_{SD} as an indicator of BTI is its use for monitoring the V_{TH} shift similarly to its use as a TSEP (based on equation 2). This can be done using the basic test setup shown in Fig. 9, which consists in a gate driver circuit where the supply voltage is the stress voltage V_{STRESS} and the duration of the stress is controlled using a low voltage pulse generated using a waveform generator. A constant sensing current is continuously circulating through the source-drain terminals and is used for sensing the V_{SD} before and after V_{STRESS} is applied. The circuit can be used for evaluating PBTI and NBTI induced V_{TH} shifts, just by changing the polarity of the stress. Once V_{STRESS} is removed, the voltage V_{GS} is 0, and the measured V_{SD}, can be used for estimating the threshold voltage shift, due to the body effect. V_{SD} was measured using a differential probe model TA043 from Pico Electronics and an oscilloscope model TDS5054B from Tektronix.

The operation of the method is shown in Fig. 10 for both positive and negative stresses, where the normalized V_{TH} has been calculated using Eq. 2. In the case of the positive stress, as shown in Fig. 10(a) for V_{STRESS}=20 V, when the V_{GS} is high, the measured V_{SD} is low, since the MOSFET is ON. When the V_{GS} is turned-OFF, the channel is cut-off, hence V_{SD} is high again. The positive shift of V_{TH} caused by BTI is indicated by an increase of V_{SD} with respect to the initial value, which recovers with time, as shown in the figure.

In the negative stress, as shown in Fig. 10(b) for V_{STRESS}=-26 V, when the V_{GS} is negative, V_{SD} increases due to the body effect. Once the stress is removed, the negative shift of V_{TH} is indicated by a dip of V_{SD} with respect to the initial value. The recovery of V_{TH} with time is clearly observed and is opposite to PBTI.

During the stress pulse, the self-heating can be neglected (due to the low sensing current) and the variation of V_{SD} can be attributed to the change of V_{TH} due to BTI. The main benefit of this simple method is that it allows the observation of V_{TH} recovery due to BTI in a non-intrusive way, together with the initial $V_{TH,peak}$. This method requires a controlled

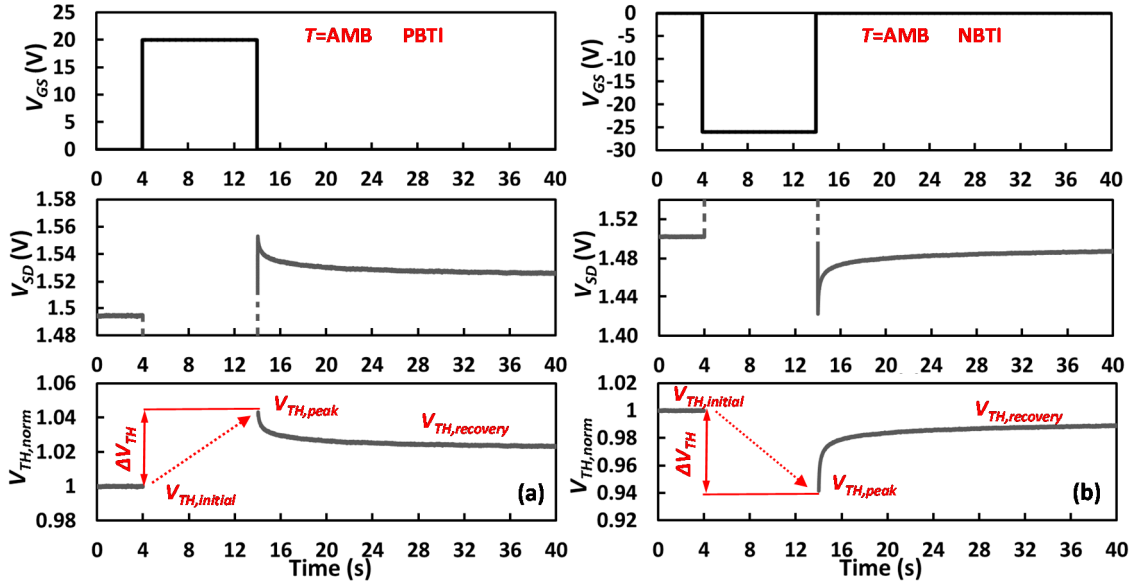

Fig. 10 (a) Gate stress voltage, V_{SD} voltage and normalized V_{TH} for PBTI, (b) Gate stress voltage, V_{SD} voltage and normalized V_{TH} for NBTI

temperature as V_{SD} as well as V_{TH} are both temperature dependent. It should however be noted that this technique of BTI characterisation will only work with SiC devices/modules that do not use an anti-parallel SiC diode, since the anti-parallel diode will prevent the flow of the sensing current through the body diode.

Conclusion

This paper evaluates the impact of the V_{TH} shift caused by BTI in highly accelerated stress tests. It affects both the on-state resistance and the 3rd quadrant body diode characteristics. If the device is driven in saturation, the higher contribution of the channel resistance makes the impact of V_{TH} shift more apparent and easier to identify. Due to the body effect, for a known temperature, there is a relationship between V_{TH} and V_{SD}, hence the 3rd quadrant characteristics can be used for identifying the initial threshold voltage shift and its consequent recovery once the stress is removed. The implementation of this method is easy and is similar to the use of V_{SD} as indirect temperature sensor, which makes its implementation for condition monitoring possible.

Acknowledgements

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