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Impact of carbon impurities on the initial leakage current of AlGaN/GaN high electron mobility transistors

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Abstract

We have systematically studied the origin of high gate-leakage currents in AlGaN/GaN high electron mobility transistors (HEMTs). Devices that initially had a low gate-leakage current (good devices) are compared with ones that had a high gate-leakage current (bad devices). The apparent zero-bias Schottky barrier height of bad devices ($0.4 < \phi_{B0} < 0.62$ eV) was found to be lower than that of the good devices ($\phi_{B0} = 0.79$ eV). From transmission electron microscopy (TEM) and electron energy loss spectroscopy (EELS) analysis, we found that this difference is due to the presence of carbon impurities in the nickel layer in the gate region.

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1. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) have a great potential to enable high power and high frequency electronics applications. While there has been some successful commercialisation of these devices, large scale market adoption has not yet been seen. This is partially due to an unclear understanding of the origin of low device fabrication yield and reliability, particularly of the origin of high gate-leakage currents [1].

High gate-leakage currents have been observed in devices after stressing under reverse bias at high temperatures [2]. Initially it was proposed that the increase in gate-leakage current is due to gate-edge degradation in the form of cracks, pits or grooves [3], [4]. However, later studies showed that this is not necessarily the case. Gate-edge degradation is not always accompanied by an increase of the gate-leakage current [5-9] and an increase of the gate-leakage current is not always accompanied by gate-edge degradation [10], [11].

More recently, an alternative explanation based on percolation path theory was proposed to explain increases in gate-leakage currents [10], [12]. This is consistent with the statistical distribution of this degradation. However, the nature of the physical defects associated with the formation of the percolation path is still unclear.

While there have been many studies of increases of gate-leakage due to stressing, there is still a limited understanding of the origin of initially high gate leakage currents in unstressed devices (i.e. bad devices). This understanding is important as it could be used as the basis for process optimization and therefore could lead to further yield improvements. Furthermore, without screening these devices from reliability test data, and underestimate the true reliability could result.

2. Experimental details

Figure 1 shows the layer structure of the devices used in this work. The epitaxial layers were grown using metal organic chemical vapor deposition (MOCVD). Device fabrication was carried out using conventional device processing that involved a gate lift-off process. After fabrication, these devices underwent thermal aging at 225°C for 500 h. Further details on the device dimensions and process parameters can be found in ref. [13].

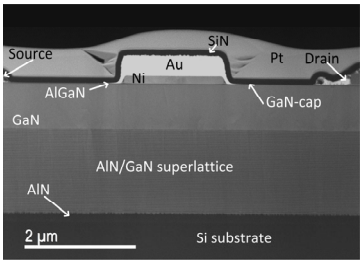

Figure 1. High angle annular dark field (HAADF) image of an AlGaN/GaN-on-Si high electron mobility transistor.

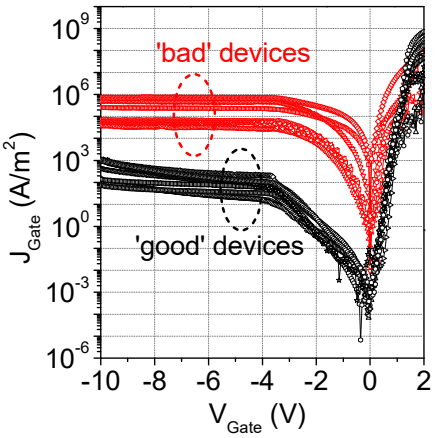

Figure 2. J_{Gate}-V_{Gate} curves (direct current, static) of bad devices (red) and good devices (black), measured at $V_{Drain} = 0$ V at room temperature.

We tested a total of 30 devices. 6 of these devices had a very high initial gate-leakage current density ($J_{Gate} > 5 \times 10^4$ A/m^2). We considered those to be 'bad' devices. The remaining had a very low leakage current density ($J_{Gate} < 2 \times 10^2$ A/m^2), and thus we considered those to be 'good' devices. J_{Gate}-V_{Gate} curves for these devices are shown in Figure 2.

Figure 3 shows I_{Drain}-V_{Gate} curves of good and bad devices. We can clearly see that bad devices have a much higher initial drain leakage current than good devices. The threshold voltage of both types of devices

is quite similar. Good devices have V_{th} = -2.6±0.2 V, while bad devices have V_{th} = -2.5±0.3 V. This suggests that there is no substantial difference in the trap level density below the gate.

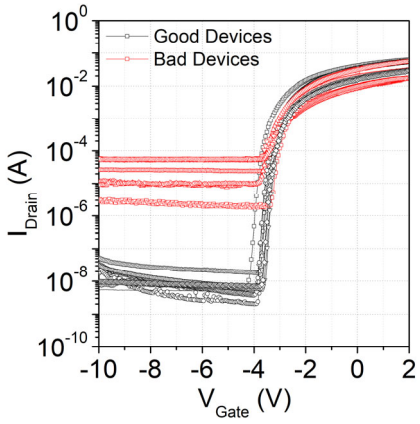

Figure 3. I_{Drain}-V_{Gate} curves (direct current, static) of bad devices (red) and good devices (black), measured at V_{Drain} = 10 V, at room temperature.

Bad devices used in this study are already considered 'failed' as fabricated, since their leakage current is very high, and therefore the failure time can be considered as t_F = 0. For good devices, we have carried out high temperature reverse bias tests and reported the results in [6]. In this test, the good devices do not experience any increase of the leakage current for > 500 h. Instead, devices fail due to a decrease of the maximum drain current, which can be explained by pit formation at the gate-edge. A similar failure mechanism was also observed for good devices stressed in the on-state, as we have also reported previously [7].

We employed various characterization techniques to understand the origin of high leakage currents in bad devices. Apparent zero-bias Schottky barrier heights (ϕ_{B0}) were extracted from J_{Gate}-V_{Gate} curves, photon emission microscopy was used to locate defects, transmission electron microscopy (TEM) was used to characterize the structure of defects, and electron energy loss spectroscopy (EELS) was used to characterize the chemical composition of the defects.

3. Results and discussion

We calculated the apparent zero-bias Schottky barrier height, ϕ_{B0}, using equation (1)[14],

$$\phi_{B0} = \frac{kT}{q}\ln\left(\frac{A^{**}T^2}{J_0}\right), \quad (1)$$

where q is the electron charge, k is the Boltzmann constant, T is temperature and A^{**} is the effective Richardson constant. J_0 is the reverse saturation gate leakage current density, which is obtained from a linear extrapolation of ln(J_{Gate}) vs.V_{Gate} as illustrated in Figure 4.

We also calculated the ideality factor of these devices, n, using equation (2),

$$n = \frac{q}{kT}\frac{\delta V_G}{\delta \ln(J_G)}, \quad (2)$$

where $\delta V_{Gate}/\delta \ln(J_{Gate})$ is obtained from the inverse slope of the linear portion of ln(J_{Gate}) vs V_{Gate} curve as shown in Figure 4.

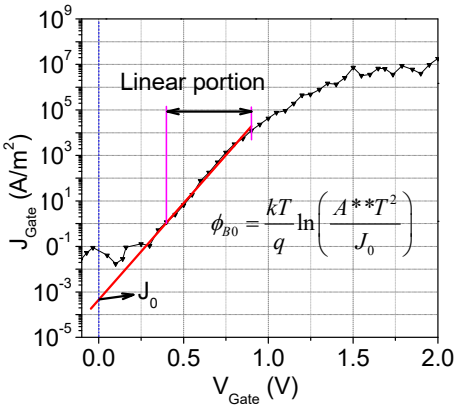

Figure 4. Method for determination of the apparent zero-bias Schottky barrier height (ϕ_{B0}) and ideality factor (n) from a J_G-V_G curve (V_G > 0 V).

Table1. Comparison of good and bad devices

Parameters	Good Devices	Bad Devices
V_{th} (V)	-2.6±0.2	-2.5±0.3
ϕ_{B0} (eV)	0.79±0.03	0.4 to 0.62
n	2.03±0.4	3.9±0.6
J_{Gate} (A/m^2)	<10^2	>10^4
# of devices	24 out of 30	6 out of 30

Table 1 summarizes the calculated parameters of good and bad devices. Good devices are seen to have apparent zero-bias barrier heights of ϕ_{B0} = 0.79 ± 0.03 eV. This is reasonably close to the value reported in the literature [15–17]. On the other hand, bad devices have substantially lower apparent zero-bias barrier heights, 0.4 < ϕ_{B0} < 0.62 eV. The ideality factor of all

devices (bad and good) is $n >> 1$. This value is commonly reported in the literature for AlGaN/GaN [17,18]. It indicates that the forward current mechanism is not only thermal emission. Other possible transport mechanisms are direct tunnelling and trap assisted tunnelling [17]. While this suggests that the true barrier height values may not be the same with apparent barrier height [18], this does not rule out the possibility that the true barrier height of bad devices is lower than that of good devices. As we will latter show, this is supported by our observation of locally high carbon content in the nickel layer at the locations that have high leakage currents.

From Arslan *et al.* [18] and Donoval *et al.* [19], it is reasonable to conclude that the true barrier height does not change at different temperatures. While the apparent barrier height increased with temperature, the reverse leakage current of their devices remained relatively constant. Furthermore, they showed that the high tunnelling current they observed was the result of the presence of threading dislocations that are uniformly distributed throughout the Schottky contact. In our case, the reverse leakage current of bad devices is much higher than that of the good devices. Instead of observing high emission uniformly throughout the whole Schottky contact area, the high leakage current is emitted locally. We also do not observe differences in the threading dislocation density at these locations compared with other locations that do not emit high leakage currents. One likely explanation for our measurement of high overall leakage currents is a local lowering of the barrier height of bad devices at a few locations with orders of magnitude higher emissions.

Figure 5 shows the calculated apparent zero-bias Schottky barrier height plotted against the measured J_{Gate}. It is apparent that J_{Gate} increases exponentially with a decrease of ϕ_{B0}. This is consistent with the well accepted understandings of current transport mechanisms in Schottky diodes. As the zero-bias barrier height decreases, it is easier for electrons to flow across the interface via some of the possible current transport mechanisms, which include Schottky emission, Fowler-Nordheim tunnelling and/or Poole-Frenkel tunnelling [14].

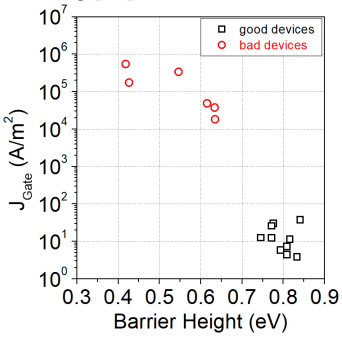

Figure 5. J_{Gate} as a function of the apparent zero-bias barrier height (ϕ_{B0}). J_{Gate} values were measured at V_{Gate} = -3 V.

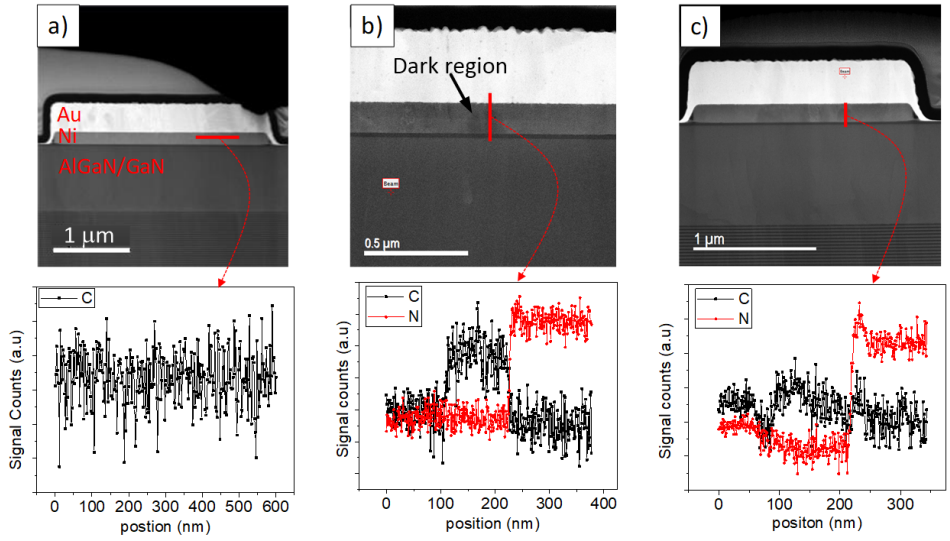

Figure 7. High angle annular dark field (HAADF) images and electron energy loss spectroscopy line scan of devices at different locations. a) A good device, b) a bad device at a hotspot, and c) a bad device at a non-hotspot location.

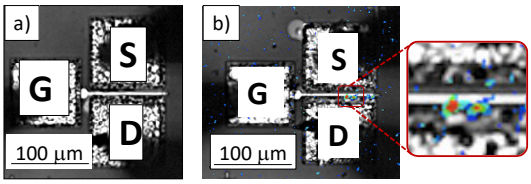

Figure 6. Photon emission microscopy images of devices operating at V_{Gate} = -10 *V*, V_{Drain} = 0 *V* at room temperature. a) A good device that has a low gate leakage current, b) A bad device that has a high gate leakage current.

To further investigate the physical origin of high initial leakage currents, we used photon emission microscopy to spatially localize high gate leakage current regions. Figure 6 shows a comparison of a good device with a bad device operating under a constant reverse bias. In good devices, we did not observe photon emission under constant reverse bias. However, in bad devices we consistently observed one or more localized sites of high photon emission, commonly referred to as hotspots. The locations of these hotspots were random along the gate.

Knowledge of the location of the hotspots guided us in sample preparation for transmission electron microscopy analysis. Figure 7 shows a series of high angle annular dark field (HAADF) images and respective elemental composition analyses made using electron energy loss spectroscopy (EELS). In bad devices at hotspots, we consistently observed dark regions in the nickel layer. These dark regions contain a significant amount of carbon as an impurity in the nickel (Fig. 7b). In good devices, we did not observe these dark regions (Fig. 7a).

Carbon has a lower work function (ϕ_{Carbon} = 4.6 eV) than nickel (ϕ_{Nickel} = 5.2 eV) [20]. It has also been reported that the effective work function decreases as carbon content increases in Nickel [21]. In a Schottky metal-semiconductor contact like in the case of devices used in this work, zero-bias barrier heights (ϕ_{B0}) decrease with decreasing work function (ϕ_m) according to equation (2) [14],

$$\phi_{B0} = \phi_m - \chi, \tag{2}$$

where χ is the electron affinity of the semiconductor. Work function lowering due to carbon impurities explains why bad devices have lower effective barrier heights and therefore higher gate-leakage currents.

We postulate that one possible source of carbon is photoresist residue (hydrocarbon) from the lift-off gate formation process. Etching and cleaning processes prior to nickel deposition might not be optimum and it could leave hydrocarbon residue on the AlGaN surface. Upon annealing at 225ºC for 500 h, carbon atoms from decomposed hydrocarbons could diffuse into the nickel layer and cause an increase of leakage current. This is supported by the diffusion distance (δ) calculated for carbon in nickel via lattice diffusion:

$$\delta = \sqrt{Dt} \tag{3}$$
$$D = D_0 \exp\left(-\frac{E_a}{kT}\right),$$

where E_a is the activation, 0.87 eV [22] and D_o is the pre-exponential factor, D_o = 2.89 ×10^{-5} cm^2/s [22]. Here, using these parameters, we obtained δ = 3.04 μm. This is even larger than the gate length of the devices.

This photoresist residue is likely to be non-uniformly distributed across the wafer, which would explain why some devices are good while others are bad. It is however noteworthy to mention that the yield of this fabrication process used in this work is 80%. This is considered quite high for an experimental-grade device fabricated using a lift-off process.

4. Conclusions

In conclusion, we have shown that carbon impurities can cause a very high initial leakage current for AlGaN/GaN-on-Si high electron mobility transistors. Its presence in the gate metal can reduce the zero-bias Schottky barrier height. This finding highlights the detrimental effect of carbon to the device fabrication yield. The methodology demonstrated in this work can also be applied to study the increase of gate-leakage current due to device stressing.

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