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Design and investigation of negative capacitance–based core-shell dopingless nanotube tunnel field-effect transistor

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Abstract

Investigation and analysis of a ferroelectric material–based dopingless nanotube tunnel field-effect transistor are conducted using a lead zirconate titanate (PZT) gate stack to induce negative capacitance in the device. Landau–Khalatnikov equations are used in deriving the parameter values of the ferroelectric material to ensure accurate results. The nanotube structure of the tunnel field-effect transistor allows for better electrostatic control owing to its gate-all-around structure. Incorporation of negative capacitance further reduces the voltage supply requirement and power consumption of the structure while simultaneously improving switching. In addition, the device is studied for varying thicknesses of the dielectric PZT material. The threshold voltage of the device under study was calculated as 0.281 V, and the average subthreshold slope of the device was reduced to 18.271 mV/decade, far below the thermionic limit of 60 mV/decade.

1 | INTRODUCTION

The scaling down of metal oxide semiconductor field-effect transistors (MOSFETs) over the years has led to highly dense chips and hence, the introduction of short channel effects [1]. Furthermore, it is essential to overcome the Boltzmann's Tyranny, which limits the subthreshold swing observed in a MOSFET to 60 mV/decade. Introduction of tunnel field-effect transistors (TFETs) has helped in achieving a subthreshold swing below the thermionic limit, with another advantage being a reduction in short channel effects. However, TFETs are no exception to Moore's law. Thus, the increased density of the chip components still poses a challenge. This trend has also led to the problem of increasing power dissipation in the chip. Because the dissipated power is directly proportional to the switching event, one possible solution to the issue could be to reduce the switching activity in the circuit. An alternative is to lower the operating voltage of the device. However, the power consumption, on-state current of the device and short channel effects have a trade-off relationship with each other that poses challenges of its own when trying to design an optimized MOSFET [2]. Thus, if the operating gate voltage of the device is reduced, the on-state current will decrease as well, and this phenomenon is undesirable. Several device structures such as the impact ionization MOSFET [3], and techniques such as the introduction of a narrow band-gap material such as SiGe [4] or InAs [5] can result in a lowering of the subthreshold swing as well as in reduction of the short-channel effects observed in devices. Another method to achieve enhanced switching is the introduction of negative capacitance through a ferroelectric material in the structure, which is discussed herein.

wThe introduction of a ferroelectric insulator to the device through gate stacking can induce a negative capacitance in the structure [6]. However, in the non-equilibrium condition, a ferroelectric material is unable to show negative capacitance because of the energy barrier formed during transition of phase. A ferroelectric material can be stabilized, however, in the state of negative differential capacitance through the introduction of a dielectric capacitor connected in series with the ferroelectric [7]. This results in amplification of the voltage because the ferroelectric starts to act as a transformer and thus can lower the voltage requirements. In addition, it should be noted that capacitance has a proportional relationship with charge, and the charge across the gate capacitance(C_{gg}) remains the same as the ferroelectric capacitance (C_{FE}) because they are connected in series. Thus, to introduce the same charge in the channel, it is important to reduce the voltage of the device. This negative capacitance can further enhance the total

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capacitance of the device, which will result in a significant improvement in the on-state current.

In this work, integration of a dopingless nanotube tunnel field-effect transistor(DL-NT-TFET) and a ferroelectric material has been achieved through numerical models and TCAD simulations to design a ferroelectric DL-NT-TFET(Fe-DL-NT-TFET). The operation of the device remains the same, while the ferroelectric acting as a step-up transformer has been included in the gate region by making a serial connection between the two. This enables the reduction of voltage mismatch in the designed structure [8].

The ferroelectric material has been modelled using the 1-D Landau model without imposing a boundary condition through a metallic intermediate layer. Now, because the metal-ferroelectric-metal-insulator-semiconductor structure cannot be designed through simulators, the Landau–Khalatnikov theory of ferroelectrics (L–K theory) [9] has been used to incorporate the effect of the ferroelectric material with a simulated structure of the DL-NT-TFET.

The Gibbs free energy density, U, for the ferroelectric material can be given in terms of polarization, P, by the L-K equation as (1):

$$\begin{aligned} U &= \alpha t_{FE}P^2 + \beta t_{FE}P^4 + \gamma t_{FE}P^6 - V_{FE}P \\ U &= \alpha t_{FE}Q^2 + \beta t_{FE}Q^4 + \gamma t_{FE}Q^6 - V_{FE}Q \end{aligned} \quad (1)$$

Here, α, β and γ are the material-dependent anisotropy constants, ferroelectric material thickness (t_{FE}) represents the thickness of the ferroelectric material, V_{FE} is the voltage applied across the ferroelectric region, and Q is the charge across the ferroelectric material. For the equilibrium state, the equation used is given by (2). The relationship between charge and V_{FE} is dictated by (3):

$$\frac{\partial U}{\partial Q} = 2\alpha t_{FE}Q + 4\beta t_{FE}Q^3 + 6\gamma t_{FE}Q^5 - V_{FE} \quad (2)$$

$$V_{FE} = 2\alpha t_{FE}Q + 4\beta t_{FE}Q^3 + 6\gamma t_{FE}Q^5 \quad (3)$$

$$V_{GNC} - V_{gate(eff)} = 2\alpha t_{FE}Q + 4\beta t_{FE}Q^3 + 6\gamma t_{FE}Q^5 \quad (4)$$

The voltage drop across the ferroelectric region is given by (4), where V_{GNC} represents the applied gate voltage, while $V_{gate(eff)}$ represents the intermediate contact potential formed when the ferroelectric dielectric is connected with the dielectric of the device in series. The ferroelectric material used in this work to induce negative capacitance in this material is lead zirconate titanate (PZT), whose molecular composition is given as $Pb[Zr_{43}Ti_{57}]O_3$. It is resilient, with varying thickness, and has nanosecond polarization reversal. Apart from this, PZT offers high reliability, and its properties change as the thickness of the material varies [10].

In this work, the ferroelectric material is assumed to be thick because firstly, negligible variation was observed in the ferroelectric properties when the ferroelectric region had a low thickness [11], and secondly, the device structure is dopingless. Based on the doping concentration and temperature, the properties of PZT may vary. The Landau coefficients have been calculated based on [12], where $\alpha = -1.8 \times 10^{11}$, $\beta = 5.8 \times 10^{22}$ and $\gamma = 0$. Because the relationship between Q and V_{FE} is also dependent upon t_{FE}, a change in its value can accommodate the variation in the Landau parameters. The optimum value of the thickness of the ferroelectric material after an extensive analysis suitable for the device was found to be 3.79 μm.

The "Device Structures" section of this paper discusses the structure of the device and its parametric values. The "Results and Discussion" section deals with an analysis of all the results that have been simulated and their discussions, while the "Conclusion" provides a brief insight into the observations made in the paper.

2 | DEVICE STRUCTURES

The Fe-DL-NT-TFET consists of a simulated DL-NT-TFET structure and a ferroelectric layer that has been connected in series with the DL-NT-TFET structure. This is done to induce a negative capacitance in the circuit that will lower the power supply requirements of the circuit and will lead to higher gain as well as voltage amplification. The structure of the Fe-DL-NT-TFET is shown in Figure 1, in which the series connection between the capacitors represents how the structure incorporates the effect of a ferroelectric material introduced externally. The three-dimensional structure of DL-NT-TFET is shown in Figure 1(a), and one-half of the 3-D structure in 2-D configuration resembling the cross-section marked by a cutline in the 3-D structure of the device is represented in Figure 1(b). The 3-D structure of the Fe-DL-NT-TFET with an externally connected ferroelectric layer is shown in Figure 1(c), and one-half of the 3-D structure in 2-D configuration is shown in Figure 1(d).

The dopingless structure of the device allows it to be fabricated with more efficiency because the non-uniform doping constraints have been eliminated. Furthermore, the shell gate and gate-all-around (GAA) structure of the Fe-DL-NT-TFET gives the device better control over the applied gate voltage [13]. The nanotube structure gives the device good electrostatic control that is suitable for very low-power applications [14]. The on-state current of the device with a nanotube structure is improved owing to the larger cross-sectional area of the junction. Lateral tunnelling in the nanotube device leads to better performance because of the dependency of band-to-band tunnelling, the mechanism through which the current flows in TFETs, on the junction cross-sectional area [15]. The core consists of silicon dioxide (SiO_2) with a platinum electrode whose work function is equal to 5.93 eV and a hafnium electrode whose work function is 3.9 eV to form the source and drain, respectively, because the device is dopingless [16]. Application of the charge plasma technique allows the elimination of the doping techniques implemented at high temperatures [17]. The core is further covered with a layer of intrinsic silicon with a concentration of 10^{15} atoms/cm^3 over which another layer of SiO_2, gate oxide is wrapped. This leads to the formation of a GAA structure because the shell gate is formed all around the

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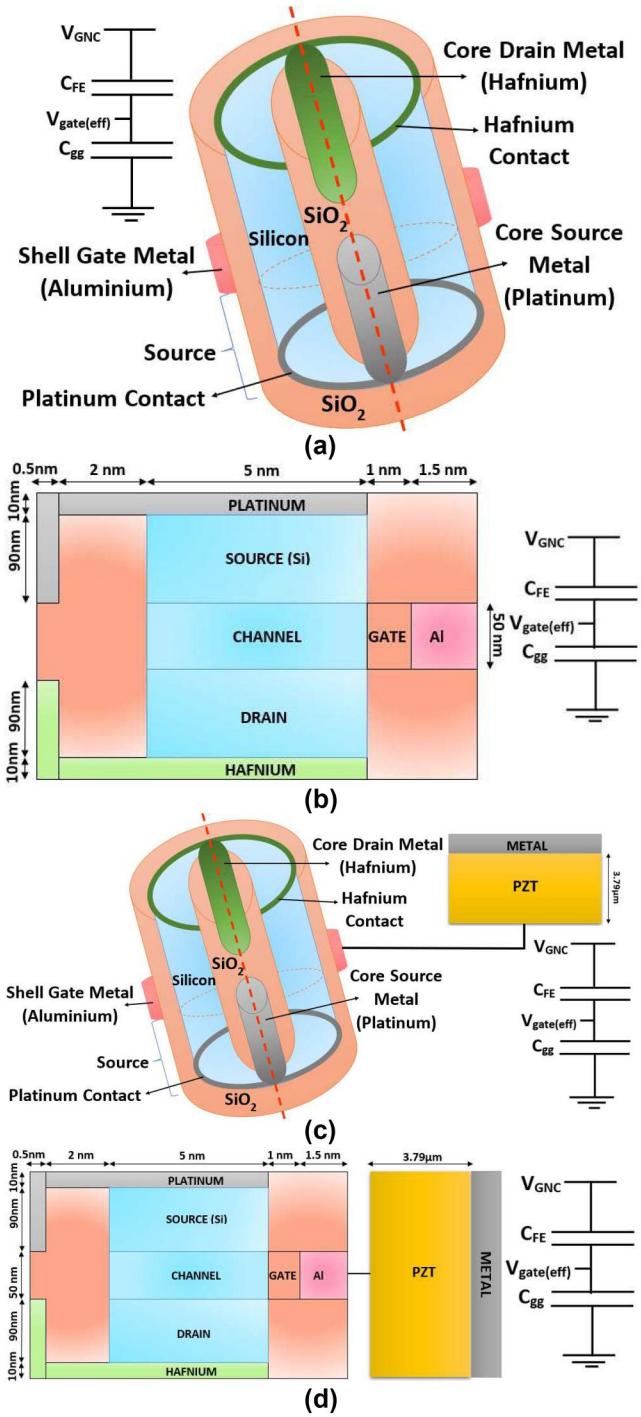

FIGURE 1 Structure of (a) 3-D configuration of dopingless nanotube tunnel field-effect transistor (DL-NT-TFET) (b) One-half of 3-D structure of DL-NT-TFET in 2-D configuration (c) 3-D configuration of ferroelectric DL-NT-TFET (Fe-DL-NT-TFET) (d) One-half of 3-D structure of Fe-DL-NT-TFET in 2-D configuration [18]. C_{FE}, ferroelectric capacitance; *Cgg*, gate capacitance; *PZT*, lead zirconate titanate; *Vgate(eff)*, intermediate contact potential; *VGNC*, applied gate voltage

nanotube structure. Over this dielectric, a layer of aluminium, whose work function has been taken to be 4.35 eV, has been embedded to provide the contact for the gate. The source and drain regions have a length of 90 nm each, and the channel length is 50 nm. The thickness of the intrinsic body is taken to be 5 nm, whereas the thickness of the gate oxide is 1 nm. Taking the three-dimensional structure into account, the radius of the nanotube is 5 nm. The thickness of the ferroelectric layer consisting of PZT has been taken as 3.79 μm. The values of the Landau parameters for the calculation of the effect of the ferroelectric material on the device have been taken as per the thickness of the ferroelectric region while taking the dopingless structure of the Fe-DL-NT-TFET into account. Table 1 summarizes the values of all the parameters for the structure.

The Silvaco Atlas TCAD tool has been used for the design and simulation of the device, whereas the numerical analysis has been conducted by incorporating the observations made in MATLAB. The latter has been used to perform all the calculations based on the L–K equations to enable the results of further simulations and analysis to be as accurate and realistic as possible. During the simulations, the Lombardi model has been used because of the non-planar structure of the device. The Shockley–Read–Hall model enables the use of fixed minority lifetimes, while using the Auger model enabled the direct transition of the carriers, which becomes significant when the current density becomes too high. The non-local band-to-band tunnelling model allows model tunnelling with more accuracy.

A vertical structure is preferred, as it is difficult to fabricate GAA over lateral nanotube even with the use of a sacrificial layer (yellow electrode is used as core-source instead of gate; a shell-source electrode is omitted for the proposed devices) [19–21].

3 | RESULTS AND DISCUSSION

A negative slope occurring in the polarization-ferroelectric voltage plot signifies the implementation of negative capacitance in the circuit. This phenomenon has been observed in the analysis of the designed structure of Fe-DL-NT-TFET.

TABLE 1 Parameters for FE-DL-NT-TFET

Device parameter	Value
Source material	Silicon
Source length	90 nm
Gate length	50 nm
Drain length	90 nm
Intrinsic body thickness	5 nm
Gate oxide thickness	1 nm
Radius	5 nm
Source/Channel/Drain doping	10^{15} atoms cm^{-3}
Source metal work function	5.93 eV
Gate metal work function	4.35 eV
Drain metal work function	3.9 eV
Ferroelectric material thickness	3.79 μm

Abbreviation: FE-DL-NT-TFET, ferroelectric dopingless nanotube tunnel field effect transistor.

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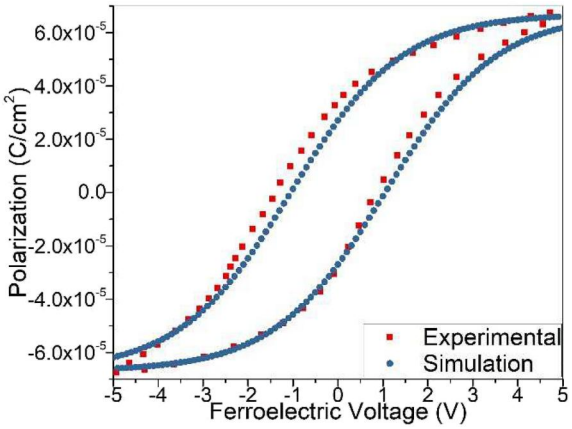

FIGURE 2 Simulated transients and characterization of 3.79 μm thick lead zirconate titanate material calculated by Landau–Khalatnikov equation using Landau parameters ($\alpha = -1.8 \times 10^{11}$, $\beta = 5.8 \times 10^{22}$ and $\gamma = 0$)

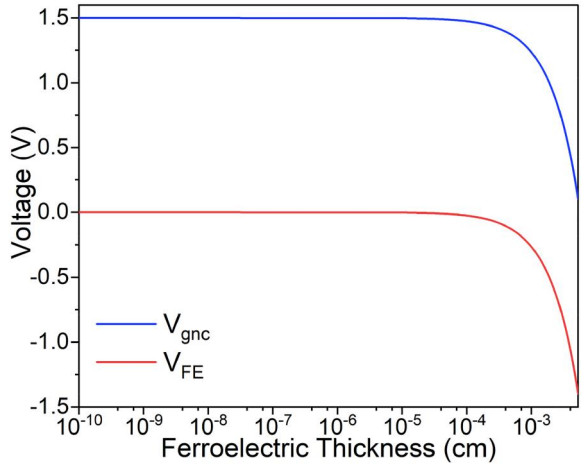

FIGURE 3 Applied gate voltage (V_{GNC}) and voltage across ferroelectric material (V_{FE}) plots versus varying ferroelectric material thickness (from 10^{-10} to 10^{-3} cm) for ferroelectric dopingless nanotube tunnel field-effect transistor

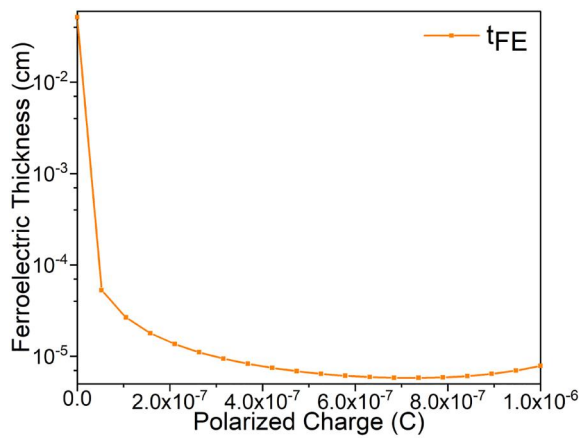

FIGURE 4 Ferroelectric material thickness (t_{FE}) versus polarized charge plot with variation in charge (from 0 to 1.0×10^{-6} C) for ferroelectric dopingless nanotube tunnel field-effect transistor

The physical and electrical characterization based on the Landau theory of the 3.79 μm thick PZT layer can be observed in Figure 2. The figure compares the experimental [11] and simulated results, which show a hysteretic behaviour. The simulated result represents the hysteresis loop obtained when 3.79 μm thick PZT has been used.

If the applied voltage is smaller than the coercive voltage of the material, the capacitance is observed to be positive, and thus it acts as a simple capacitor. But as soon as the applied voltage surpasses the coercive voltage, the material begins to show a negative capacitance transient [7]. This indicates that the analytical model of the PZT designed through MATLAB was successful, and it was also used for the study of other characteristics of the device. As is well established, the PZT material varies in its properties with variations in the thickness of the ferroelectric material. In doped devices, the polarization charge is greater than in dopingless devices. Because the polarization charge is low in the simulated dopingless structure, t_{FE} must be kept high. From Figure 3, it can be observed that when t_{FE} varies from 10^{-10} to 10^{-5} cm, no significant change in the applied gate voltage and V_{FE} were observed. Thus, to obtain realistic results from the simulations, the thickness of the ferroelectric material has been varied from 10^{-5} to 0.0053 cm during further device analysis. After t_{FE} enters this range and the negative capacitance effect comes into play, even a minor change in t_{FE} results in significant variation in the threshold voltage as shown in Figure 3. This occurs because during this range of t_{FE}, V_{GNC} and V_{FE} show maximum variation, thus indicating that the range allows for efficient and accurate analysis of the effect of introducing negative capacitance to the simulated structure.

The polarized charge is directly proportional to the interface charges present in the device that are present towards the edges of the dielectric material. The polarization charge is the parameter responsible for generation of the hysteresis loop as observed in the case of ferroelectric materials. In Figure 4, it is seen that with an increase in the value of the polarization and interface charges, the thickness of the ferroelectric material decreases, thus indicating that for doped devices, a thinner film of ferroelectric material is required to incorporate the effect of negative capacitance. Whereas dopingless devices have lower interface charges than their doped counterparts, a thicker ferroelectric will be required for the design of a negative capacitance-based device. The referred work [22] shows that with the increment of t_{FE}, the remnant polarization, saturated polarization and coercive electric field vary, but the variation is minimal and does not change the device behaviour for a lower t_{FE} thickness.

When the C_{FE} and C_{gg} present in the device are connected in series to obtain a stable negative capacitance structure, the total capacitance of the device (C_T) can be given by

$$C_T = \frac{C_{FE} C_{gg}}{C_{FE} + C_{gg}} \tag{5}$$

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The total gate capacitance, C_{gg}, is obtained through TCAD simulations of the Fe-DL-NT-TFET structure when a gate bias of 1.5 V and a drain bias of 1.2 V were applied to the device. Whereas the value of the capacitance of the ferroelectric material, C_{FE}, is dictated by the L-K theory and has been calculated through MATLAB. Because the C_{FE} is observed to have a negative value, a series combination of both the capacitances, C_{FE} and C_{gg}, results in a higher value than either of the constituent capacitances. This phenomenon can be seen in Figure 5, which represents a plot between C_T, C_{gg} and C_{FE} against the applied gate voltage of the device. C_{gg} is a combination of the gate-to-source capacitance and gate-to-drain capacitance. As the C_T curve progresses towards higher values of the voltage, it obtains a significantly higher value than the other two capacitances connected in series with each other. This is another desired requirement for a device based on a ferroelectric material that aims to reduce the power requirement. Now, because the total device capacitance increases, the required gate voltage to drive the structure will be reduced. It is observed from Figure 5 that as the applied gate voltage increases, C_T also increases. Now, because the drain current (I_D) is directly proportional to the capacitance of the device, it should show an increment in its value as well. This can be observed in Figure 6, which shows a plot between the I_D and applied gate voltage of the device. The curve for I_D without including the effect of ferroelectric material shows a lower value of I_D at 0.5 V as compared to the I_D corresponding to Fe-DL-NT-TFET because the total capacitance of the designed device has a higher value than the total gate capacitance (C_{gg}) of simple DL-NT-TFET. Another noteworthy phenomenon is the steeper slope of the I_D plot for Fe-DL-NT-TFET. This indicates an improvement in the subthreshold swing as well.

In Figure 7, a plot of varying I_Ds in accordance with varying thickness of the ferroelectric material ($t_{FE} = 10^{-5}$ cm to 0.0053 cm) can be observed. It can be inferred from the plot that although switching improves as the thickness of the ferroelectric layer increases, the on-state current of the device remains the same. The improvement in the on-state current is not sacrificed while using a thicker ferroelectric material, while the required gate voltage for the device to function is significantly reduced. It is known that the transconductance of the device is proportional to the drain current of the device and is given by $g_m = dI_D/dV_{GS}$.

From Figure 5, it is observed that with an increasing applied gate voltage, the drain current of the device is also enhanced. In addition, for the simple DL-NT-TFET, the value of I_D is more than the value of I_D for Fe-DL-NT-TFET. Thus, the transconductance of the device should also show an increment in value as the applied gate voltage progresses. Figure 8 shows a transconductance-applied gate voltage plot for the simple and ferroelectric based DL-NT-TFETs. As expected, the value of g_m seems to be increasing as the curves progress, and it is higher for Fe-DL-NT-TFET than for its simple counterpart.

The variation in the value of transconductance with a varying thickness of the ferroelectric material is shown in

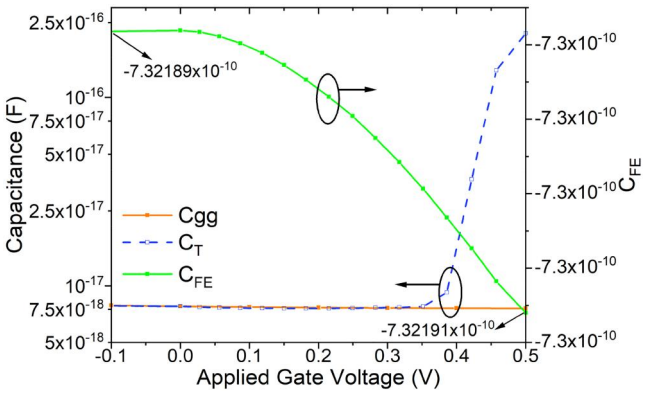

FIGURE 5 Capacitance (total gate capacitance, C_{gg}; total device capacitance, C_T and ferroelectric material capacitance, C_{FE}) versus applied gate voltage (from −0.1 to 0.5 V) plot for ferroelectric dopingless nanotube tunnel field-effect transistor

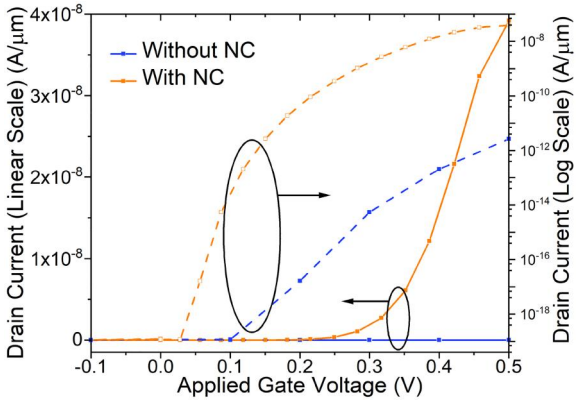

FIGURE 6 Drain current versus applied gate voltage plot for ferroelectric dopingless nanotube tunnel field-effect transistor while applied gate voltage varies from −0.1 to 0.5 V. *NC*, negative capacitance

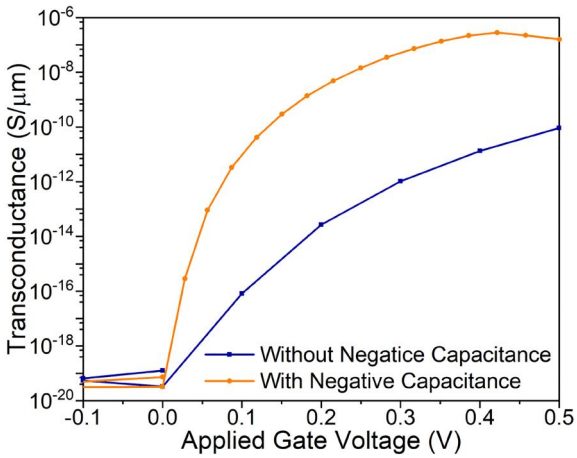

FIGURE 7 Transconductance (g_m) versus applied gate voltage plot for ferroelectric dopingless nanotube tunnel field-effect transistor for varying applied gate voltage (from −0.1 to 0.5 V)

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Figure 9 on both linear and log scales. It can be observed from the figure that as the thickness of PZT increases, the value of g_m also increases. Thus, by using a thicker ferroelectric layer, the power supply can be scaled down further.

The surface potential at the interface of the ferroelectric layer and the gate in the simulated device is represented in Figure 10 with a variation in the thickness of the ferroelectric material. It can be observed that with an increase in the applied gate voltage of the Fe-DL-NT-TFET, the potential also increases. In addition, as t_{FE} increases, the curve for potential becomes steeper, while the maximum value of the potential remains the same. Because the value of charge present at the interface is directly proportional to the value of potential, and furthermore, because current and charge have a proportional relation, the drain current for the device will show a similar phenomenon, as shown in Figure 6. The recombination and generation rate define the processes through which the charge carriers, holes or electrons, are created and destroyed. The recombination rate describes the rate at which the electrons present in the conduction band lose energy and combine with the holes present in the valence band of a semiconductor material (Figure 11). With an increase in the gate voltage, the rate of recombination of charge carriers seems to go down, which shows that the amount of charge present at the interface of the ferroelectric dielectric and the gate decreases with an increment in the applied gate voltage. However, the maximum recombination rate for all values of t_{FE} remains the same.

Figure 12 represents the variation in electric field with applied gate voltage. It can be observed from the plots that the values of electric field show an increase until a certain value and then start decreasing. It is known that by reducing the electric field, the effective capacitance of a device can be increased. This phenomenon occurs due to the presence of dielectrics, and in doing so, the same charge is obtained at a lower voltage. This trend of an overall increase in the effective capacitance of the device can be observed in Figure 5. With an increase in the applied gate voltage in the Fe-DL-NT-TFET, the electron concentration, as shown by Figure 13, indicates an enhancement. For increasing thickness

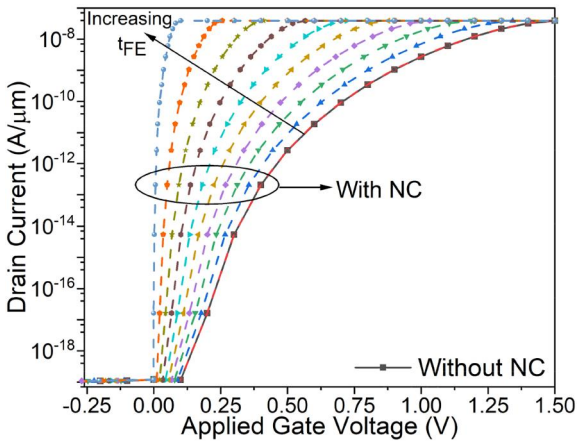

FIGURE 8 Drain current versus applied gate voltage plot for variation in thickness of ferroelectric material ($t_{FE} = 10^{-5}$ to 0.0053 cm) in ferroelectric dopingless nanotube tunnel field-effect transistor. *NC*, negative capacitance; t_{FE}, ferroelectric material thickness

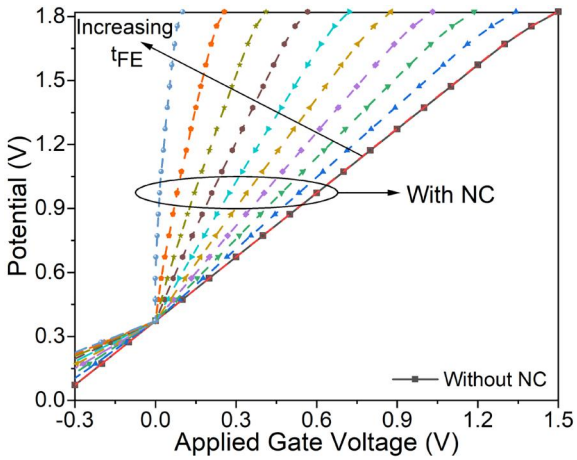

FIGURE 10 Surface potential versus applied gate voltage plot with varying ferroelectric thickness (from $t_{FE} = 10^{-5}$ to 0.0053 cm) for ferroelectric dopingless nanotube tunnel field-effect transistor. *NC*, negative capacitance; t_{FE}, ferroelectric material thickness

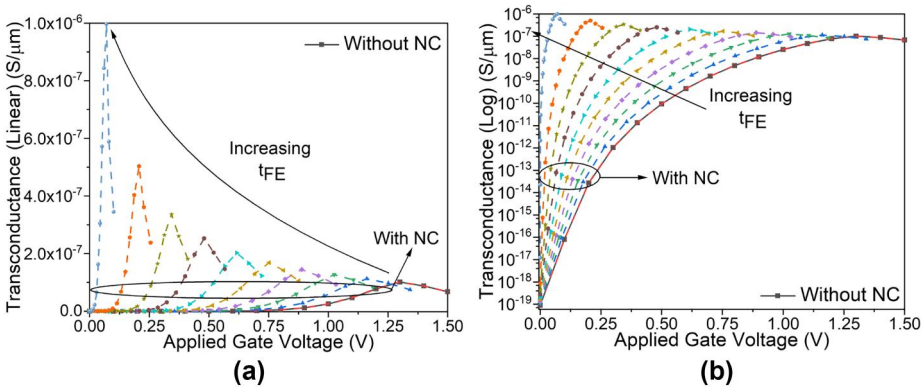

FIGURE 9 Variation in transconductance with applied gate voltage of ferroelectric dopingless nanotube tunnel field-effect transistor with variation in t_{FE} (from 10^{-5} to 0.0053 cm) in (a) linear scale (b) log scale. *NC*, negative capacitance; t_{FE}, ferroelectric material thickness

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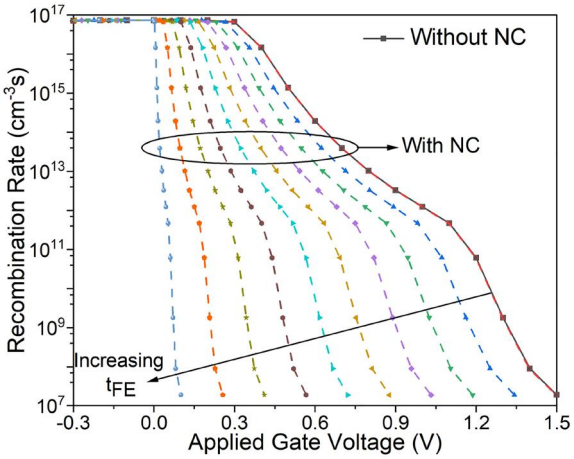

FIGURE 11 Recombination rate versus applied gate voltage plot for ferroelectric dopingless nanotube tunnel field-effect transistor where t_{FE} varies from 10^{-5} to 0.0053 cm. *NC*, negative capacitance; t_{FE}, ferroelectric material thickness

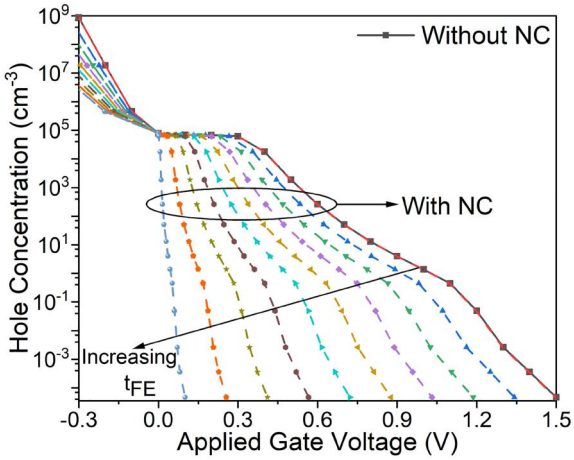

FIGURE 13 Hole concentration versus applied gate voltage plot with varying t_{FE} (10^{-5} cm to 0.0053 cm) for ferroelectric dopingless nanotube tunnel field-effect transistor. *NC*, negative capacitance; t_{FE}, ferroelectric material thickness

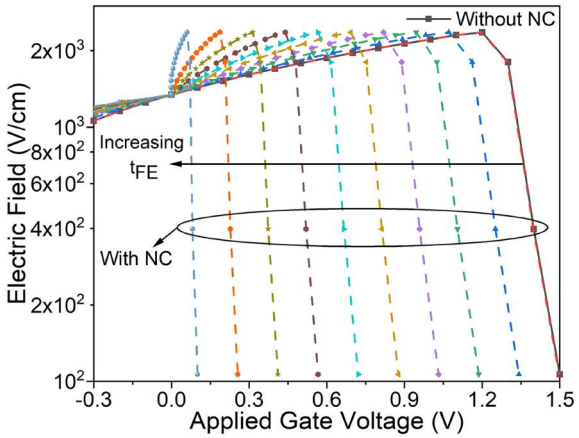

FIGURE 12 Electric field variation versus applied gate voltage for ferroelectric dopingless nanotube tunnel field-effect transistor for different values of ferroelectric layer thickness (from $t_{FE} = 10^{-5}$ to 0.0053 cm). *NC*, negative capacitance; t_{FE}, ferroelectric material thickness

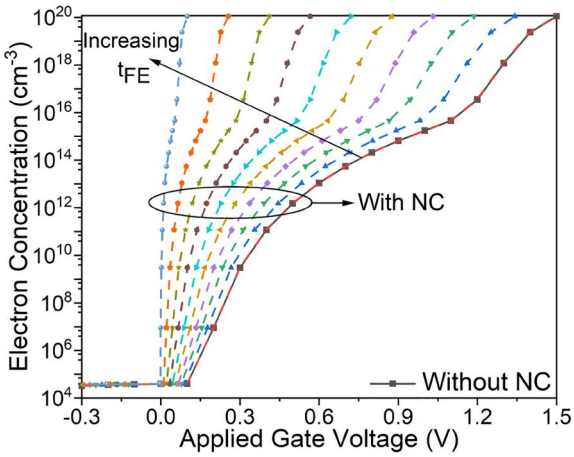

FIGURE 14 Electron concentration versus applied gate voltage plot with varying t_{FE} (10^{-5} to 0.0053 cm) for ferroelectric dopingless nanotube tunnel field-effect transistor. *NC*, negative capacitance; t_{FE}, ferroelectric material thickness

of the ferroelectric layer, the electron concentration increases more abruptly, which indicates that the switching of the device is better. Quite the opposite happens with the hole concentration. As can be observed from Figure 14, the concentration of the positive charge carriers decreases with an increase in the applied gate voltage. This happens because the electrons in the conduction band eventually start losing their energy and recombining with holes. With an increase in the ferroelectric dielectric thickness, the hole concentration will start to decrease more abruptly.

The average subthreshold slope of a device is given by $S_{avg} = (V_T - V_{off})/\log(I_T - i_{off})$. It can be observed from Figure 15 that as the thickness of the dielectric material increases, the average subthreshold swing decreases. In addition, the values of the threshold voltage and the subthreshold swing represented in Figure 16 decrease with an increase in t_{FE}.

A decrement in the value of the average subthreshold swing and subthreshold slope indicate better switching capability of Fe-DL-NT-TFET. In addition, as can be observed from the graph, the device thus designed has a capability of overcoming the thermionic limit of 60 mV/decade. A decreasing value of the threshold voltage with an increasing t_{FE} indicates that the device can work at lower gate voltages and thus can be efficient in reducing the power supply requirement.

It can be seen in Figure 17 that the value of maximum transconductance of the Fe-DL-NT-TFET increases as t_{FE} increases. This happens because the transconductance of a device is directly dependent upon its drain current. In Figure 9, the value of the peaks in transconductance corresponding to the increasing ferroelectric thickness continue to decrease, and thus, the maximum transconductance of the device should also increase.

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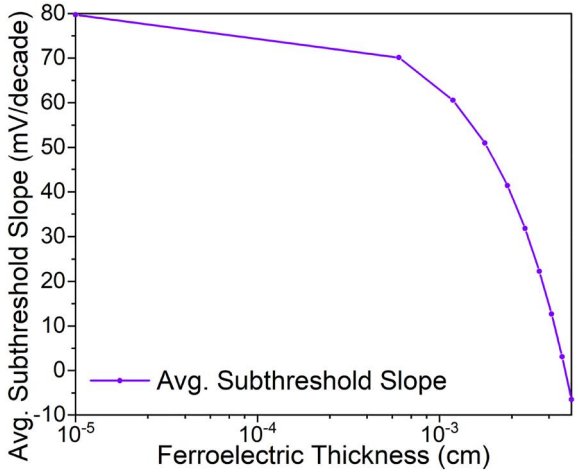

FIGURE 15 Average subthreshold slope versus applied gate voltage plot for ferroelectric dopingless nanotube tunnel field-effect transistor with variable ferroelectric thickness (from 10^{-5} to 0.0053 cm)

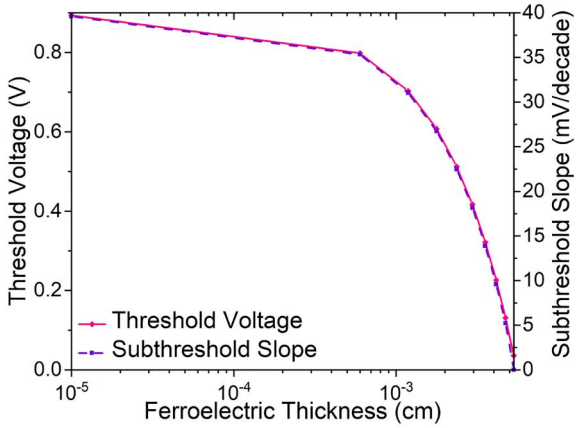

FIGURE 16 Threshold voltage and subthreshold slope versus applied gate voltage plot for ferroelectric dopingless nanotube tunnel field-effect transistor with varying ferroelectric material thickness (from 10^{-5} to 0.0053 cm)

4 | CONCLUSION

In this work, the analysis of a Fe-DL-NT-TFET has been conducted based on the simulations and through numerical models designed to incorporate the effect of introducing a ferroelectric dielectric in a DL-NT-TFET structure. The Landau–Khalatnikov equations were used to design a numerical model externally and through it, a negative capacitance was induced on the simulated model of the DL-NT-TFET. The subthreshold slope (SS) of DL-NT-TFET before introduction of the ferroelectric layer was calculated as 39.68 mV/dec, whereas the SS for ferroelectric-based DL-NT-TFET was observed to be 12.04 mV/dec. The average SS for Fe-DL-NT-TFET was reduced to 18.27 mV/dec. The threshold voltage for DL-NT-TFET was initially observed as 0.89 V. Upon applying the negative capacitance technique, the threshold voltage was lowered to 0.28 V, thus improving the switching as well as lowering the power supply needed for operation of the device, which is a sought-after property in low-power applications.

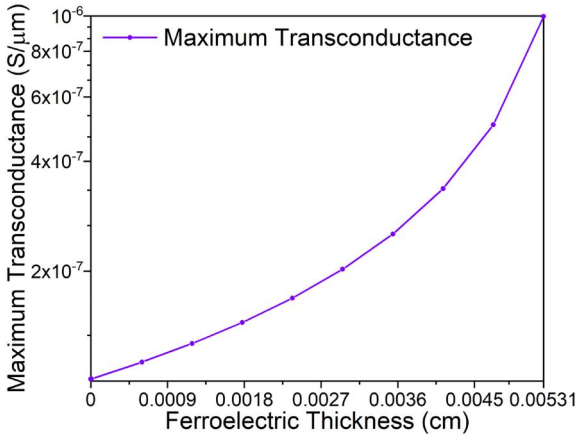

FIGURE 17 Maximum transconductance versus ferroelectric material thickness (t_{FE}) plot for ferroelectric dopingless nanotube tunnel field-effect transistor with t_{FE} varying from 10^{-5} to 0.0053 cm

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