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# Capacitor-free low dropout regulators using nested Miller compensation with active resistor and 1-bit programmable capacitor array

*W.-J. Huang S.-I. Liu*

*Graduate Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan 10617, Republic of China*
*E-mail: lsi@cc.ee.ntu.edu.tw*

**Abstract:** A capacitor-free CMOS low dropout regulator (LDR) using the nested Miller compensation with an active resistor (NMCAR) is presented. It can efficiently control the damping factor and reduce the required Miller compensation capacitance. It can also resolve the trade-off between dc loop gain and damping factor, which existed in the LDR using the nested Miller compensation. To reduce the total Miller compensation capacitances further, a capacitor-free CMOS LDR using both the NMCAR and a 1-bit programmable capacitor array is presented. For this LDR, the total on-chip compensation capacitance is reduced 40% without influencing its stability. Furthermore, it also enhances the recovery time, compared with the LDR using the NMCAR technique. Two proposed LDRs with bandgap voltage references have been fabricated in a 0.35 μm CMOS process. They can operate with and without output capacitors.

## 1 Introduction

Low dropout regulator (LDR) provides an accurate, stable and low-noise output voltage. To reduce the output dropout voltage, the efficiency of an LDR is increased, and the operation time of the battery-powered devices is prolonged. These advantages make LDRs [1–6] widely used in portable systems, especially in RF circuitry. A conventional LDR [1] is composed of an error amplifier, a power PMOS transistor, a feedback resistor network and a bandgap voltage reference. The output capacitor is often needed to reduce the output voltage ripple. However, the equivalent series resistance (ESR) of the output capacitor degrades the stability. In addition, the parasitic capacitance of the power PMOS transistor slows down the recovery time of the regulator if the output current is suddenly changed.

To consider the stability, the conventional LDR locates the dominant pole at very low frequency at the output to achieve the frequency compensation. It requires a large output capacitor and it is difficult to integrate on a single chip. To have a fast transient response, a buffer [3, 4] is inserted between the error amplifier and the power PMOS transistor. To achieve the large dc loop gain in the low supply voltage, a gain stage replaces this buffer in the regulator. It converts the LDR to be a multi-stage amplifier. To stabilise a multi-stage LDR, the complicated frequency compensation is needed [4, 5]. The nested Miller compensation (NMC) technique and its variants are widely presented in the literature [7]. The LDR [4] using the NMC technique [7] has to trade off the dc-loop gain and damping factor. To improve this trade-off, a stable LDR without the output capacitor adopts the damping-factor-control technique [5].

To effectively control the damping factor and reduce the required Miller capacitance, the novel NMC with active resistor (NMCAR) technique is presented to realise a capacitor-free LDR. To reduce the required frequency compensation capacitances and the recovery time further, a capacitor-free LDR using a 1-bit programmable capacitor array (PCA) is presented. By using the proposed 1-bit PCA, this LDR reduces 40% of the total on-chip frequency

compensation capacitor without influencing its stability, compared with that using the NMCAR technique. In addition, it speeds up the recovery time.

## 2 LDR using the NMC technique

The LDR using the NMC technique [7] with and without the output capacitor is analysed, respectively, as follows:

### 2.1 With output capacitor

The LDR using the NMC technique and its small-signal model is shown in Figs. 1*a* and 1*b*, respectively. In Fig. 1*a*, this LDR is composed of two gain stages, a power PMOS transistor, the output capacitor ($C_{OUT}$) and its associated ESR resistance ($R_{ESR}$). The feedback resistor network consists of the resistors, $R_{F1}$ and $R_{F2}$. $g_{m1}$, $g_{m2}$ and $g_{mp}$ are the transconductance of the first gain stage, the second gain stage and the power PMOS transistor, respectively. $R_{O1}$, $R_{O2}$, $C_{P1}$ and $C_{P2}$ are the output resistances and capacitances at the outputs of two gain stages, respectively. $C_{m1}$ and $C_{m2}$ are Miller compensation capacitances. $R_{OUT}$ $(=R_L \| R_{Op} \| (R_{F1}+R_{F2}))$ is the equivalent output resistance where $R_L$ is the load resistance and $R_{Op}$ is the output resistance of the power PMOS transistor. To simplify the derivations, the following assumptions are reasonably made

$$g_{m1}R_{O1}, g_{m2}R_{O2}, g_{mp}R_{OUT} \gg 1 \tag{1}$$

$$g_{mp} \gg g_{m1}, g_{m2} \tag{2}$$

$$C_{m1} \gg C_{P1}, C_{m2} \gg C_{P2} \tag{3}$$

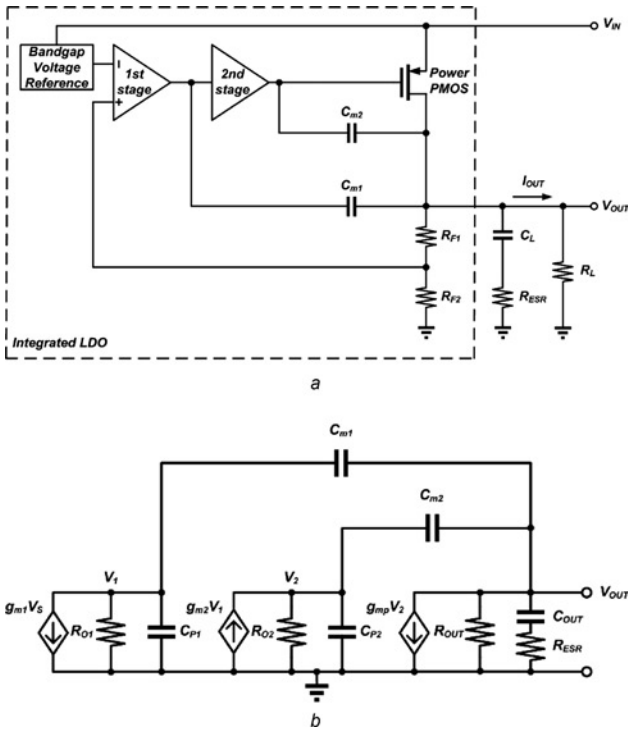


**Figure 1** *LDR using the NMC technique*

*a* NMC LDR

*b* Its equivalent small-signal model

and

$$C_{OUT} \gg C_{m1}, C_{m2} \tag{4}$$

Thus, the small-signal loop gain is expressed as

$$L(s) = \frac{A_0(1 - s(C_{m2}/g_{mp}) - s^2(C_{m1}C_{m2}/g_{m2}g_{mp}))(1 + sC_{OUT}R_{ESR})}{(1 + (s/p_{-3dB}))[1 + s(C_{OUT}R_{ESR} + (C_{m2}/g_{m2})) + s^2(C_{m2}C_{OUT}/g_{m2}g_{mp})]} \tag{5}$$

where the dc loop gain is given by

$$A_0 = g_{m1}g_{m2}g_{mp}R_{O1}R_{O2}R_{OUT}\left(\frac{R_{F2}}{R_{F1}+R_{F2}}\right) \tag{6}$$

and the dominant pole is at

$$p_{-3dB} = \frac{1}{C_{m1}g_{m2}g_{mp}R_{O1}R_{O2}R_{OUT}} \tag{7}$$

The second-order polynomial in the denominator as in (5) is rewritten as

$$F(s) = 1 + s\left(\frac{2\zeta}{p_c}\right) + s^2\left(\frac{1}{p_c^2}\right) \tag{8}$$

where

$$p_c = \sqrt{\frac{g_{m2}g_{mp}}{C_{m2}C_{OUT}}} \tag{9}$$

And the damping factor

$$\zeta = \frac{1}{2}\left(C_{OUT}R_{ESR} + \frac{C_{m2}}{g_{m2}}\right)\sqrt{\frac{g_{m2}g_{mp}}{C_{m2}C_{OUT}}} \tag{10}$$

To ensure the loop stability, the LDR adopts the single-pole system within the unity-gain frequency of the LDR. Thus, the gain bandwidth (GBW) is placed to be less than 1/2 of complex pole ($P_C$) (i.e. 2 GBW $\leq P_C$). That is

$$2\frac{g_{m1}}{C_{m1}}\left(\frac{R_{F2}}{R_{F1}+R_{F2}}\right) \leq \sqrt{\frac{g_{m2}g_{mp}}{C_{m2}C_{OUT}}} \tag{11}$$

According to (7), Miller theorem locates the dominant pole at the output of the first gain stage instead of the output of the power PMOS transistor and the dominant pole depends on $C_{m1}$. Hence, a large $C_{m1}$ is required to realise a low dominant pole. Moreover, it is possible to decrease $C_{OUT}$ significantly or without the output capacitor. If the values of $C_{OUT}$ ($\sim$1 μF) and $R_{ESR}$ ($\sim$0.001 Ω) are small and $C_{OUT}R_{ESR} \ll C_{m2}/g_{m2}$, the damping factor is approximated as

$$\zeta \simeq \frac{1}{2}\sqrt{\frac{C_{m2}}{g_{m2}} \cdot \frac{g_{mp}}{C_{OUT}}} \tag{12}$$

To have a small $C_{m2}$, $g_{m2}$ can be reduced to realise an appropriate damping factor. Unfortunately, it lowers the dc-loop gain of the LDR to reduce $g_{m2}$. To have a large dc

loop gain of the LDR, that is, $g_{m2}$ is increased and a large $C_{m2}$ is needed, too. It means that there is a trade-off between the damping factor and the dc loop gain. Reversely, if the values of $C_{OUT}$ ($\sim$10 μF) and $R_{ESR}$ ($\sim$10 Ω) are large and $C_{OUT}R_{ESR} \gg C_{m2}/g_{m2}$, the damping factor is approximated to

$$\zeta \simeq \frac{R_{ESR}}{2}\sqrt{\frac{g_{m2}g_{mp}C_{OUT}}{C_{m2}}} \tag{13}$$

A large damping factor is realised and two real poles are separated, so the stability is assured.

Besides, the numerator of the loop gain in (5) has three zeros. From the first-order polynomial in the numerator of (5), the ESR zero is located at

$$z_{ESR} = \frac{1}{C_{OUT}R_{ESR}} \tag{14}$$

From the second-order polynomial in the numerator of (5), one zero is in the right half-plane (RHP) and the other is in the left half-plane (LHP). They are expressed as

$$\begin{aligned} z_{RHP} &= \frac{g_{m2}}{2C_{m1}}\left(1 - \sqrt{\frac{4C_{m1}g_{mp}}{C_{m2}g_{m2}} + 1}\right) \\ z_{LHP} &= \frac{g_{m2}}{2C_{m1}}\left(1 + \sqrt{\frac{4C_{m1}g_{mp}}{C_{m2}g_{m2}} + 1}\right) \end{aligned} \tag{15}$$

Obviously, these three zeros occur at very high frequencies even much higher than the non-dominant poles, so their effects can be neglected.

Fig. 2 shows the loop frequency response of the conventional LDR and the LDR using NMC technique. On the basis of the above analyses, some results are observed as follows. For a conventional LDR [1], a big output capacitor is required to lower the dominant pole for the sake of stability considerations. It is difficult to integrate the big output capacitor on a chip. For an LDR [4] using the NMC technique, the output capacitor contributes to the non-dominant pole, and the output capacitor can be lowered to reduce the area and cost. In the light load (i.e. the output current is low), the non-dominant poles are close to the unity-gain frequency. To be stable, a large $C_{m1}$ is needed to lower the dominant pole to adopt the single-pole system within the unity-gain frequency. In the heavy load, when the output current grows, the non-dominant poles increase, too. However, a small damping factor may occur if the output capacitor is small enough. To have an appropriate damping factor, a large $C_{m2}$ is needed.

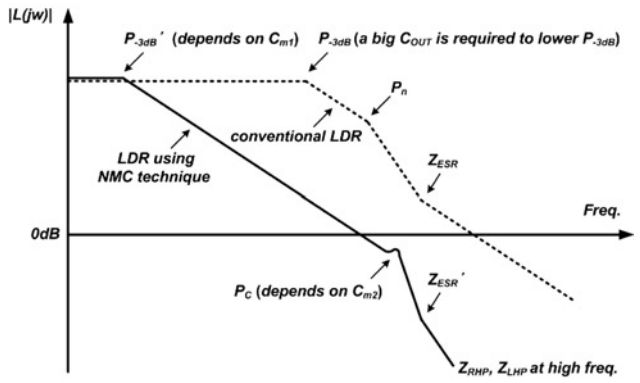


**Figure 2** *Frequency response of the conventional LDR and the LDR using NMC technique*

## 2.2 Without output capacitor

To realise a system with the on-chip regulator, it is desirable to reduce or eliminate the output capacitor. If the output capacitor is eliminated, the loop gain of the regulator in Fig. 1*a* is expressed as

$$L(s) = \frac{A_0(1 - s(C_{m2}/g_{mp}) - s^2(C_{m1}C_{m2}/g_{m2}g_{mp}))}{(1 + (s/p_{-3dB}))(1 + s(C_{m2}/g_{m2}))} \tag{16}$$

Clearly, the dominant pole is unchanged, but the non-dominant pole is given as

$$p_n = \frac{g_{m2}}{C_{m2}} \tag{17}$$

From (7) and (16), the stability of the LDR highly depends on $C_{m1}$ and $C_{m2}$. It is possible to realise the dominant pole at a lower frequency and the non-dominant pole higher than the unity-gain frequency to achieve a stable system. When the output capacitor does not exist, this LDR has a single pole within the unity-gain frequency, and it is an unconditional stable system. Besides, the numerator in (15) has two zeros, which occur at very high frequencies and even much higher than the non-dominant pole. Their effects are neglected.

# 3 Proposed LDRs

In order to control the damping factor effectively and reduce the required Miller compensation capacitance, an LDR using the NMC with an active resistor (NMCAR) is presented; it is called an NMCAR LDR. It can resolve the trade-off between the dc loop gain and damping factor, which existed in the LDR using the NMC technique. To reduce the total Miller compensation capacitances further and the recovery time, a capacitor-free LDR is presented by using both the NMCAR and a 1-bit PCA. Both the LDRs are described as follows.

## 3.1 NMCAR LDR

The proposed NMCAR LDR and its small-signal model are shown in Figs. 3*a* and 3*b*, respectively. For Fig. 3*a*, the first stage is realised by a differential amplifier, $M_{1a}$–$M_{1e}$. The second stage is composed of $M_2$–$M_5$ and $M_a$. The power PMOS transistor is $M_p$. The first frequency compensation capacitor, $C_{m1}$, and the second one, $C_{m2}$, series with a




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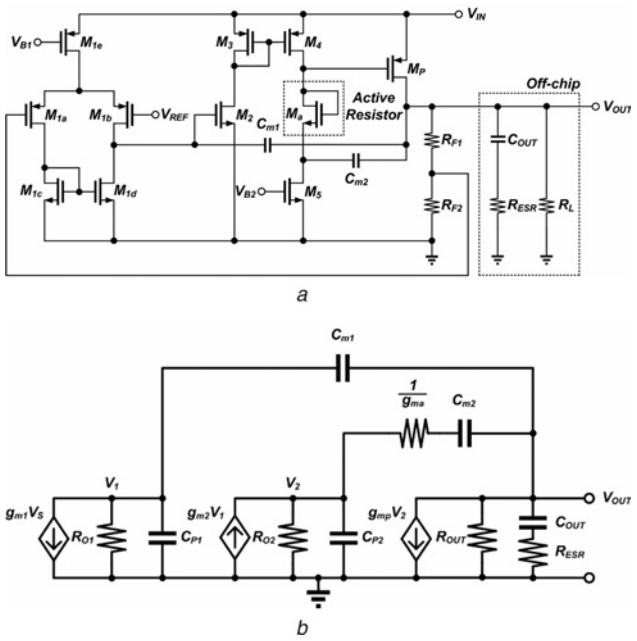


**Figure 3** *Proposed NMCAR LDR*

*a* NMCAR LDR
*b* Its equivalent small-signal model

diode-connected NMOS $M_a$ realise the proposed NMCAR technique. The impedance seen at the source of $M_a$ is $1/g_{ma}$ without considering the body effect. If $g_{ma} \ll g_{mp}$, the small signal loop gain of the regulator in Fig. 3*b* is expressed as

$$L(s) = \frac{A_0(1 + s(C_{m2}/g_{ma}) - s^2(C_{m1}C_{m2}/g_{m2}g_{mp}))}{(1 + sC_{OUT}R_{ESR})} \frac{(1 + sC_{OUT}R_{ESR})}{(1 + (s/p_{-3dB}))[1 + s(C_{OUT}R_{ESR} + (C_{m2}/g_{m2}) + (C_{m2}/g_{ma})) + s^2(C_{m2}C_{OUT}/g_{m2}g_{mp})]} \quad (18)$$

Similarly, the damping factor is derived as

$$\zeta = \frac{1}{2}\left(C_{OUT}R_{ESR} + \frac{C_{m2}}{g_{m2}} + \frac{C_{m2}}{g_{ma}}\right)\sqrt{\frac{g_{m2}g_{mp}}{C_{m2}C_{OUT}}} \quad (19)$$

Assume that the NMC LDR and the NMCAR LDR have the same total Miller capacitances. The simulated frequency responses of these LDRs are shown in Fig. 4. In NMCAR LDR, a small $g_{ma}$ enhances the damping factor without influencing the dc loop gain and without increasing $C_{m2}$. Comparing (10) with (18), if $C_{OUT}R_{ESR} \ll C_{m2}/g_{m2}$, the required $C_{m2}$ is much smaller than that of Fig. 1*a* by a factor of $1 + g_{m2}/g_{ma}$. Therefore the damping factor is controlled by $g_{ma}$ instead of $g_{m2}$.

Besides, the numerator of (17) has three zeros. From the first-order polynomial in the numerator of (17), it is an ESR zero at

$$z_{ESR} = \frac{1}{C_{OUT}R_{ESR}} \quad (20)$$

From the second-order polynomial in the numerator of (17), an RHP zero and an LHP zero are given as

$$z_{RHP} = \frac{g_{m2}g_{mp}}{2C_{m1}g_{ma}}\left(-1 - \sqrt{\frac{4C_{m1}g_{ma}^2}{C_{m2}g_{m2}g_{mp}} + 1}\right)$$
$$z_{LHP} = \frac{g_{m2}g_{mp}}{2C_{m1}g_{ma}}\left(-1 + \sqrt{\frac{4C_{m1}g_{ma}^2}{C_{m2}g_{m2}g_{mp}} + 1}\right) \quad (21)$$

Similarly, as three zeros occur at very high frequencies even much higher than the non-dominant poles, their effects can be also neglected.

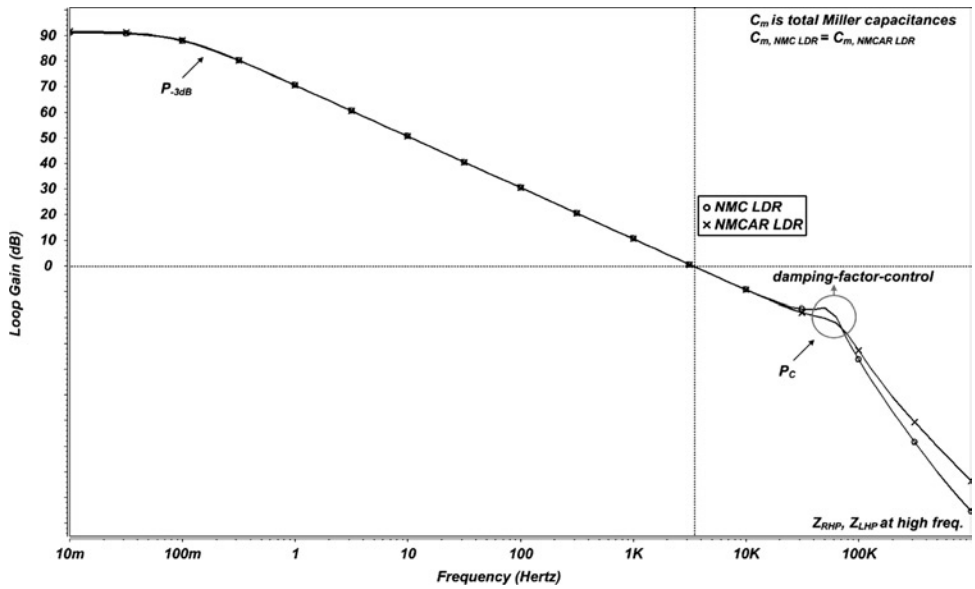


**Figure 4** *Simulated frequency responses of the NMC LDR and the NMCAR LDR*

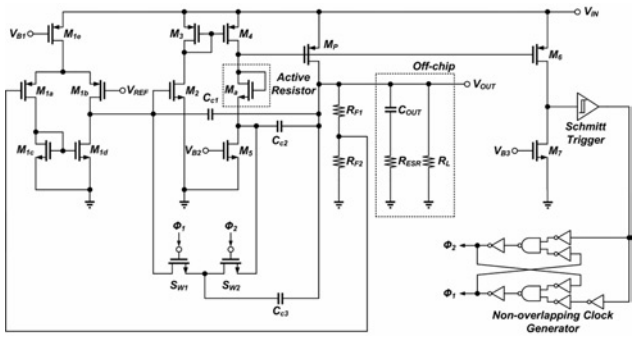


**Figure 5** *NMCAR LDR with a 1-bit PCA*

## 3.2 NMCAR LDR with a 1-bit PCA

For the sake of stability considerations, if the output capacitor is small, a large $C_{m1}$ is required to lower the dominant pole in the light load. In addition, a large $C_{m2}$ is required to control the damping factor in the heavy load. Hence, $C_{m1}$ and $C_{m2}$ have the different requirements in the light and heavy loads, respectively. To reduce the total required area of the frequency compensation capacitances, the NMCAR LDR with a 1-bit PCA is shown in Fig. 5. To take a glance of the proposed circuit, it seems that three frequency compensation capacitors are needed and the area is increased. However, it is not true. In fact, the total

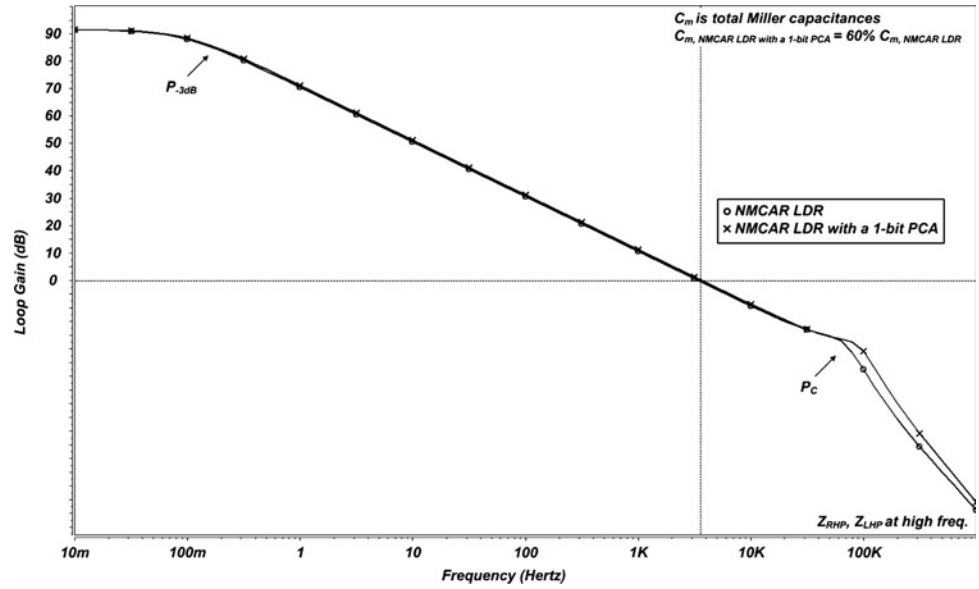


**Figure 6** *Simulated frequency responses of the NMCAR LDR with and without a 1-bit PCA in the light loads*

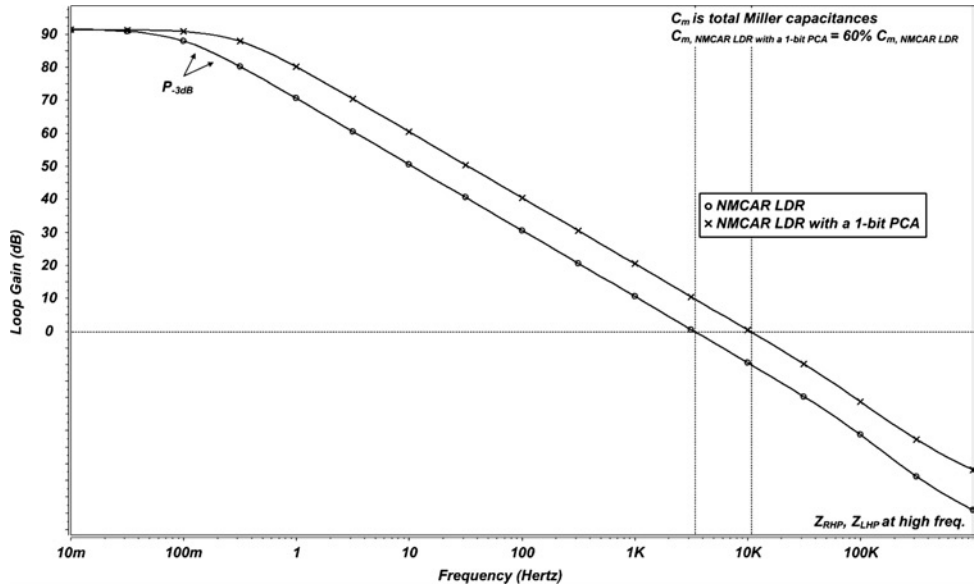


**Figure 7** *Simulated frequency responses of the NMCAR LDR with and without a 1-bit PCA in the heavy loads*



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**Table 1** Summary of the frequency compensation parameters of the NMC and the proposed LDRs

| | NMC LDR | NMCAR LDR | NMCAR LDR with a 1-bit PCA |
|---|---|---|---|
| $I_{OUT} = 0$ mA, $C_{OUT} \neq 0$ | $p_{-3dB} = \frac{1}{C_{m1}g_{m2}g_{mp}R_{O1}R_{O2}R_{OUT}}$,<br>$\zeta = \frac{1}{2}\left(C_{OUT}R_{ESR} + \frac{C_{m2}}{g_{m2}}\right)\sqrt{\frac{g_{m2}g_{mp}}{C_{m2}C_{OUT}}}$,<br>$z_{ESR} = \frac{1}{C_{OUT}R_{ESR}}$,<br>$z_{RHP} = \frac{g_{m2}}{2C_{m1}}\left(1 - \sqrt{\frac{4C_{m1}g_{mp}}{C_{m2}g_{m2}} + 1}\right)$,<br>$z_{LHP} = \frac{g_{m2}}{2C_{m1}}\left(1 + \sqrt{\frac{4C_{m1}g_{mp}}{C_{m2}g_{m2}} + 1}\right)$ | $p_{-3dB} = \frac{1}{C_{m1}g_{m2}g_{mp}R_{O1}R_{O2}R_{OUT}}$,<br>$\zeta = \frac{1}{2}\left(C_{OUT}R_{ESR} + \frac{C_{m2}}{g_{m2}} + \frac{C_{m2}}{g_{ma}}\right)\sqrt{\frac{g_{m2}g_{mp}}{C_{m2}C_{OUT}}}$,<br>$z_{ESR} = \frac{1}{C_{OUT}R_{ESR}}$,<br>$z_{RHP} = \frac{g_{m2}g_{mp}}{2C_{m1}g_{ma}}\left(-1 - \sqrt{\frac{4C_{m1}g_{ma}^2}{C_{m2}g_{m2}g_{mp}} + 1}\right)$,<br>$z_{LHP} = \frac{g_{m2}g_{mp}}{2C_{m1}g_{ma}}\left(-1 + \sqrt{\frac{4C_{m1}g_{ma}^2}{C_{m2}g_{m2}g_{mp}} + 1}\right)$ | $p_{-3dB} = \frac{1}{0.92C_{m1}g_{m2}g_{mp}R_{O1}R_{O2}R_{OUT}}$,<br>$\zeta = \frac{1}{2}\left(C_{OUT}R_{ESR} + \frac{0.28C_{m2}}{g_{m2}} + \frac{0.28C_{m2}}{g_{ma}}\right)\sqrt{\frac{g_{m2}g_{mp}}{0.28C_{m2}C_{OUT}}}$,<br>$z_{ESR} = \frac{1}{C_{OUT}R_{ESR}}$,<br>$z_{RHP} = \frac{g_{m2}g_{mp}}{1.84C_{m1}g_{ma}}\left(-1 - \sqrt{\frac{3.68C_{m1}g_{ma}^2}{0.28C_{m2}g_{m2}g_{mp}} + 1}\right)$,<br>$z_{LHP} = \frac{g_{m2}g_{mp}}{1.84C_{m1}g_{ma}}\left(-1 + \sqrt{\frac{3.68C_{m1}g_{ma}^2}{0.28C_{m2}g_{m2}g_{mp}} + 1}\right)$ |
| $I_{OUT} = 150$ mA, $C_{OUT} \neq 0$ | | | $p_{-3dB} = \frac{1}{0.32C_{m1}g_{m2}g_{mp}R_{O1}R_{O2}R_{OUT}}$,<br>$\zeta = \frac{1}{2}\left(C_{OUT}R_{ESR} + \frac{0.88C_{m2}}{g_{m2}} + \frac{0.88C_{m2}}{g_{ma}}\right)\sqrt{\frac{g_{m2}g_{mp}}{0.88C_{m2}C_{OUT}}}$,<br>$z_{ESR} = \frac{1}{C_{OUT}R_{ESR}}$,<br>$z_{RHP} = \frac{g_{m2}g_{mp}}{0.64C_{m1}g_{ma}}\left(-1 - \sqrt{\frac{1.28C_{m1}g_{ma}^2}{0.88C_{m2}g_{m2}g_{mp}} + 1}\right)$,<br>$z_{LHP} = \frac{g_{m2}g_{mp}}{0.64C_{m1}g_{ma}}\left(-1 + \sqrt{\frac{1.28C_{m1}g_{ma}^2}{0.88C_{m2}g_{m2}g_{mp}} + 1}\right)$ |
| $I_{OUT} = 0$ mA, $C_{OUT} = 0$ | $p_{-3dB} = \frac{1}{C_{m1}g_{m2}g_{mp}R_{O1}R_{O2}R_{OUT}}$,<br>$p_n = \frac{g_{m2}}{C_{m2}}$ | $p_{-3dB} = \frac{1}{C_{m1}g_{m2}g_{mp}R_{O1}R_{O2}R_{OUT}}$,<br>$p_n = \frac{g_{m2}}{C_{m2}}\left(\frac{1}{1+g_{m2}/g_{ma}}\right)$ | $p_{-3dB} = \frac{1}{0.92C_{m1}g_{m2}g_{mp}R_{O1}R_{O2}R_{OUT}}$,<br>$p_n = \frac{g_{m2}}{0.28C_{m2}}\left(\frac{1}{1+g_{m2}/g_{ma}}\right)$ |
| $I_{OUT} = 150$ mA, $C_{OUT} = 0$ | | | $p_{-3dB} = \frac{1}{0.32C_{m1}g_{m2}g_{mp}R_{O1}R_{O2}R_{OUT}}$,<br>$p_n = \frac{g_{m2}}{0.88C_{m2}}\left(\frac{1}{1+g_{m2}/g_{ma}}\right)$ |

frequency compensation capacitance in the NMCAR LDR is larger.

The current of $M_p$ is sensed by $M_6$ in Fig. 5. This current is compared with a constant current source, $M_7$, and the result drives the Schmitt trigger [8] and non-overlapping clock generator to generate two non-overlapping clocks, $\Phi_1$ and $\Phi_2$. The Schmitt trigger with a hysteresis is to avoid the switching noise and speed up the transition time [8]. The non-overlapping clocks avoid to turning on both switches, $S_{W1}$ and $S_{W2}$ simultaneously. When the output current is very small and close to zero, a small gate–source voltage biased the power PMOS transistor in cut-off region to fix the output voltage. During the light load, the output current is increased and the power PMOS transistor works in the saturation region. The clock $\Phi_1$ is high and the switch $S_{W1}$ is on ($\Phi_2$ is low and $S_{W2}$ is off). It is equivalent to add $C_{c1}$ with $C_{c3}$ to make $C_{m1}$. It lowers both the dominant pole and unity-gain frequency to have a good phase margin in the light load. Compared with the NMCAR LDR, this LDR with a 1-bit PCA reduces 40% of the total on-chip frequency compensation capacitance. The simulated frequency responses of these two LDRs are similar in the light load, as shown in Fig. 6. When the output current crosses the threshold level, this 1-bit PCA is triggered and the polarities of the clocks, $\Phi_1$ and $\Phi_2$, are changed. It equivalently adds $C_{c2}$ with $C_{c3}$ to make $C_{m2}$ and it enhances the damping factor in the heavy load and further extends the bandwidth because of the smaller capacitor on the first frequency compensation loop. On the basis of the simulation results, to achieve the suitable phase margin and damping factor for all operated frequency bands, this threshold level is designed close to 2% of the maximum output current, that is, 3 mA. In the heavy load, the power PMOS transistor still operates in the saturation region. In addition, the power PMOS transistor operates in the triode region at dropout if the input voltage is lowered enormously.

According to (11), the GBW is placed to be less than 1/2 of complex pole. In the light load, $C_{c3}$ is switched to $C_{c1}$. The dimension conditions of $C_{c1}$, $C_{c2}$ and $C_{c3}$ are given by

$$2\frac{g_{m1}}{(C_{C1}+C_{C3})}\left(\frac{R_{F2}}{R_{F1}+R_{F2}}\right) \le \sqrt{\frac{g_{m2}g_{mp}}{C_{C2}C_{OUT}}} \quad (22)$$

In the heavy load, the transconductance of the power PMOS transistor is enhanced and $C_{c3}$ is switched to $C_{c2}$. The dimension conditions of $C_{c1}$, $C_{c2}$ and $C_{c3}$ are then given by

$$2\frac{g_{m1}}{C_{C1}}\left(\frac{R_{F2}}{R_{F1}+R_{F2}}\right) \le \sqrt{\frac{g_{m2}g_{mp}}{(C_{C2}+C_{C3})C_{OUT}}} \quad (23)$$

Thus, the GBW and complex poles are limited by the range of the $C_{OUT}$. If $C_{OUT}$ is increased to reduce the noise and voltage dip of the output voltage, the total required compensation capacitances will increase. In this case, the range of $C_{OUT}$ is form 0 to 1 μF. To reduce the total required compensation capacitances and fit the above dimension conditions, $C_{c1}$, $C_{c2}$ and $C_{c3}$ are chosen by $2C_{c1} = 2C_{c2} = C_{c3} = 30$ pF. Compared with the NMCAR LDR without a 1-bit PCA, one with a 1-bit PCA raises both the dominant pole and unity-gain frequency in the heavy load, as shown in Fig. 7. Its recovery time is enhanced owing to the lower total compensation capacitances in the transient response and a higher unity-gain frequency in the frequency response. Finally, Table 1 summarises the frequency compensation parameters of the NMC and proposed LDRs.

**Table 2** The central device sizes used in the proposed LDRs

| | NMCAR LDR | NMCAR LDR with a 1-bit PCA |
|---|---|---|
| $M_{1a}$ | 4 μm/4 μm | |
| $M_{1b}$ | 4 μm/4 μm | |
| $M_{1c}$ | 2 μm/12 μm | |
| $M_{1d}$ | 2 μm/12 μm | |
| $M_{1e}$ | 2 μm/6 μm | |
| $M_2$ | 6 μm/12 μm | |
| $M_3$ | 1 μm/0.4 μm | |
| $M_4$ | 4 μm/0.4 μm | |
| $M_5$ | 24 μm/12 μm | |
| $M_a$ | 12 μm/12 μm | 8 μm/12 μm |
| $M_P$ | 10 800 μm/0.4 μm | |
| $R_{F1}$ | 186.665 kΩ | |
| $R_{F2}$ | 56 kΩ | |
| $C_{compensation}$ | $C_{m1} = 50$ pF, $C_{m2} = 50$ pF | $C_{c1} = 16$ pF, $C_{c2} = 14$ pF, $C_{c3} = 30$ pF |

## 4 Experimental results

Two proposed LDRs with bandgap voltage references have been fabricated in a 0.35 μm CMOS process. The central

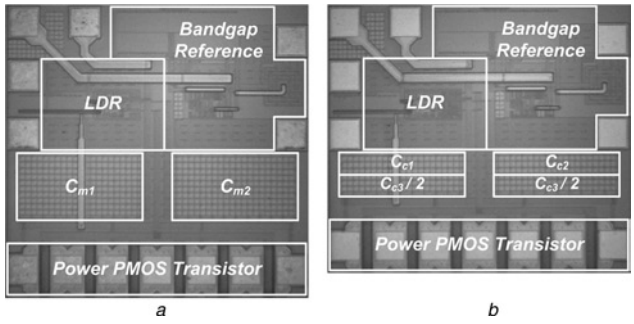


**Figure 8** *Die photos*
*a* NMCAR LDR
*b* NMCAR LDR with a 1-bit PCA



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device sizes used in the proposed LDRs are listed in Table 2. Their photos are shown in Figs. 8*a* and 8*b*, where the active area of the NMCAR LDRs without and with a 1-bit PCA is 0.67 and 0.60 $mm^2$, respectively. The maximum output current is 150 mA with 1.8 V output voltage for the supply voltage changed from 2 to 5 V. The measured quiescent currents with $V_{IN} = 2$ V and $V_{IN} = 5$ V are 39 and 43.8 μA, respectively. The measured line regulation for both the proposed LDRs is less than 0.05%/*V* and 0.06%/*V* at the output current $I_{OUT} = 0$ mA and $I_{OUT} = 150$ mA, respectively. In addition, the measured load regulation is less than 60 ppm/mA at 3.3 V supply voltage.

## 4.1 Experimental results of the NMCAR LDR

For the LDR using the NMCAR technique, Fig. 9 shows the measured transient responses of the LDR at 3.3 V with the output current switching from 0 to 150 mA for the output capacitor of $C_{OUT} = 1$ μF and $R_{ESR} = 1$ Ω (Fig. 9*a*), $C_{OUT} = 1$ μF and $R_{ESR} = 0.3$ Ω (Fig. 9*b*) and $C_{OUT} = 0$ (Fig. 9*c*), respectively. The experimental results show that the proposed LDR can recover to the preset output voltage within 8 μs under $C_{OUT} = 1$ μF and $R_{ESR} = 1$ Ω. The proposed LDR increase the tolerance to the ESR of the output capacitor while greatly improving the damping factor without compromise on dc loop gain. Hence, when a small ESR is used, the damping transient response is improved and its recovery time is faster than that with a high ESR.

## 4.2 Experimental results of the NMCAR LDR with a 1-bit PCA

For the NMCAR LDR with a 1-bit PCA, Fig. 10 shows the measured transient responses of the LDR at 3.3 V with the output current switching from 0 to 150 mA for the output capacitor of $C_{OUT} = 1$ μF and $R_{ESR} = 1$ Ω (Fig. 10*a*), $C_{OUT} = 1$ μF and $R_{ESR} = 0.3$ Ω (Fig. 10*b*) and $C_{OUT} = 0$ (Fig. 10*c*), respectively. The experimental results show that the proposed LDR can recover to the preset output voltage within 6 μs under $C_{OUT} = 1$ μF and $R_{ESR} = 1$ Ω. The recovery time is enhanced, compared with the NMCAR LDR. When $C_{c3}$ is switched from one state to another, it may induce the charge injection to the output voltage in the transient. However, the proposed LDR regulates the output voltage by a high loop gain. The measured transient response, line regulation and load regulation demonstrate that the charge injection does not significantly impact on its stability and regulation.

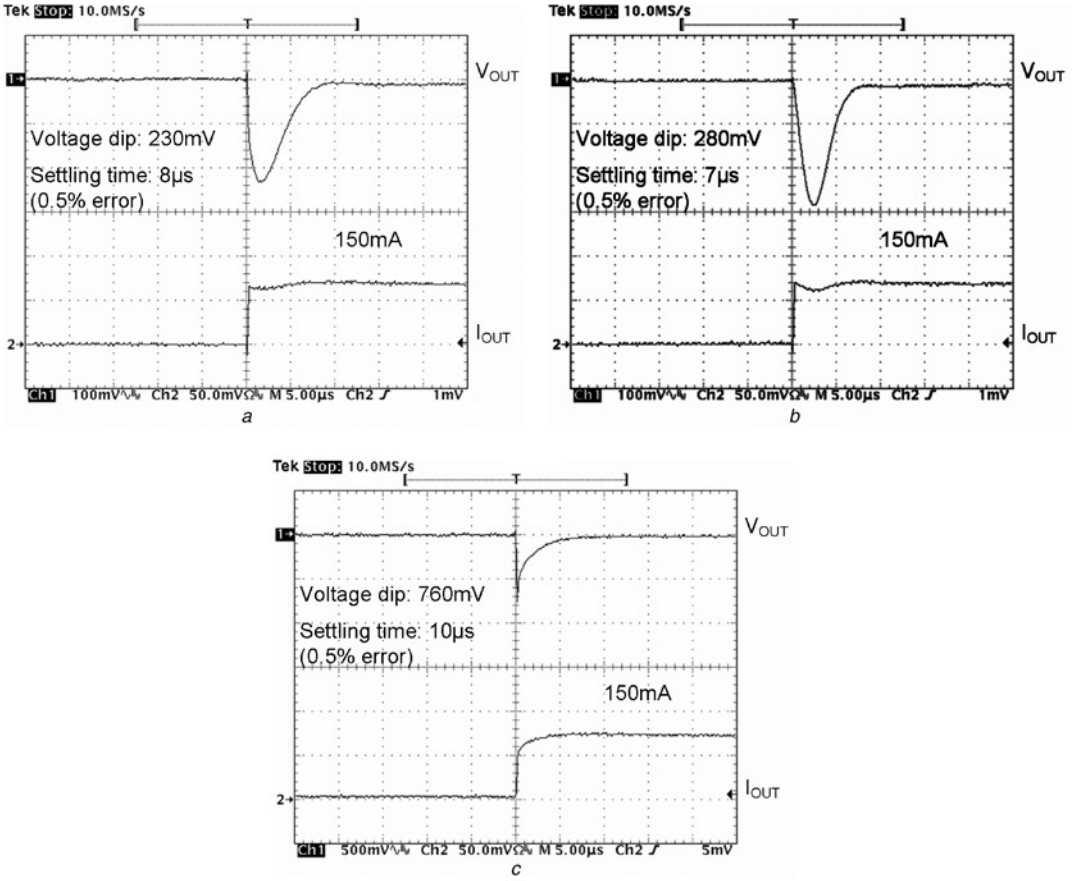


**Figure 9** *Transient response of the NMCAR LDR at $V_{IN} = 3.3$ V with the output current switching from 0 to 150 mA*

*a* $C_{OUT} = 1$ μF and $R_{ESR} = 1$ Ω
*b* $C_{OUT} = 1$ μF and $R_{ESR} = 0.3$ Ω
*c* $C_{OUT} = 0$

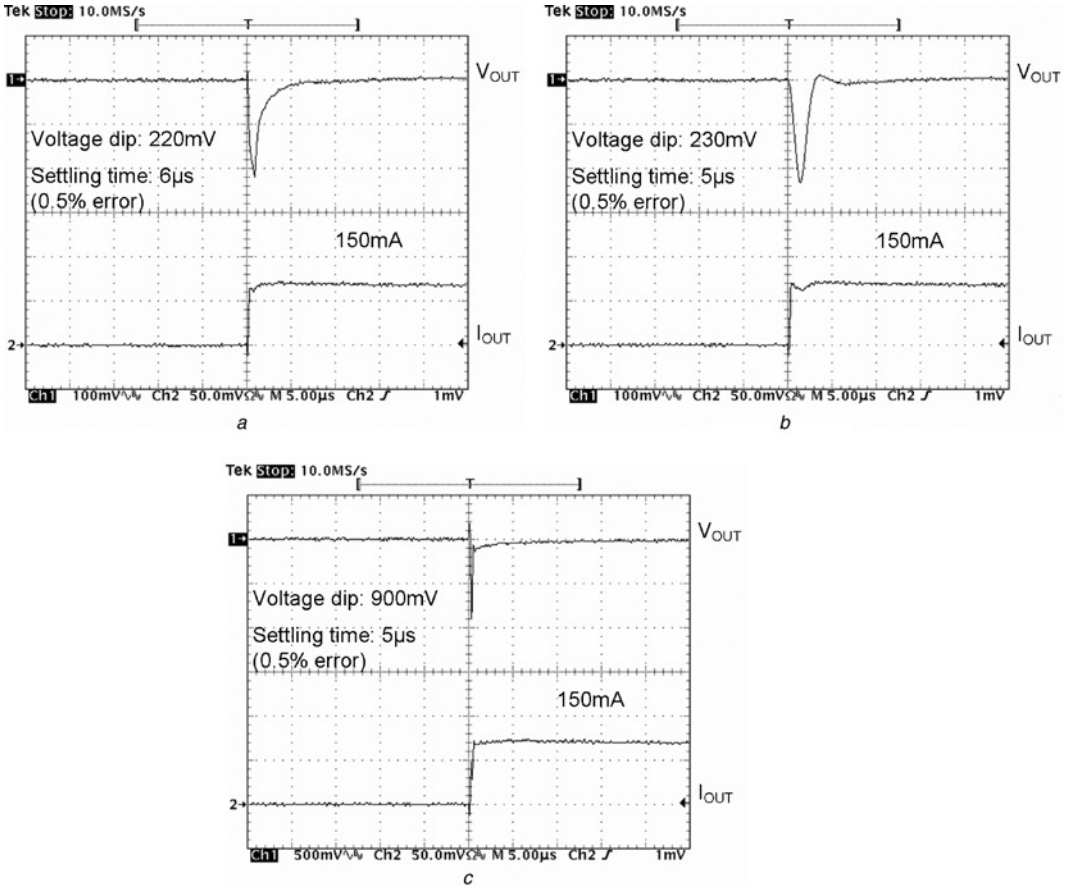


**Figure 10** *Transient response of the NMCAR LDR with a 1-bit PCA at $V_{IN} = 3.3$ V with the output current switching from 0 to 150 mA*

*a* $C_{OUT} = 1$ µF and $R_{ESR} = 1\ \Omega$
*b* $C_{OUT} = 1$ µF and $R_{ESR} = 0.3\ \Omega$
*c* $C_{OUT} = 0$

Fig. 11*a* shows the transient response of the LDR with the output current switching from 0 to 50 mA for $C_{OUT} = 0$. Fig. 11*b* shows that with the output current switching from 0 to 20 mA for $C_{OUT} = 0$. In addition, the experimental results indicate that the LDR with a 1-bit PCA does not influence its stability for switching different output currents.

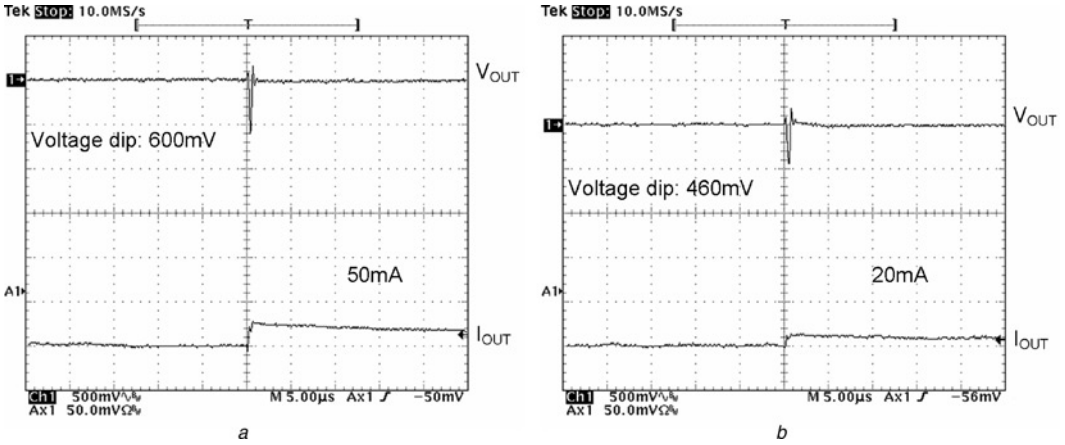


**Figure 11** *Transient response of the NMCAR LDR with a 1-bit PCA at $V_{IN} = 3.3$ V for $C_{OUT} = 0$*

*a* With output current switching from 0 to 50 mA
*b* With output current switching from 0 to 20 mA




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**Table 3** Performance summary

| | | NMCAR LDR | NMCAR LDR with a 1-bit PCA |
|---|---|---|---|
| process | | 3.3 V 0.35 μm CMOS | |
| supply voltage | | 2–5 V | |
| output voltage | | 1.8 V | |
| max. output current | | 150 mA | |
| quiescent current | $V_{IN} = 2$ V | bandgap reference: 19.4 μA LDR: 19.6 μA | |
| | $V_{IN} = 5$ V | bandgap reference: 23.6 μA LDR: 20.2 μA | |
| line regulation | $I_{OUT} = 0$ mA | $<0.05\%/V$ | |
| | $I_{OUT} = 150$ mA | $<0.06\%/V$ | |
| load regulation | | $<60$ ppm/mA | |
| settling time (voltage dip) | $C_{OUT} = 1$ μF, $R_{ESR} = 1$ Ω | 8 μs (230 mV) | 6 μs (220 mV) |
| | $C_{OUT} = 1$ μF, $R_{ESR} = 0.3$ Ω | 7 μs (280 mV) | 5 μs (230 mV) |
| | $C_{OUT} = 0$ | 10 μs (760 mV) | 5 μs (900 mV) |
| active chip area | | 0.67 mm$^2$ | 0.60 mm$^2$ |

### 4.3 Performance comparisons

Table 3 summarises the measured performances for two LDRs. The NMCAR LDR with a 1-bit PCA significantly reduces the required frequency compensation capacitances, and further quickens the recovery speed without increasing the quiescent current. Table 4 gives the comparisons with other LDRs. Compared with [1] and [3], the proposed LDRs achieve the capacitor-free operation. In [5], the LDR is compensated by introducing two zeros, $z_e$ and $z_f$, to cancel the non-dominant poles within the unity-gain frequency to extend the bandwidth, while $z_e$ is ESR zero and $z_f$ is coming from on-chip passive devices, the stability would be easily affected from the process variation. The proposed LDRs always adopt the single-pole system within the unity-gain frequency to achieve an unconditional stable.

## 5 Conclusion

Two LDRs using the proposed NMCAR and a 1-bit PCA are presented. Both the LDRs have been fabricated in a 0.35 μm CMOS process. Experimental results demonstrate the proposed LDRs. The NMCAR LDR can effectively control the damping factor and reduce the required Miller compensation capacitance. It can also resolve the trade-off between dc loop gain and damping factor, which existed in the LDR using the NMC. Unlike pole-zero cancellation within the unity-gain frequency, the proposed LDRs always adopt the single-pole system within the unity-gain frequency to achieve an unconditional stable. To reduce the total Miller compensation capacitances further, a capacitor-free CMOS

**Table 4** Performance comparisons

| | Rincon-Mora and Allen [2] | Rincon-Mora [3] | Leung and Mok [5] | NMCAR LDR | NMCAR LDR with a 1-bit PCA |
|---|---|---|---|---|---|
| process | 2 μm CMOS | 1 μm BiCMOS | 0.6 μm CMOS | 0.35 μm CMOS | |
| supply voltage, V | 1.2–10 | 1.25–8 | 1.5–4.5 | 2–5 | |
| output voltage, V | 0.9 | 0.9 | 1.3 | 1.8 | |
| max. output current, mA | 50 | 200 | 100 | 150 | |
| max. quiescent current, μA | 230 ($V_{IN} = 1.2$ V) | N/A | 38 ($V_{IN} = 2$ V) | 39 ($V_{IN} = 2$ V) | |
| line regulation, %/V | 0.117 | 0.222 | 0.124 | 0.06 | |
| load regulation, ppm/mA | 422 | 305 | N/A | 60 | |
| settling time, μs | N/A | N/A | 2 ($C_{OUT} = 0$) | 10 ($C_{OUT} = 0$) | 5 ($C_{OUT} = 0$) |
| active area, mm$^2$ | 1.3787 | N/A | 0.3073 | 0.67 | 0.60 |
| capacitor-free | no | no | yes | yes | |

LDR is presented by using both the NMCAR and a 1-bit PCA. It also speeds up the recovery time.

## 6 Acknowledgment

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