A hybrid nanomemristor/transistor logic circuit capable of self-programming

Julien Borghetti, Zhiyong Li, Joseph Straznicky, Xuema Li, Douglas A. A. Ohlberg, Wei Wu, Duncan R. Stewart, and R. Stanley Williams[1]

Information and Quantum Systems Lab, Hewlett-Packard Laboratories, 1501 Page Mill Road, Palo Alto, CA 94304

Edited by Konstantin Likharev, State University of New York, Stony Brook University, and accepted by the Editorial Board December 19, 2008 (received for review July 9, 2008)

Memristor crossbars were fabricated at 40 nm half-pitch, using nanoimprint lithography on the same substrate with Si metal-oxide-semiconductor field effect transistor (MOS FET) arrays to form fully integrated hybrid memory resistor (memristor)/transistor circuits. The digitally configured memristor crossbars were used to perform logic functions, to serve as a routing fabric for interconnecting the FETs and as the target for storing information. As an illustrative demonstration, the compound Boolean logic operation (A AND B) OR (C AND D) was performed with kilohertz frequency inputs, using resistor-based logic in a memristor crossbar with FET inverter/amplifier outputs. By routing the output signal of a logic operation back onto a target memristor inside the array, the crossbar was conditionally configured by setting the state of a nonvolatile switch. Such conditional programming illuminates the way for a variety of self-programmed logic arrays, and for electronic synaptic computing.

crossbar | integrated circuit | memristor | nanoimprint lithography

The memory resistor (memristor), the 4th basic passive circuit element, was originally predicted to exist by Leon Chua in 1971 (1) and was later generalized to a family of dynamical systems called memristive devices in 1976 (2). For simplicity in the exposition of this article, we will use the word "memristor" to mean either a "pure" memristor or a memristive device, because the distinction is not important in the context of the present discussion. The first intentional working examples of these devices, along with a simplified physics-based model for how they operate, were described in 2008 (3, 4). A memristor is a 2-terminal thin-film electrical circuit element that changes its resistance depending on the total amount of charge that flows through the device. This property arises naturally in systems for which the electronic and dopant equations of motion in a semiconductor are coupled in the presence of an applied electric field. The magnitude of the nonlinear or charge dependent component of memristance in a semiconductor film is proportional to the inverse square of the thickness of the film, and thus becomes very important at the nanometer scale (3).

Memristance is very interesting for a variety of digital and analog switching applications (1, 2), especially because a memristor does not lose its state when the electrical power is turned off (the memory is nonvolatile). Because they are passive elements (they cannot introduce energy into a circuit), memristors need to be integrated into circuits with active circuit elements such as transistors to realize their functionality. However, because a significant number of transistors are required to emulate the properties of a memristor (1), hybrid circuits containing memristors and transistors can deliver the same or enhanced functionality with many fewer components, thus providing dramatic savings for both chip area and operating power. Perhaps the ideal platform for using memristors is a crossbar array, which is formed by connecting 2 sets of parallel wires crossing over each other with a switch at the intersection of each wire pair (see Fig. 1).

Crossbars have been proposed for and implemented in a variety of nanoscale electronic integrated circuit architectures, such as memory and logic systems (5–12). A 2-dimensional grid offers several advantages for computing at the nanoscale: It is scalable down to the molecular scale (13, 14), it is a regular structure that can be configured by closing junctions to express a high degree of complexity and reconfigured to tolerate defects in the circuit (15–17), and because of its structural simplicity it can be fabricated inexpensively with nanoimprint lithography (7, 18, 19). We previously demonstrated ultrahigh density memory and crossbar latches (20). Recently, new hybrid circuits combining complementary metal-oxide-semiconductor (CMOS) technology with nanoscale switches in crossbars, called CMOS-molecule [CMOL (21)] and field-programmable nanowire interconnect [FPNI (22)], have been proposed. These field-programmable gate array (FPGA)-like architectures combine the advantages of CMOS (high yield, high gain, versatile functionality) with the reconfigurability and scalability of nanoscale crossbars. Simulations of these architectures have shown that by removing the transistor-based configuration memory and associated routing circuits from the plane of the CMOS transistors and replacing them with a crossbar network in a layer of metal interconnect above the plane of the silicon, the total area of an FPGA can be decreased by a factor of 10 or more while simultaneously increasing the clock frequency and decreasing the power consumption of the chip (21, 22).

Here, we present the first feasibility demonstration for the integration and operation of nanoscale memristor crossbars with monolithic on-chip FETs. In this case, the memristors were simply used as 2-state switches (ON and OFF, or switch closed and opened, respectively) rather than dynamic nonlinear analog device to perform wired-logic functions and signal routing for the FETs; the FETs were operated in either follower or inverter/amplifier modes to illustrate either signal restoration or fast operation of a compound binary logic function, "(A AND B) OR (C AND D)," more conveniently written using the Boolean algebra representation as AD + CD, in which logical AND is represented by multiplication and OR by addition. These exercises were the prelude to the primary experiment of this article, which was the conditional programming of a nanomemristor within a crossbar array by the hybrid circuit. We thus provide a proof-of-principles validation that the same devices in a nanoscale circuit can be configured to act as logic, signal routing and memory, and the circuit can even reconfigure itself.

Author contributions: J.B., Z.L., J.S., D.R.S., and R.S.W. designed research; J.B., Z.L., X.L., D.A.A.O., and W.W. performed research; J.B., Z.L., J.S., X.L., D.A.A.O., W.W., and D.R.S. contributed new reagents/analytic tools; J.B., Z.L., and R.S.W. analyzed data; and J.B., Z.L., and R.S.W. wrote the paper.

The authors declare no conflict of interest.

This article is a PNAS Direct Submission. K.L. is a guest editor invited by the Editorial Board.

Freely available online through the PNAS open access option.

[1]To whom correspondence should be addressed. E-mail: stan.williams@hp.com.

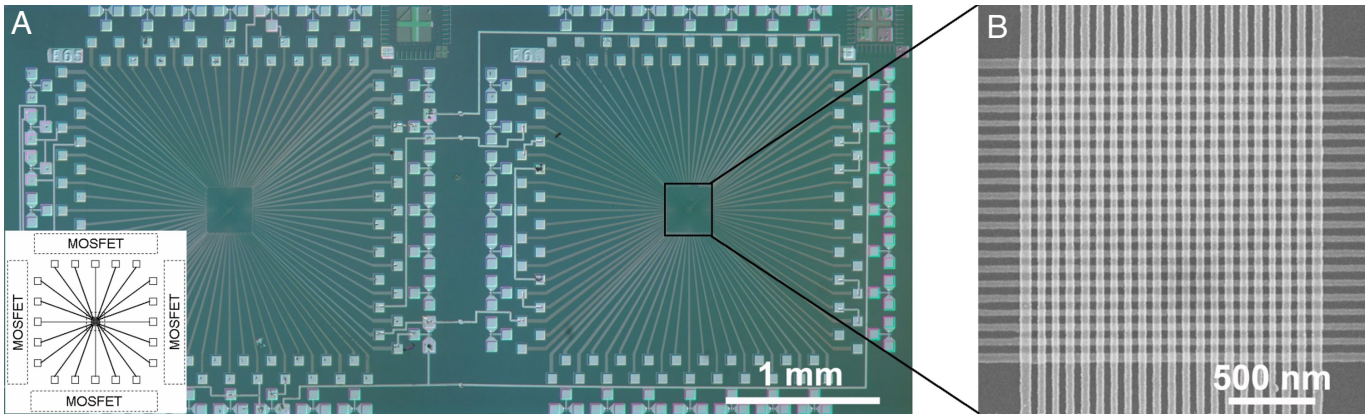

Fig. 1. A hybrid nanomemristor/transistor logic circuit. (*A*) Optical micrographs of 2 interconnected nanocrossbar/FET hybrid circuits. (*Inset*) Schematic of a single nanocrossbar device showing the relative layout of the crossbar, the fan-out and the FETs. (*B*) Scanning electron microscope image of 1 nanocrossbar region.

Results and Discussion

Fig. 1 shows 2 interconnected hybrid memristor-crossbar/FET circuits. The Fig. 1*A Inset* illustrates the layout of each circuit: 4 linear arrays of FETs with large contact pads for the source, drain and gate were fabricated to form a square pattern; the memristor crossbar, which included fan out to contact pads on both sides of each nanowire, was fabricated within the square defined by the FETs but on top of an intervening spacer layer. The metal traces to interconnect the crossbar fan-out pads and the FET source/drain and gate pads were fabricated using photolithography and Reactive Ion Etching (RIE) to create vias in the spacer layer, followed by metal deposition and liftoff. A magnified view of the crossbars is in Fig. 1*B*, showing the 21 horizontal (*Upper*) and 21 vertical (*Lower*) nanowires, each 40 nm wide, with a ≈20-nm-thick active layer of the semiconductor TiO_2 sandwiched in between the top and bottom nanowires to form the memristors.

Fig. 2 shows the typical current vs. voltage (I–V) electrical behavior for the initial ON-switching of a nanoscale memristor at a crossbar junction. The TiO_2 active layer of the as-fabricated device is an effective electrical insulator as measured in the two bottom traces for positive and negative voltage sweeps. When a small amplitude bias sweep is applied to a junction, $-2\ \mathrm{V} < V_{\mathrm{app}} < +2\ \mathrm{V}$, no resistance switching is observed within the typical sweep time window of several seconds. However, when a positive voltage larger than approximately +4 V is applied, the junction switches rapidly to an ON state that is >10,000 times more conductive. This conductance does not change perceptibly for at least 1 year when a programmed device is stored "on the shelf," but if subjected to alternate polarity bias voltages, such a device will undergo reversible resistance switching (4, 23), which is the basis for memristance. The apparent existence of a threshold voltage for switching is caused by the extremely nonlinear current-voltage characteristic of the TiO_2 film (4); at low bias voltage, the charge flowing through the device is very low, so resistance changes are negligible, but at higher voltage the current is exponentially larger, which means that the charge required to switch the device flows through it in a very short time (and thus it is more properly a memristive device). In the following, we will use this effective switching threshold voltage to program memristive junctions to demonstrate logic operations of the crossbar arrays.

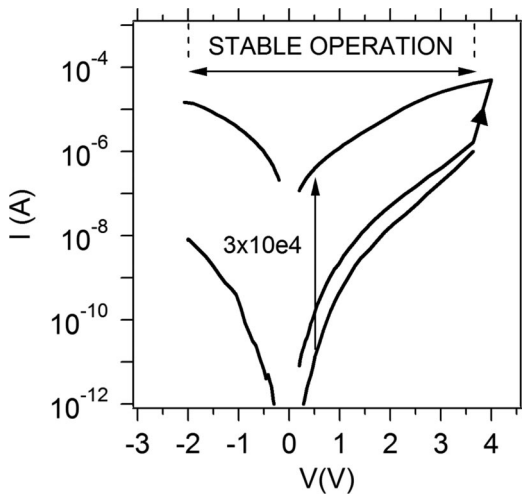

Fig. 2. Representative I–V traces of a nanoscale memristor. The OFF device has a high resistivity. A large positive bias ($V > 4$ V), with the resulting high current, rapidly switches a memristor to a more conductive state, the programmed-ON state. The stable operation window denotes the bias range, which does not significantly change the junction conductance for either the OFF or the programmed-ON state.

Programmable Logic Array. The equivalent circuit for testing the compound logic operation is shown schematically in Fig. 3*A*. This circuit computes AB + CD from 4 digital voltage inputs, V_{A} to V_{D}, representing the 4 input values A to D, respectively. The operations AB and CD are performed on 2 different rows in the crossbar, and the results are output to inverting transistors, which then restore the signal amplitudes and send voltages corresponding to NOT(AB) and NOT(CD), or equivalently A NAND B and C NAND D and denoted using Boolean algebra as $\overline{\mathrm{AB}}$ and $\overline{\mathrm{CD}}$, respectively, back onto the same column of the crossbar. There, the operation $\overline{\mathrm{AB}} \times \overline{\mathrm{CD}}$ is performed and the result is sent to another inverting transistor, which outputs the result $\overline{\overline{\mathrm{AB}} \times \overline{\mathrm{CD}}} = \overline{\overline{\mathrm{AB}}} + \overline{\overline{\mathrm{CD}}} = \mathrm{AB} + \mathrm{CD}$, following from De Morgan's Law, as an output voltage level on V_{OUT}. The signal path is emphasized by the thick colored lines in Fig. 3*A*: red–blue–green from the inputs to the output. In red, 2 programmed-ON memristors are linked to a transistor gate to perform as a NAND logic gate with the inputs V_{A} and V_{B} in one operation or V_{C} and V_{D} in the other. In blue, the outputs from the first 2 logic gates are then connected to the second stage NAND gate formed from 2 other programmed-ON memristors and 1 transistor. The green line shows the output voltage.

This experiment began with the configuration of the array. The conductivity of all of the crossbar nanowires was measured by making external connections with a probe station to the

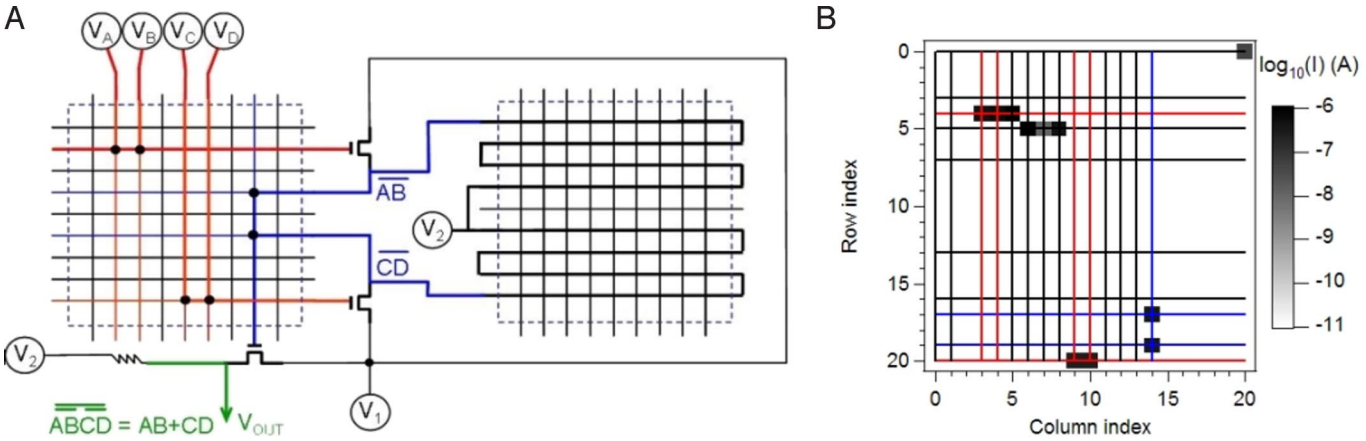

Fig. 3. Programmed memristor map and transistor interconnections. (*A*) Equivalent circuit schematic of the hybrid programmable logic array. The dashed lines define the nanocrossbar boundary, the black dots are the programmed memristors, V_A through V_D are the 4 digital voltage inputs and V_{OUT} is the output voltage. V_1 and V_2 are the transistor power supply voltage inputs. A single nanowire has a resistance of ≈33 kΩ, and 4 connected in series provides a ≈130-kΩ on-chip load resistor for a transistor. (*B*) Map of the conductance of the memristors in the crossbar. The straight lines represent the continuous nanowires, and their colors correspond to those of the circuit in *A*. The broken nanowires are the missing black lines in the array. The squares display the logarithm of the current through each memristor at a 0.5-V bias.

contact pads at the ends of the fanout wires connected to each nanowire, and those that were not broken or otherwise defective are shown as straight black or colored lines in Fig. 3*B*. More than 90% of the addressable nanomemristors in a typical crossbar passed the electrical test to show that they were in their desired state, but in some cases a significant number of the memristors were not addressable because of broken nanowires or other structural problems not related to the junctions. After mapping the working resources, the circuit to compute AB + CD was then designed, which is what a defect-tolerant compiler for a nanoscale computer would need to do (15). Each required programmed-ON memristor was configured by externally applying a voltage pulse of +4.5 V across its contacting nanowires, whereas all other memristors in the row and column of the target junction were held at 4.5/2 = 2.25 V, a voltage well below the effective threshold such that those junctions were not accidentally programmed ON. Fig. 3*B* displays in various colors the nanowires in the crossbar selected from those that were determined to be good and the conductance map for the programmed-ON memristors. The gray-scale squares display the current through the individual memristors upon the application of a test voltage of 500-mV bias. There was a large conductance difference between the OFF state memristors (white, corresponding to I <10 pA) and the programmed-ON junctions (black, I ≈ 1 uA). The conductance map can be compared with the schematic circuit diagram in Fig. 3*A*. The inputs V_A and V_B are connected to the memristors at columns 3 and 4 and row 4. Row 4 is also connected to a transistor gate, as can be seen from Fig. 1*A*. The inputs V_C and V_D are connected to the junctions at columns 9 and 10 and row 20. The 2 junctions routing the outputs of the first stage transistors are at column 14 and rows 17 and 19. The actual connections to the transistors can also be seen in the photograph in Fig. 1*A*.

The logic operations were tested with voltages in the 0- to 1-V range to avoid any accidental programming of memristors in the crossbar. The junction states must be robust with respect to a voltage stress for both positive and negative biases, because the signals are routed by the top and the bottom nanowires. The operation of the $\overline{AB}$ NAND gate is described here. Two voltage sources were connected to contact pads leading to 2 programmed-ON memristors sharing a single nanowire, the latter being connected to the high impedance(s) of a transistor gate or/and an oscilloscope. The output voltage of the NAND gate was 1 V when $V_A = V_B = 1$ V, which represented a binary 1 logic value, or it was in the range 0.5 V to 0 V, which represented a binary 0. The level 0.5 V was expected when 1 V and 0 V were applied to 2 identical junctions that essentially act as a voltage divider. In the memristor-crossbar framework (9, 16, 24), this represents a wired-AND gate, where the horizontal nanowire carries the output voltage. The experimentally measured margin between the high (1) and low (0) levels at the output of the wired-AND gate was 0.4 V because of nonuniformities in the programmed-ON memristors. To amplify the margin, the horizontal nanowire was connected to the gate of an n-type silicon FET biased in the inverter mode, which produced an inverted output voltage with a 0.8-V margin. A positive voltage ($V_2 \sim 1.5$ V) was applied to the transistor drain through a

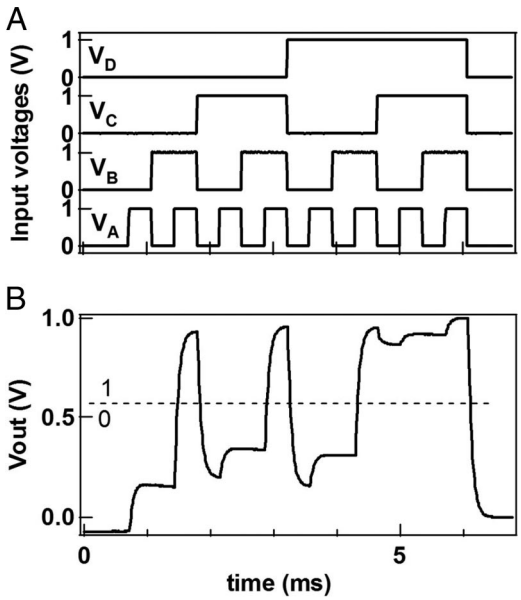

Fig. 4. Operation of the logic circuit. (*A*) The time sequence of the input voltage pulses used to represent the logic values 1 and 0 for the 4 inputs A through D, and (*B*) the output voltage versus time that represents the 16 outcomes from the 4-input compound logic operation AB + CD. The operating frequency was 2.8 kHz and the voltage margin separating the highest low signal from the lowest high signal was 0.52 V.

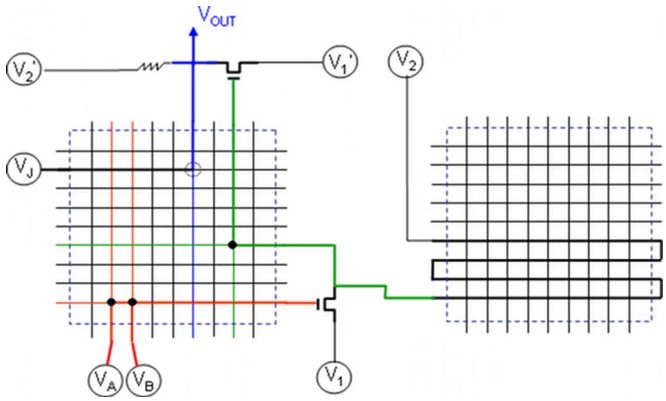

Fig. 5. Equivalent circuit schematic for the conditional programming demonstration. The initially programmed memristors are marked by filled black circles, and the target memristor for configuration by an open black circle. V_A and V_B are the logic value inputs; V_1, V_2, V_1' and V_2' are the transistor voltage supplies and V_J addresses the target memristor.

133-kΩ load (which was formed from a configured set of nanowires in the rows of an adjacent crossbar, shown schematically in Fig. 3*A*) to keep the FET output voltage in the 0- to 1-V range when the gate voltage was swept from 0 V to 1 V.

The NAND gate with inputs V_C and V_D had the identical operation mode with similar voltages and margin. The second logic stage was similar to the first stage NANDs but (*i*) the signals were delivered from integrated transistors rather than external voltage sources and (*ii*) there was a possible cross-talk channel between the nanowires shown schematically as red and blue in Fig. 3*A*, if the memristor between those two wires had a nonnegligible conductivity. In fact, the entire circuit behaved as the expected AB + CD logic operation and had a 0.52-V margin between the high and low signals at V_{OUT} at an operating frequency of 2.8 kHz. Fig. 4*A* shows the time dependence of the 4 voltage pulse traces V_A to V_D acting as the inputs to the compound logic operation, and Fig. 4*B* shows the 16 results of the 4-input logic operation measured as the voltage on V_{OUT}. The speed of the circuit was actually limited by the load on the output transistor, which had to charge the parasitic capacitance of the measurement cabling. There was a second transistor connected to the top of the vertical nanowire shown as blue in Fig. 3*A* that, when biased in follower mode, could increase the operating frequency of the 4-input logic operation to 10 kHz, but at the price of a lower margin (0.21 V) and restricted voltage range (−0.6 V to −1.3 V).

Self-Programming of a Nanocrossbar Memristor. The above experiments were existence proofs for several proposed hybrid architectures involving wired logic (24) and routing in a configured crossbar (5, 9, 10, 12, 16). A completely different type of demonstration is the conditional programming of a memristor by the integrated circuit in which it resides, which illustrates a key enabler for a reconfigurable architecture (21, 22, 25), memristor based logic (24) or an adaptive (or "synaptic") circuit that is able to learn (26, 27). Based on a portion of the hybrid circuit described above, we showed that the output voltage from an operation could be used to reprogram a memristor inside the nanocrossbar array, which could have been used as memory, an electronic analog of a synapse or simply interconnect, to have a new function.

The electrical circuit is shown schematically in Fig. 5. For simplicity, the operation used was a single NAND with inputs V_A

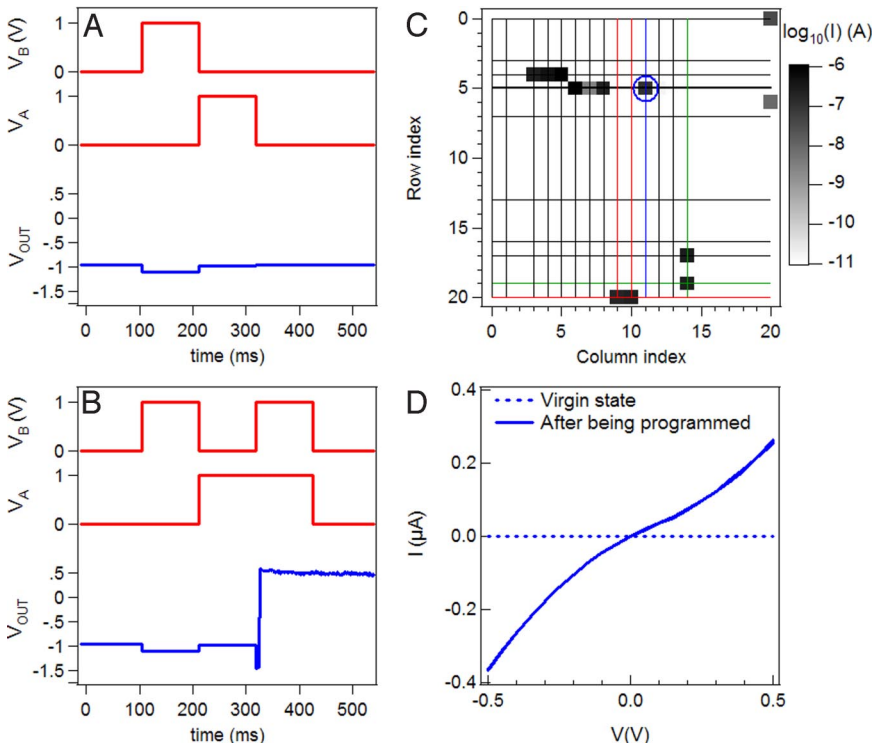

Fig. 6. Self-programming demonstration. (*A*) Input (red) and output (blue) voltages for testing the conditional programming, where the inputs do not include a true event for the AND operation. (*B*) Input (red) and output (blue) voltages where the inputs do include a true event for the AND operation–the memristor switched ON rapidly after the rising edge (6 ms) of the A = 1,B = 1 pulse pair. (*C*) Conductance map of the crossbar after the conditional programming, to be compared with the previous map in Fig. 2*B*. The target memristor is indicated by a blue circle. The color pattern of the nanowires refers to the schematic circuit of Fig. 5. (*D*) I–V traces of the target memristor before and after the conditional programming experiment, which show that the device switched from an open or OFF state to a highly conductive ON state after the single programming pulse from the logic operation shown in *B*.

and V_B, but it could be any digital or even analog signal that originates from within the circuit. The output signal (green lines in Fig. 5) was routed through a memristor to a 2nd stage transistor that delivered a voltage V_{OUT} to the target junction (circled in Figs. 3*B* and 6*C*). This transistor was biased in the follower mode: $V_1'' = +1$ V was applied to the drain and $V_2'' = -4$ V through a 133-kΩ resistor was applied to the source. The amplification factor was $\approx$0.8, and the resting bias $V_{OUT} = V_S$ was -1 V. The target memristor addressing voltage V_J for the target memristor was tweaked to $+3.2$ V, such that the voltage drop across this junction was slightly below the threshold ($V_J - V_S = 4.5$ V) when the circuit was at rest.

Fig. 6*A* shows the 2 input and the output signals when the inputs V_A and V_B did not include a TRUE event for the A AND B operation. The output voltage remained essentially constant at the resting voltage. Fig. 6*B* shows V_{OUT} when the inputs included a TRUE event, for which the output voltage reached -1.45 V and the voltage drop across the memristor exceeded the threshold voltage ($V_J - V_{OUT} = 4.65$ V). After only 6 ms at such bias above the threshold, the measured V_{OUT} jumped from -1.45 V to $+0.5$ V as the result of the large increase in conductivity of the junction separating V_J from V_{OUT}, indicating that the memristor had been programmed-ON.

To verify the programming of the junction, the conductance map of the entire crossbar (Fig. 6*C*) and the target memristor I–V characteristic (Fig. 6*D*) were measured. Comparing Fig. 6 *C* with Fig. 3*B* shows the programming of the crossbar was changed by the logic operation. However, there were also two undesired effects. The memristor connecting the column 7 and row 5 nanowires suffered a slight relaxation of its programmed state, and an additional memristor connecting column 20 with row 6 was apparently programmed. The latter effect could have been caused by an unanticipated leakage path in the array during the programming event, or given its placement it was most likely the result of an accidental electrical discharge during the sample handling.

Summary. We built and tested hybrid integrated circuits that interconnected two 21×21 nanoscale memristor crossbars and several conventional silicon FETs. This prototype was first a necessary step to develop the processing procedures that will be needed for physically integrating memristors with conventional silicon electronics, second a test bed to configure and exercise the building blocks of several proposed hybrid memristor/transistor architectures (9, 15, 16, 17, 21, 22, 24–27), and finally a successful proof-of-principles demonstration of the ability of such a system to alter its own programming. The particular demonstrations involved the simultaneous routing of multiple signals through a nanocrossbar from and to FETs and the realization of a Boolean sum-of-product operation, where the FETs provided voltage margin restoration and signal inversion after the wired-AND operations and impedance matching to improve the operating frequency. The self-programming of the memristor crossbar constituted the primary result of this research report and illuminates the way toward further investigations of a variety of new architectures, including adaptive synaptic circuits (26, 27).

Methods

Construction of the hybrid circuits began with the fabrication of n-type FETs on silicon-on-insulator (SOI) wafers to prove that the entire process was compatible with CMOS processing techniques. The process is similar to that reported in ref. 28 and is briefly described here. The SOI wafer with a 50-nm-thick Si device layer was first ion-implanted with boron to a doping level of 3×10^{18}/cm^3. The source and drain regions where the transistors would be located were then ion-implanted with phosphorous to a doping density of 10^{20}/cm^3. A 5-nm-thick oxide was thermally grown as the gate dielectric layer over the channels with lateral dimensions of 3×5 μm^2 defined by the photolithography process. Aluminum was then deposited to construct the gate, source, and drain contacts of the n-type FETs. Subsequently, 300 nm of plasma-enhanced chemical vapor deposition (PECVD) oxide was deposited as a protective, passivation layer to cover the FET arrays. Then, an additional 700-nm layer of UV-imprint resist was spin coated onto the wafer and cured to act as a planarization layer. The nanocrossbars were fabricated on top of this substrate with UV-imprinting processes for each layer of the nanowires and their fanouts to the electrical contact pads. The active memristor layer, which was deposited on top of the first layer of metal wires by 5 cycles of blanket electron-beam evaporation of 1.5-nm Ti films immediately followed by an oxygen plasma treatment, was sandwiched between the top and bottom nanowires. A RIE process was used to remove the blanket titanium dioxide between the top nanoelectrodes. Finally, to make electrical connections between the nanocrossbar fanouts and the FET terminals, photolithography was used to define the location of vias that were then created by RIE through the planarization and PECVD silicon oxide layers. Al metal was evaporated through the vias to connect the appropriate nanowire contact pads with their corresponding FET terminals and probe pads to complete the hybrid circuit. The net yield of addressable and functional memristive devices observed in these experiments was only $\approx$20%, which was mainly due to broken leads and/or nanowires to the nanojunctions resulting from the unoptimized imprinting process. However, $>$90% of the addressable memristors were operational when tested.

ACKNOWLEDGMENTS. We thank Philip J. Kuekes, Gregory S. Snider, and Dmitri Strukov for valuable discussions. This work was partially supported by the Defense Advanced Research Projects Agency.

1. Chua LO (1971) Memristor—The missing circuit element. *IEEE Tran Circuits Theory* 18:507–519.
2. Chua L, Kang S (1976) M Memristive devices and systems. *Proc IEEE* 64:209–223.
3. Strukov D, Snider G, Stewart D, Williams R (2008) The missing memristor found. *Nature* 453:80–83.
4. Yang JJ, *et al.* (2008) Memristive switching mechanism for metal/oxide/metal nanodevices. *Nat Nanotechnol* 3:429–433.
5. Collier C, *et al.* (1999) Electronically configurable molecular-based logic gates. *Science* 285:391–394.
6. Rueckes T, *et al.* (2000) Carbon nanotube-based nonvolatile random access memory for molecular computing. *Science* 289:94–97.
7. Chen Y, *et al.* (2003) Nanoscale molecular-switch crossbar circuits. *Nanotechnology* 14:462–468.
8. Huang Y, *et al.* (2001) Logic gates and computation from assembled nanowire building blocks. *Science* 294:1313–1317.
9. Stan M, Franzon P, Goldstein S, Lach J, Ziegler M (2003) Molecular electronics: From devices and interconnect to circuits and architecture. *Proc IEEE* 91:1940–1957.
10. Heath J, Ratner M (2003) Molecular electronics. *Physics Today* 56:43–49.
11. Reed M, Zhou C, Muller C, Burgin T, Tour J (1997) Conductance of a molecular junction. *Science* 278:252–254.
12. Kaeriyama, *et al.* (2005) A nonvolatile programmable solid-electrolyte nanometer switch. *IEEE SolState Circ* 40:168–176.
13. Donhauser Z, *et al.* (2001) Conductance switching in single molecules through conformational changes. *Science* 292:2303–2307.
14. Lau C, Stewart D, Williams R, Bockrath M (2004) Direct observation of nanoscale switching centers in metal/molecule/metal structures. *Nano Lett* 4:569–572.
15. Heath J, Kuekes P, Snider G, Williams R (1998) A defect-tolerant computer architecture: Opportunities for nanotechnology. *Science* 280:1716–1721.
16. DeHon A (2003) Array-based architecture for FET-based, nanoscale electronics. *IEEE Trans Nanotechnol* 2:23–32.
17. Snider G (2007) Self-organized computation with unreliable, memristive nanodevices. *Nanotechnology* 18:365202.
18. Chou S, Krauss P, Renstrom P (1996) Imprint lithography with 25-nanometer resolution. *Science* 272:85–87.
19. Jung G, *et al.* (2006) Circuit fabrication at 17 nm half-pitch by nanoimprint lithography. *Nano Lett* 6:351–354.
20. Kuekes P, Stewart D, Williams R (2005) The crossbar latch: Logic value storage, restoration, and inversion in crossbar circuits. *J App Phys* 97:034301–034305.
21. Strukov D, Likharev K (2005) CMOL FPGA: A reconfigurable architecture for hybrid digital circuits with two-terminal nanodevices. *Nanotechnology* 16:888–900.
22. Snider G, Williams R (2007) Nano/CMOS architectures using a field-programmable nanowire interconnect. *Nanotechnology* 18:035204.
23. Argall F (1967) Switching phenomena in titanium oxide thin films. *Sol State Elec* 11:535–541.
24. Snider G (2005) Computing with hysteretic resistor crossbars. *Appl Phys A* 80:1165–1172.
25. Strukov D, Likharev K (2007) Reconfigurable hybrid CMOS/nanodevice circuits for image processing. *IEEE Trans Nanotechnol* 6:696–708.
26. Snider G (2008) Spike-timing-dependent learning in memristive nanodevices. IEEE Int. Symp. on Nanoscale Architectures: 85–92.
27. Likharev K, Mayr A, Muckra I, Türel O (2003) CrossNets: High-Performance Neuromorphic Architectures for CMOL Circuits. *Ann NY Acad Sci* 1006:146–163.
28. Li Z, *et al.* (2008) Fabrication and test of nano crossbar switches/MOSFET hybrid circuits by imprinting lithography. *Proc of SPIE* 6921:692108.